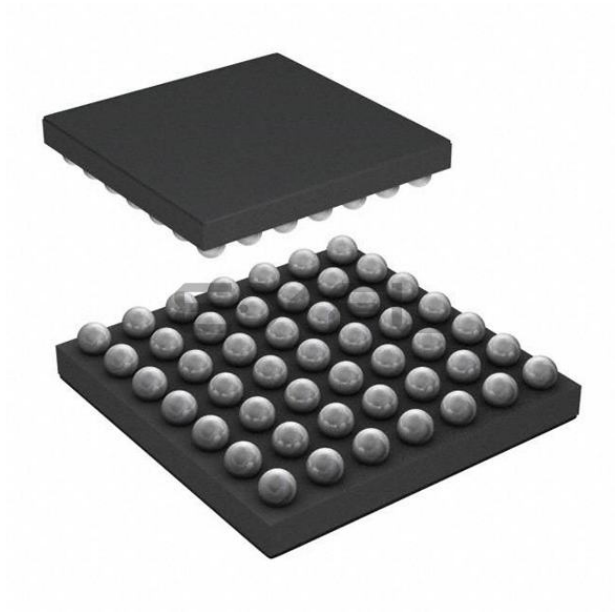

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0+
Core Size	32-Bit Dual-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	39
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.29x3.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54102j512uk49z

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54102J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54102J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash/kB	Total SRAM/kB	Core M4 w/ FPU	Core M0+	GPIO
LPC54102J512UK49	LPC54102J512UK49Z	512	104	1	1	39
LPC54102J256UK49	LPC54102J256UK49Z	256	104	1	1	39
LPC54101J512UK49	LPC54101J512UK49Z	512	104	1	0	39
LPC54101J256UK49	LPC54101J256UK49Z	256	104	1	0	39
LPC54102J512BD64	LPC54102J512BD64QL	512	104	1	1	50
LPC54102J256BD64	LPC54102J256BD64QL	256	104	1	1	50
LPC54101J512BD64	LPC54101J512BD64QL	512	104	1	0	50
LPC54101J256BD64	LPC54101J256BD64QL	256	104	1	0	50

[1] All of the parts include five 32-bit general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I2C-bus interfaces with high-speed slave mode, and one 12-bit 5.0 Msamples/sec ADC.

4. Marking

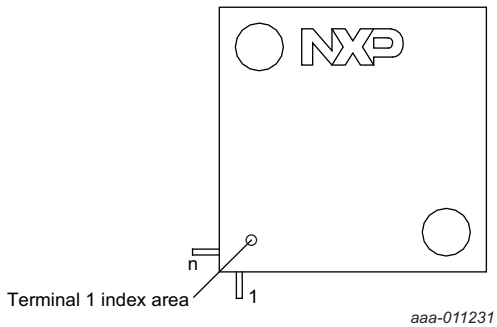


Fig 1. LQFP64 package marking

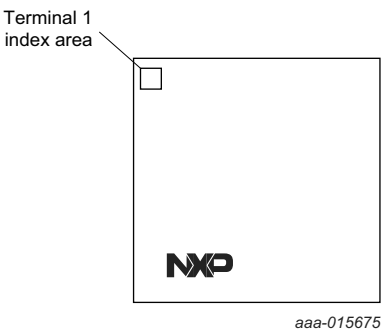


Fig 2. WLCSP49 package marking

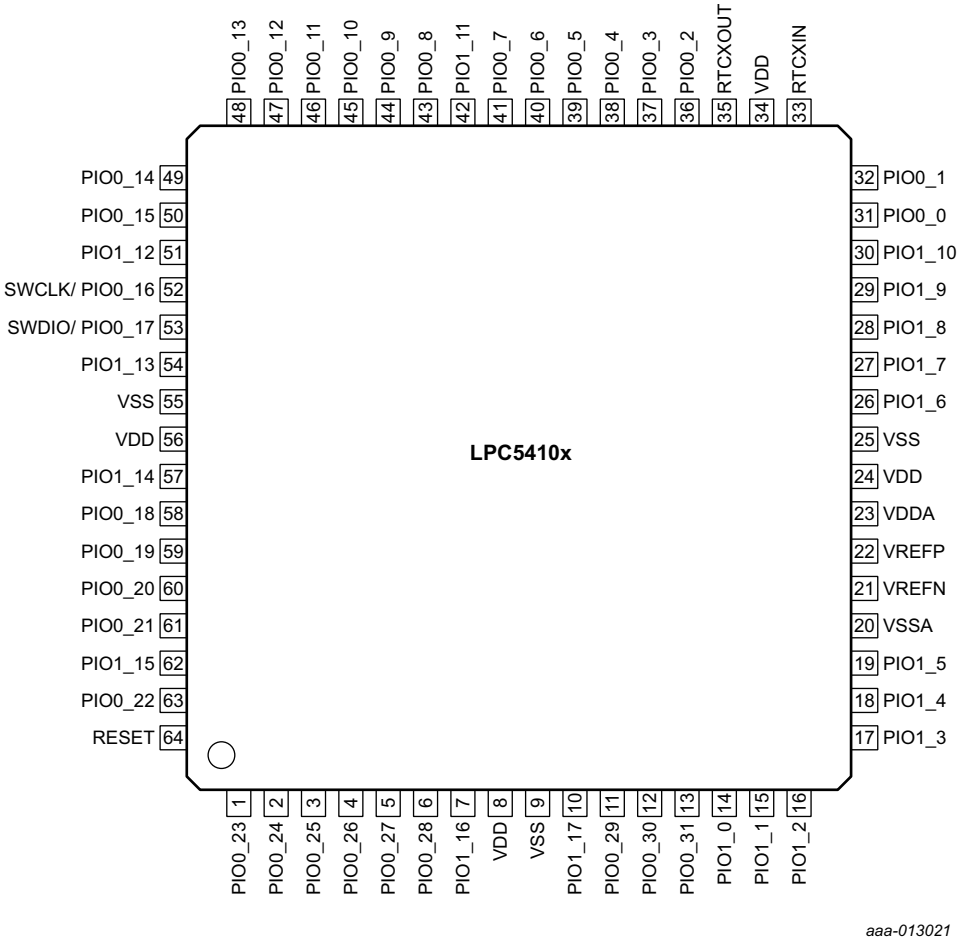


Fig 5. LQFP64 Pin configuration

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
					I/O	**I2C0_SDA —** I^2C0 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**I2C1_SCL —** I^2C1 clock input/output.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.
					I	**CT32B1_CAP1 —** 32-bit CT32B1 capture input 1.
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**I2C1_SDA —** I^2C1 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					I	**R —** Reserved.
PIO0_27	D2	5	[3]	Z	I/O	**PIO0_27 —** General-purpose digital input/output pin.
					I/O	**I2C2_SCL —** I^2C2 clock input/output.
					I	**R —** Reserved.
					I	**CT32B2_CAP0 —** 32-bit CT32B2 capture input 0.
					I	**R —** Reserved.
PIO0_28	D1	6	[3]	Z	I/O	**PIO0_28 —** General-purpose digital input/output pin.
					I/O	**I2C2_SDA —** I^2C2 data input/output.
					I	**R —** Reserved.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin (default). ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT2 —** SCT0 output 2.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_3/ ADC0_6	B2	17	[4]	PU	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin (default). ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL2 —** Slave Select 2 for SPI1.
					O	**SCT0_OUT6 —** SCT0 output 6.
					I	**R —** Reserved.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
PIO1_4/ ADC0_7	A2	18	[4]	PU	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin (default). ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I	**R —** Reserved.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO1_5/ ADC0_8	B3	19	[4]	PU	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin (default). ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO1_6/ ADC0_9	A5	26	[4]	PU	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin (default). ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					-	**R —** Reserved.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					I	**R —** Reserved.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_7/ ADC0_10	B5	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin (default). ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MOSI —** Master Out Slave in for SPI1.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					-	**R —** Reserved.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					I	**R —** Reserved.
PIO1_8/ ADC0_11	C5	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin (default). ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I	**R —** Reserved.
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I/O	**SPI0_MOSI —** Master Out Slave In for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U3_RXD —** Receiver input for USART3.
					O	**CT32B1_MAT0 —** 32-bit CT32B1 match output 0.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U3_TXD —** Transmitter output for USART3.
					O	**CT32B1_MAT1 —** 32-bit CT32B1 match output 1.
					I/O	**SPI1_MOSI —** Master Out Slave In for SPI1.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M4 and ARM Cortex-M0+ cores include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The LPC5410x support 104 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC5410x supports 512 kB of on-chip flash memory.

7.11 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- Power control API for configuring power consumption and PLL settings.

- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.15 AHB peripherals

7.15.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.15.1.1 Features

- 22 channels, 21 of which are connected to peripheral DMA requests. These come from the USART, SPI, and I^2C peripherals. One spare channels has no DMA request connected, and can be used for functions such as memory-to-memory moves.
- DMA operations can be triggered by on- or off-chip events. Each DMA channel can select one trigger input from 20 sources. Trigger sources include ADC interrupts, Timer interrupts, pin interrupts, and the SCT DMA request lines.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.16 Digital serial peripherals

7.16.1 USART

7.16.1.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- Maximum supported bit rate of 24 Mbit/s for USART master and slave synchronous modes.
- 7, 8, or 9 data bits and 1 or 2 stop bits.

- FIFO support from the System FIFO.
- Activity on the SPI in slave mode allows wake-up from deep sleep and power down modes on any enabled interrupt.

7.17 I²C-bus interface

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.17.1 Features

- All I²Cs support standard (up to 100 Kbits/s), fast mode (up to 400 Kbits/s), and Fast-mode Plus (up to 1 Mbit/s).
- All I²Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports System Management Bus (SMBus).
- No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from power down mode.
- Supports the I²C-bus specification up to Fast-mode Plus (FM+, up to 1 MHz) in both master and slave modes. High-speed (HS, up to 3.4 MHz) I²C is support in slave mode only.
- Activity on the I²C in slave mode allows wake-up from deep sleep and power down modes on any enabled interrupt.

7.18 Counter/timers

7.18.1 General-purpose 32-bit timers/external event counter

The LPC5410x includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.18.1.1 Features

- Each is a 32-bit counter/timer with a programmable 32-bit prescaler. Four of the timers include external capture and match pin connections.

7.20.4.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain and the $\overline{\text{RESET}}$ pin. The LPC5410x can wake up from deep power down mode via the $\overline{\text{RESET}}$ pin and the RTC alarm.

7.20.5 Brownout detection

The LPC5410x includes a monitor for the voltage level on the V_{DD} pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold levels can be selected to cause chip reset and interrupt.

7.20.6 Safety

The LPC5410x includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

7.21 Code security (Code Read Protection - CRP)

This feature of the LPC5410x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry can be invoked by pulling a pin on the LPC5410x LOW on reset. This pin is called the ISP entry pin.

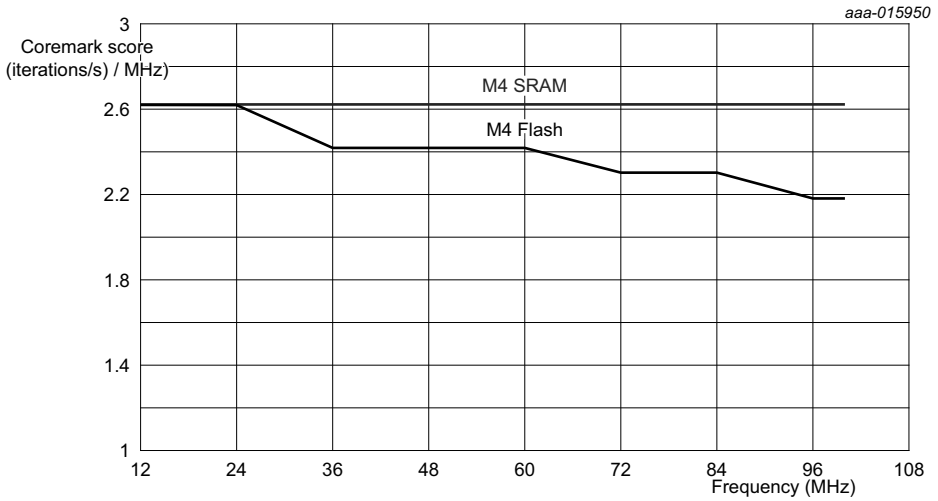
There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. CRP3 fully disables any access to the chip via SWD and ISP. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or a call to reinvoke ISP command to enable a flash update via USART.
4. In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled (No_ISP mode). For details, see the LPC5410x user manual.

CAUTION	
	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

[5] SRAM0 and SRAM1 powered, SRAM2 powered down.

[6] See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART; BOD disabled; SRAM0 and SRAM1 powered, SRAM2 powered down. See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings. Measured with Keil uVision 5.12. Optimization level 3, optimized for time on.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 8. Typical CoreMark score

Table 13. Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes
T_{amb} = −40 °C to +105 °C, 2.7 V ≤ V_{DD} ≤ 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep sleep mode; all SRAM on:	[2]	-			
		T_{amb} = 25 °C			306	480	µA
		T_{amb} = 105 °C		-	-	2.3	mA
		Power down mode;	[2]				
		first 8 kB in SRAM0 powered:					
		T_{amb} = 25 °C		-	5	10	µA
		T_{amb} = 105 °C		-	-	115	µA
		SRAM0 (64 kB) powered		-	7.3	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB) powered		-	8.6	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB), SRAM2 (8 kB) powered		-	9	-	µA
		Deep power-down mode;	[2]				
		RTC oscillator input grounded (RTC oscillator disabled)					
		T_{amb} = 25 °C		-	200	570	nA
		T_{amb} = 105 °C			-	20	µA
		RTC oscillator running with external crystal		-	280	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples. V_{DD} = 3.3 V

[3] Tested in production, V_{DD} = 3.6 V

Table 15. Typical AHB/APB peripheral power consumption[3][4][5]

V_{DD} = 3.3 V; T = 25 °C

Peripheral		I_{DD} in μA	I_{DD} in μA/MHz	I_{DD} in μA/MHz
FIFO		-	3.17	4.49
Sync APB peripheral			**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 96MHz, sync APB bus: 96 MHz**
INPUTMUX	[1]	-	0.83	0.96
IOCON	[1]	-	1.25	1.55
PINT		-	0.83	1.05
GINT		-	0.50	0.61
WWDT		-	0.17	0.28
MRT		-	0.50	0.65
RTC		-	0.08	0.09
RIT		-	0.50	0.71
UTICK		-	0.17	0.11
Timer2		-	0.58	0.67
Timer3		-	0.42	0.42
Timer4		-	0.50	0.57
Async APB peripheral			**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 96MHz, Async APB bus: 12 MHz[2]**
USART0		-	0.67	0.11
USART1		-	0.75	0.07
USART2		-	0.67	0.11
USART3		-	0.75	0.07
I2C0		-	0.92	0.10
I2C1		-	0.83	0.26
I2C2		-	0.83	0.25
SPIO0		-	0.92	0.21
SPIO1		-	0.83	0.25
CTimer0		-	0.58	0.18
CTimer1		-	0.42	0.14
Fractional Rate Generator		-	4.17	0.73

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG register. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz and 96 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

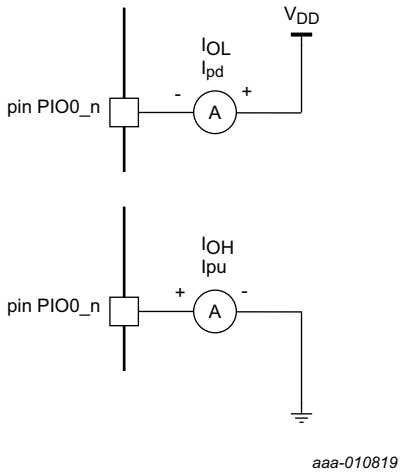
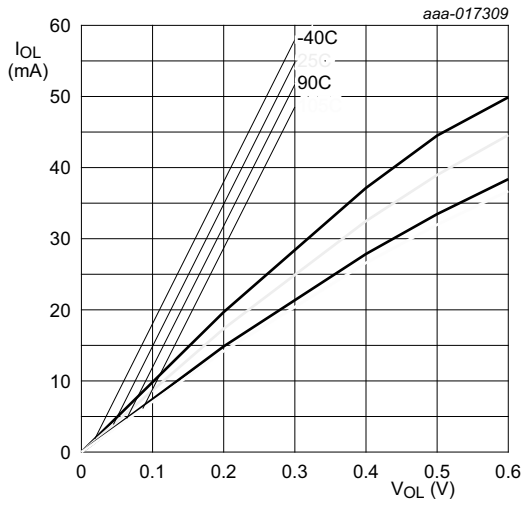
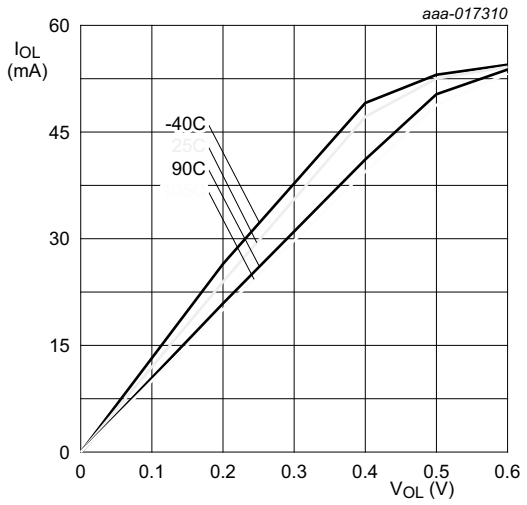


Fig 13. Pin input/output current measurement

10.4.1 Electrical pin characteristics

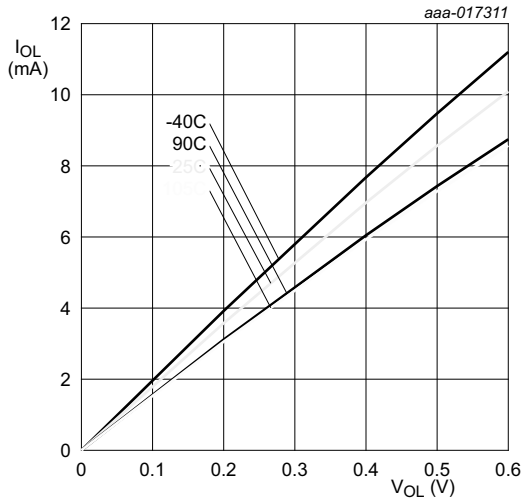


Conditions: V_{DD} = 1.8 V; on pins PIO0_23 to PIO0_28.

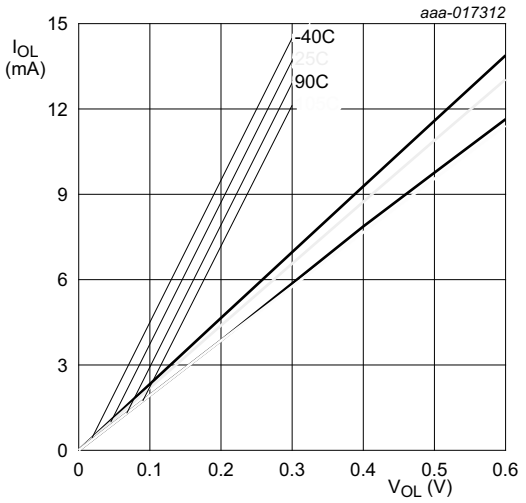


Conditions: V_{DD} = 3.3 V; on pins PIO0_23 to PIO0_28.

Fig 14. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

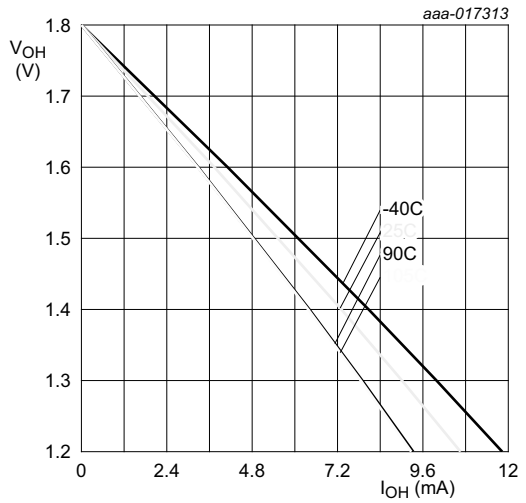


Conditions: V_{DD} = 1.8 V; on standard port pins.

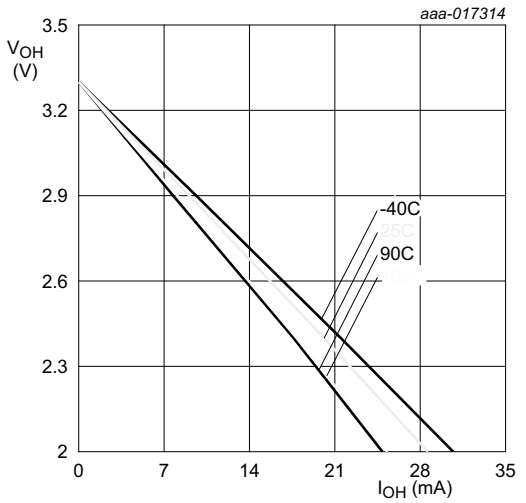


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 15. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 16. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

11.5 System PLL

Table 21. PLL lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.62 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL configuration: input frequency 12 MHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]			400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	550	µA
PLL configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]	-	-	400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	750	µA
PLL configuration: input frequency 32.768 kHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]			6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	450	µA
PLL configuration: input frequency 32.768 kHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]	-	-	6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	560	µA

[1] Data based on characterization results, not tested in production.

[2] PLL set-up requires high-speed start-up and transition to normal mode. Lock times are only valid when high-speed start-up settings are applied followed by normal mode settings. The procedure for setting up the PLL is described in the LPC5410x user manual.

[3] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

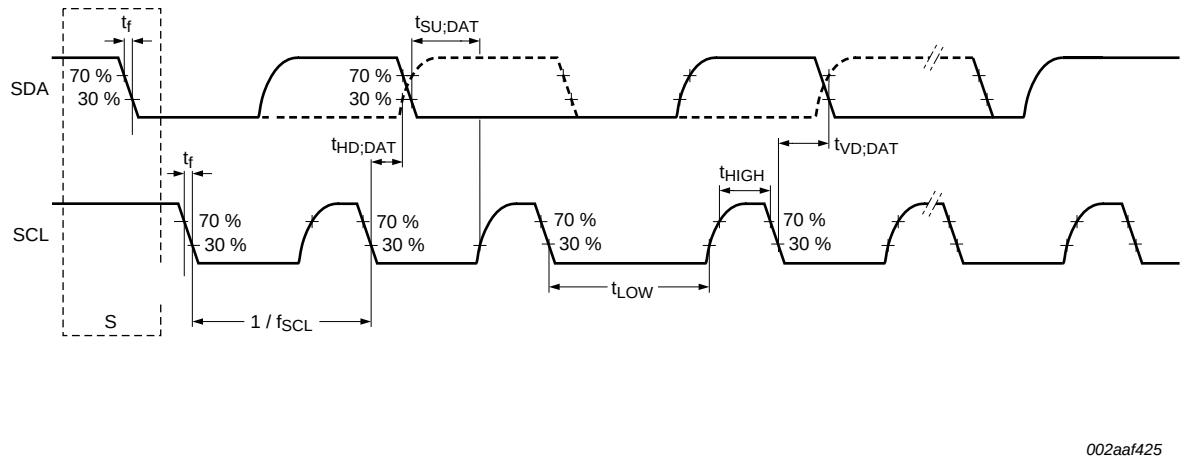
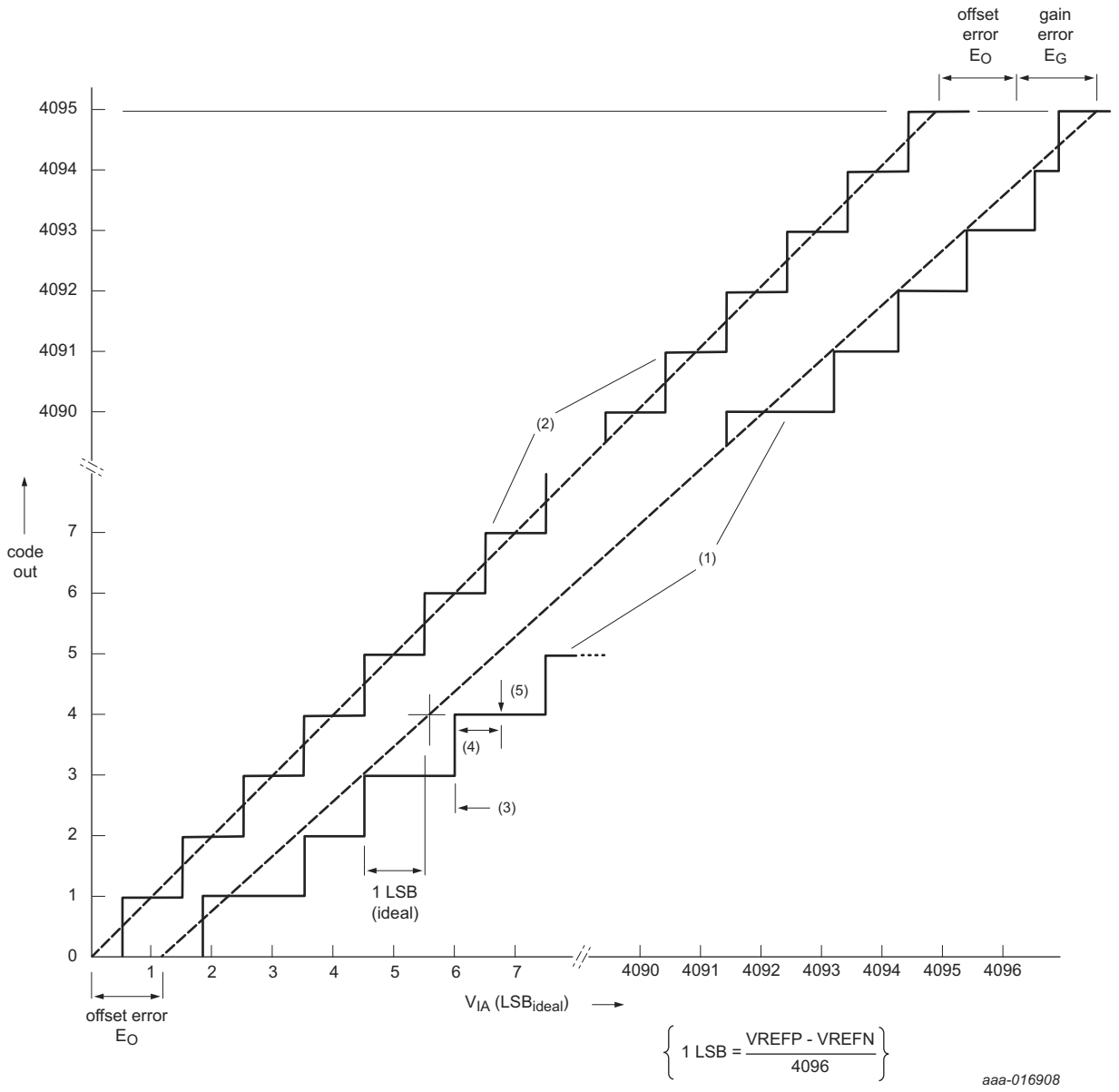


Fig 20. I^2C-bus pins clock timing



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 24. 12-bit ADC characteristics

13.2 Standard I/O pin configuration

Figure 27 shows the possible pin modes for standard I/O pins:

- Digital output driver: with configurable open-drain output.
- Digital input: pull-up resistor (PMOS device) enabled/disabled.
- Digital input: pull-down resistor (NMOS device) enabled/disabled.
- Digital input: repeater mode enabled/disabled.
- Digital input: programmable input digital filter and input inverter.
- Analog input: selected through IOCON register.

The default configuration for standard I/O pins is input with pull-up resistor enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

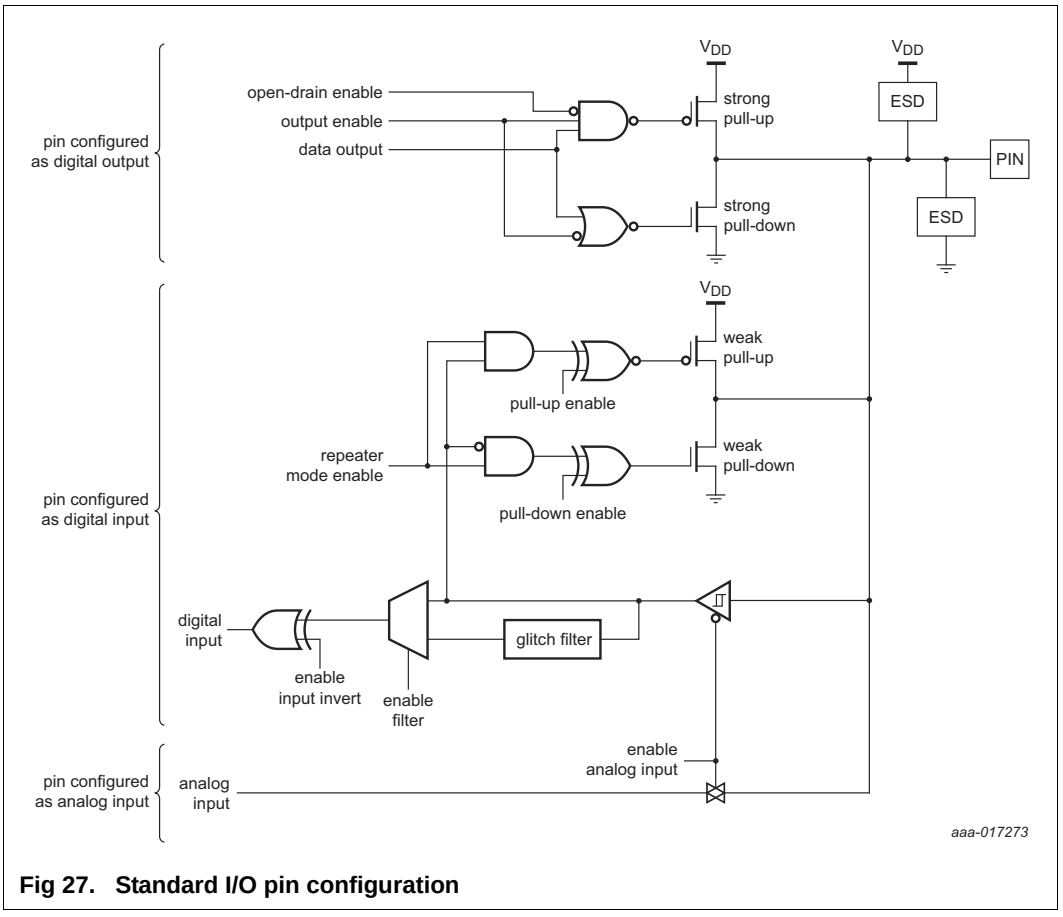


Fig 27. Standard I/O pin configuration

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to one of the GPIOs and optimize the values of external load capacitors for minimum frequency deviation.

Table 34. Recommended values for the RTC external 32.768 kHz oscillator C_L, R_S, D_L, and C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	Maximum crystal drive level D_L	External load capacitors C_{X1}/C_{X2}
12.5 pF	< 70 kΩ	0.5 μW	22 pF, 22 pF

Remark: The crystals with lower CL (< 12.5 pF) values are not recommended.

13.5.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible (within 20 mm) to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

Table 36. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modification:	• Updated Table 18 “Flash characteristics”: For N_{endu} conditions, removed the row with page erase/program; page in small sector 10000 and removed the word large so that it is "page erase/program;page in a sector". • Updated Section 7.16.1 “USART” features: changed maximum bit rates to 6.25 Mbit/s in asynchronous mode.			
LPC5410x v2.2	20151222	Product data sheet	201512007I	LPC5410x v2.1
Modification:	• Updated Section 11.6 “IRC”, Table 23 “Dynamic characteristic: IRC oscillator” for IRC frequency tolerance improvement over temperature. • Added boot code version and device revision. See Section 4 “Marking”. • Added the abbreviation ISP to the Remark: This pin is also used to force In-System Programming mode (ISP) after device reset. See the LPC5410x User Manual (Boot Process chapter) for details to PIO0_31. See Table 4 “Pin description”. • Removed 164 uA PLL spec in peripheral power consumption table, Table 15 “Typical AHB/APB peripheral power consumption[3][4][5]”. • Added Table 21 “PLL lock times and current”. • Updated Figure 10 “Deep sleep mode: Typical supply current IDD versus temperature for different supply voltages VDD”, Figure 11 “Power down mode: Typical supply current IDD versus temperature for different supply voltages VDD”, and Figure 12 “Deep power-down mode: Typical supply current IDD versus temperature for different supply voltages VDD”. • Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”: added max values to Deep sleep mode at 25 °C and 105 °C, Power down mode at 25 °C and 105 °C. Changed typ and max values for Deep power-down mode RTC oscillator input grounded (RTC oscillator disabled) at 25 °C; was: typ = 84 nA, max = 240 nA; now: typ = 160 nA, max = 340 nA. • Updated Table 13 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”: added max values to Deep sleep mode at 25 °C and 105 °C, Power down mode at 25 °C and 105 °C. Changed typ and max values for Deep power-down mode RTC oscillator input grounded (RTC oscillator disabled) at 25 °C; was: typ = 135 nA, max = 470 nA; now: typ = 200 nA, max = 570 nA. • Updated Table 7 “Limiting values”; VESD, electrostatic discharge voltage, human body model; all pins value to 4000 V; was 5000 V. • Updated Table 31 “12-bit ADC static characteristics”: ED differential linearity error, VDDA = VREFP = 1.62 V and 3.6 V, typ value ±3 and ±2; $EL_{(adj)}$ integral non-linearity, VDDA = VREFP = 1.62 V, typ value ±5; $V_{err(FS)}$ full-scale error voltage VDDA = VREFP = 1.62 V and 3.6 V, typ value to ±3			
LPC5410x v2.1	20150701	Product data sheet	-	LPC5410x v2.0
Modification:	• Updated Figure 3 “LPC5410x Block diagram”. Corrected Sync APB bridge to Async APB bridge. • Updated external clock input for clock frequencies of up to 24 MHz to 25 MHz in Section 2 “Features and benefits”. • Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”. Fixed the unit of the max value from nA to μA for IDD in deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled), T_{amb} = 105 °C.			