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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	PWM, WDT
Number of I/O	88
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 15x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f5nc8au-qip-e

■ Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■ Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

■ Interrupts

- 29 sources, 10 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer0/base timer1
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■ Subroutine Stack Levels: 2048 levels maximum (the stack is allocated in RAM)**■ High-speed Multiplication/Division Instructions**

- 16-bits $\times$ 8-bits (5 tCYC execution time)
- 24-bits $\times$ 16-bits (12 tCYC execution time)
- 16-bits $\div$ 8-bits (8 tCYC execution time)
- 24-bits $\div$ 16-bits (12 tCYC execution time)

■ Oscillation Circuits

- RC oscillation circuit (internal) : For system clock
- CF oscillation circuit : For system clock, with internal Rf
- Crystal oscillation circuit : For low-speed system clock
- Multifrequency RC oscillation circuit (internal) : For system clock

■ System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0 μ s, 2.0 μ s, 4.0 μ s, 8.0 μ s, 16.0 μ s, 32.0 μ s, and 64.0 μ s (at a main clock rate of 12MHz).

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■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) Canceled by a system reset or occurrence of interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC, and crystal oscillators automatically stop operation.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the low level.
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillators automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are four ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit

■On-chip Debugger Function

- Permits software debugging with the test device installed on the target board.

■Package Form

- QIP100E (14 × 20) : “Lead-free type”

■Development Tools

- Evaluation (EVA) chip : LC87EV690
- Emulator : EVA62S + ECB876600D + SUB875C00 + POD100QFP
ICE-B877300 + SUB875C00 + POD100QFP
- On-chip-debugger : TCB87-TypeB + LC87F5NC8A

■Programming Boards

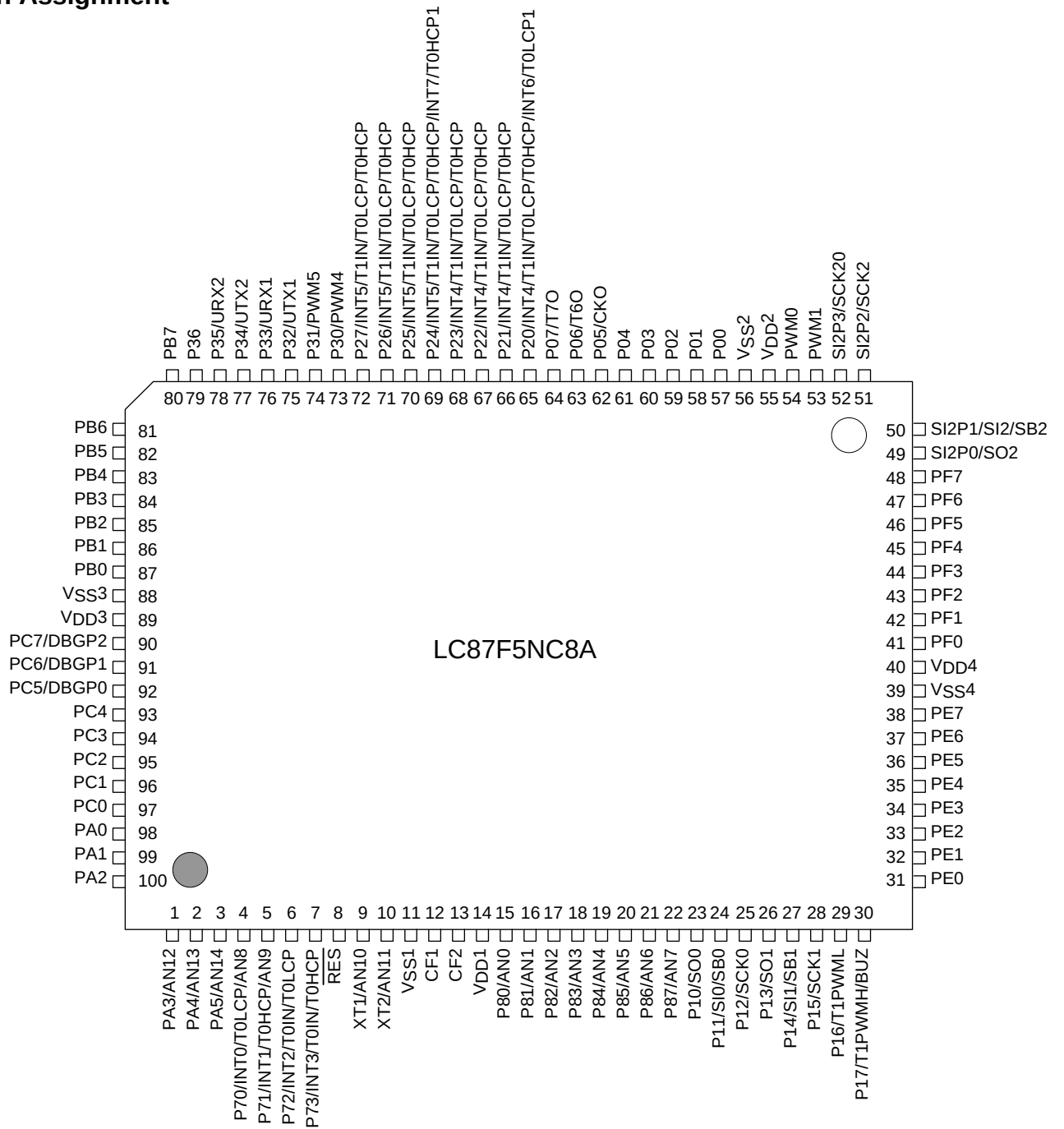
Package	Programming boards
QIP100E (14 × 20)	W87F52256Q

■Flash ROM Programmer

Maker	Model	Support version(Note)	Device
Flash Support Group, Inc. (Single)	AF9708/09/09B (including product of Ando Electric Co.,Ltd)	Revision : After Rev.02.73	LC87F76C8A
Flash Support Group, Inc.(Gang)	AF9723(Main body) (including product of Ando Electric Co.,Ltd)	Revision : After Rev.02.29	LC87F5NC8A
	AF9833(Unit) (including product of Ando Electric Co.,Ltd)	Revision : After Rev.01.88	
Our company	SKK/SKK Type-B/SKK DBG Type-B (SANYO FWS)	Application Version: After 1.04 Chip Data Version: After2.10	LC87F5NC8A

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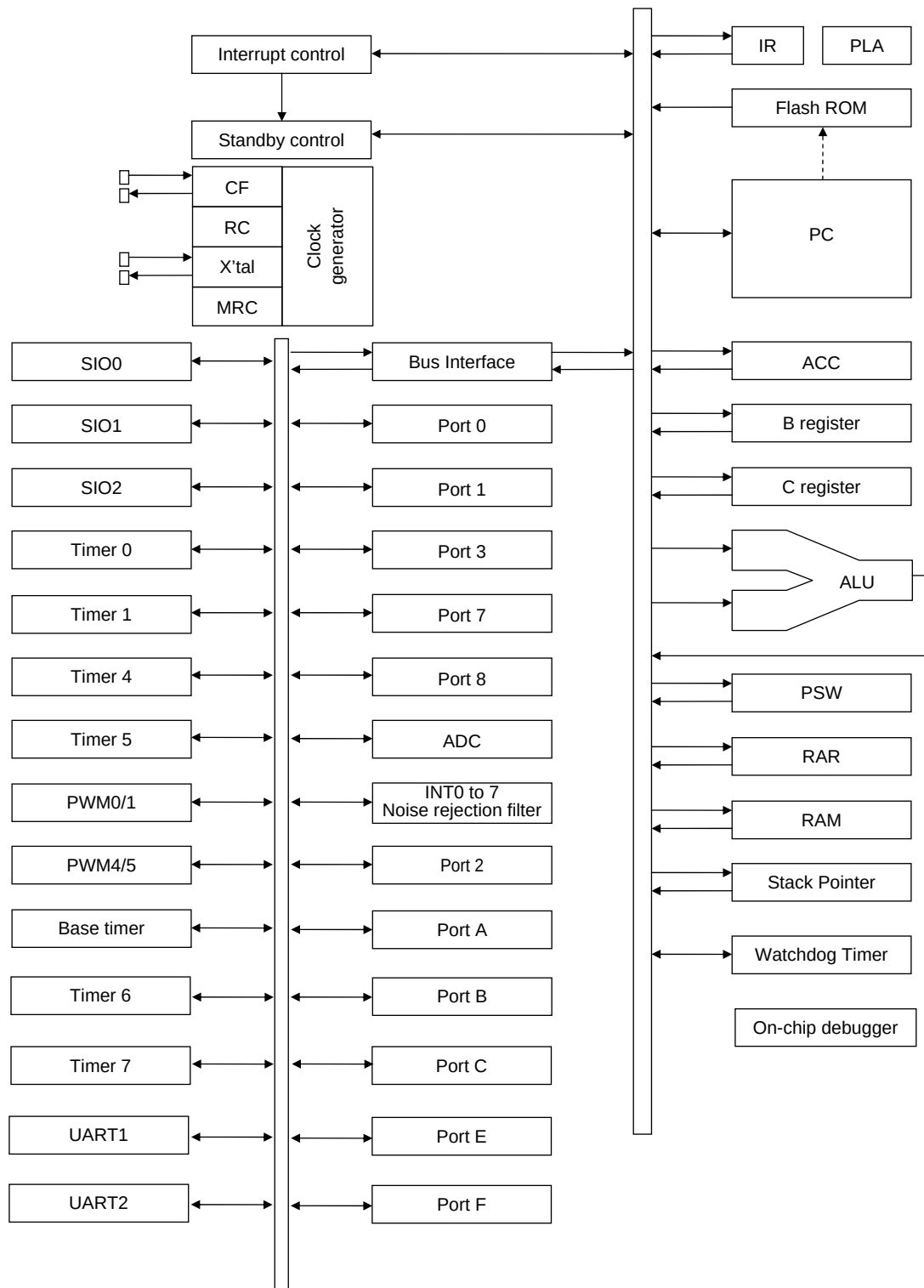
Pin Assignment



Top view

QIP100E(14×20) "Lead-free Type"

System Block Diagram



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Pin Description

Pin Name	I/O	Description	Option																														
V _{SS} 1, V _{SS} 2 V _{SS} 3, V _{SS} 4	-	- Power supply pin	No																														
V _{DD} 1, V _{DD} 2 V _{DD} 3, V _{DD} 4	-	+ Power supply pin	No																														
Port 0	I/O	• 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistor can be turned on and off in 4-bit units • HOLD release input • Port 0 interrupt input • Pin functions - P05: System clock output - P06: Timer 6 toggle output - P07: Timer 7 toggle output	Yes																														
P00 to P07																																	
Port 1	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions - P10: SIO0 data output - P11: SIO0 data input, bus I/O - P12: SIO0 clock I/O - P13: SIO1 data output - P14: SIO1 data input, bus I/O - P15: SIO1 clock I/O - P16: Timer 1 PWML output - P17: Timer 1 PWMH output, Beeper output	Yes																														
P10 to P17																																	
Port 2	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Other functions - P20: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT6 input/timer 0L capture 1 input - P21 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input - P24: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT7 input/timer 0H capture 1 input - P25 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input • Interrupt acknowledge type<table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising/ Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>		Rising	Falling	Rising/ Falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	INT6	enable	enable	enable	disable	disable	INT7	enable	enable	enable	disable	disable	Yes
			Rising	Falling	Rising/ Falling	H level	L level																										
INT4	enable	enable	enable	disable	disable																												
INT5	enable	enable	enable	disable	disable																												
INT6	enable	enable	enable	disable	disable																												
INT7	enable	enable	enable	disable	disable																												
P20 to P27																																	
Port 3	I/O	• 7-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions - P30: PWM4 output - P31: PWM5 output - P32: UART1 transmit - P33: UART1 receive - P34: UART2 transmit - P35: UART2 receive	Yes																														
P30 to P36																																	

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Pin Name	I/O	Description	Option																														
Port 7	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Other functions P70: INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer P71: INT1 input/HOLD release input/Timer 0H capture input P72: INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input P73: INT3 input with noise filter/Timer 0 event input/Timer 0H capture input • Interrupt acknowledge type <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising/ Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table> • AD converter input port: AN8 (P70), AN9 (P71)		Rising	Falling	Rising/ Falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
			Rising	Falling	Rising/ Falling	H level	L level																										
INT0			enable	enable	disable	enable	enable																										
INT1			enable	enable	disable	enable	enable																										
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												
P70 to P73																																	
Port 8	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Other functions P80 to P87: AD converter input port	No																														
P80 to P87																																	
Port A	I/O	• 6-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units	Yes																														
PA0 to PA5																																	
Port B	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units	Yes																														
PB0 to PB7																																	
Port C	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions DBGP0 to DBGP2 (PC5 to PC7): On-chip Debugger	Yes																														
PC0 to PC7																																	
Port E	I/O	• 8-bit I/O port • I/O specifiable in 2-bit units • Pull-up resistor can be turned on and off in 1-bit units	No																														
PE0 to PE7																																	
Port F	I/O	• 8-bit I/O port • I/O specifiable in 2-bit units • Pull-up resistor can be turned on and off in 1-bit units	No																														
PF0 to PF7																																	
SIO2 Port	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Shared functions: SI2P0: SIO2 data output SI2P1: SIO2 data input, bus input/output SI2P2: SIO2 clock input/output SI2P3: SIO2 clock output	No																														
SI2P0 to SI2P3																																	
PWM0, PWM1	O	• PWM0, PWM1 output port • General-purpose I/O available	No																														
$\overline{\text{RES}}$	I	Reset pin	No																														
XT1	I	• Input terminal for 32.768kHz X'tal oscillation • Shared functions: AN10: AD converter input port General-purpose input port Must be connected to V_{DD1} if not to be used.	No																														
XT2	I/O	• Output terminal for 32.768kHz X'tal oscillation • Shared functions: AN11: AD converter input port General-purpose I/O port Must be set for oscillation and kept open if not to be used.	No																														
CF1	I	Ceramic resonator input pin	No																														
CF2	O	Ceramic resonator output pin	No																														

Port Output Types

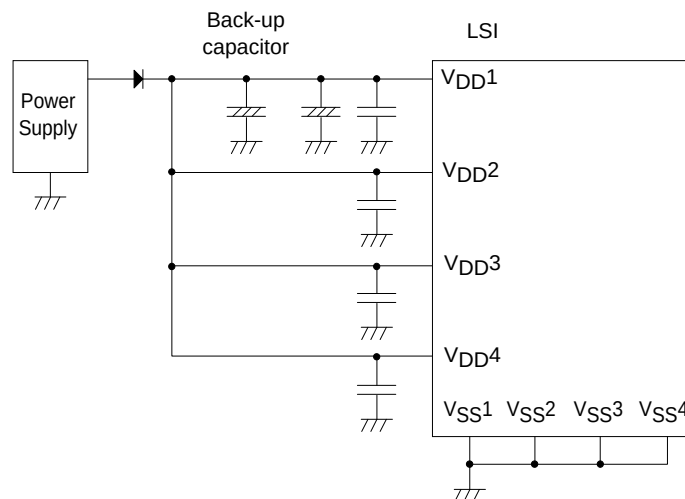
The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port	Options Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	N-channel open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P30 to P36	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	N-channel open drain	No
PA0 to PA5	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PB0 to PB7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PC0 to PC7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PE0 to PE7	-	No	CMOS	Programmable
PF0 to PF7	-	No	CMOS	Programmable
SI2P0, SI2P2 SI2P3	-	No	CMOS	No
SI2P1	-	No	CMOS (when selected as ordinary port) N-channel open drain (When SIO2 data is selected)	No
PWM0, PWM1	-	No	CMOS	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz quartz oscillator N-channel open drain (when in general-purpose No output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

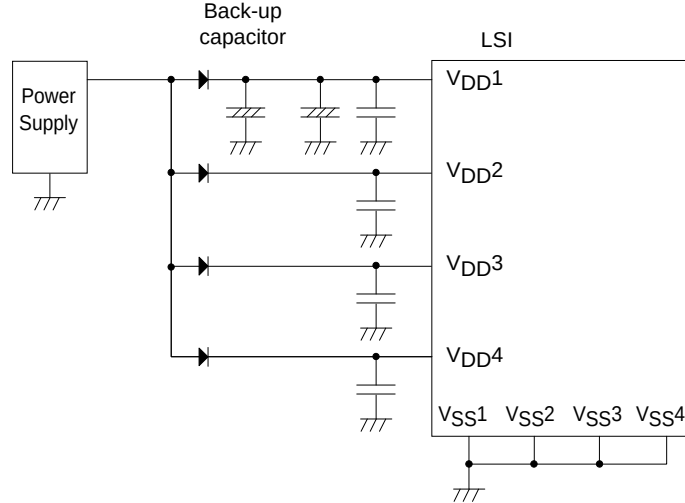
*1: Make the following connection to minimize the noise input to the V_{DD1} pin and prolong the backup time. Be sure to electrically short the V_{SS1}, V_{SS2}, V_{SS3} and V_{SS4} pins.

(Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



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(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.



Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	VDD[V]	Specification			
					min	typ	max	unit
Maximum Supply voltage	VDD max	VDD1, VDD2, VDD3, VDD4	VDD1=VDD2=VDD3=VDD4		-0.3		+6.5	V
Input voltage	VI(1)	XT1, CF1			-0.3		VDD+0.3	
Input/Output Voltage	VO(1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1, XT2			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin	-10			mA
		IOPH(2)	PWM0, PWM1	Per 1 application pin.	-20			
		IOPH(3)	P71 to P73	Per 1 application pin.	-5			
	Average output current (Note1-1)	IOM(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin	-7.5			
		IOM(2)	PWM0, PWM1	Per 1 application pin.	-10			
		IOM(3)	P71 to P73	Per 1 application pin.	-3			
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins	-10			
		ΣIOAH(2)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins	-25			
		ΣIOAH(3)	Port 0	Total of all applicable pins	-25			
		ΣIOAH(4)	Port 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins	-45			
		ΣIOAH(5)	Ports 2, 3, B	Total of all applicable pins	-25			
		ΣIOAH(6)	Ports A, C	Total of all applicable pins	-25			
		ΣIOAH(7)	Ports 2, 3, A, B, C	Total of all applicable pins	-45			
		ΣIOAH(8)	Port F	Total of all applicable pins	-25			
		ΣIOAH(9)	Ports 1, E	Total of all applicable pins	-25			
		ΣIOAH(10)	Ports 1, E, F	Total of all applicable pins	-45			

Note 1-1: Average output current is average of current in 100ms interval.

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Parameter		Symbol	Pins/Remarks	Conditions	V _{DD} [V]	Specification			
						min	typ	max	unit
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.				20	mA
		IOPL(2)	P00, P01	Per 1 application pin.				30	
		IOPL(3)	Ports 7, 8, XT2	Per 1 application pin.				10	
	Average output current (Note1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.				15	
		IOML(2)	P00, P01	Per 1 application pin.				20	
		IOML(3)	Ports 7, 8, XT2	Per 1 application pin.				7.5	
	Total output current	ΣIOAL(1)	Port 7, XT2	Total of all applicable pins				15	
		ΣIOAL(2)	Port 8	Total of all applicable pins				15	
		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins				20	
		ΣIOAL(4)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				45	
		ΣIOAL(5)	Port 0	Total of all applicable pins				45	
		ΣIOAL(6)	Port 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				80	
		ΣIOAL(7)	Ports 2, 3, B	Total of all applicable pins				45	
		ΣIOAL(8)	Ports A, C	Total of all applicable pins				45	
		ΣIOAL(9)	Ports 2, 3, A, B, C	Total of all applicable pins				80	
		ΣIOAL(10)	Port F	Total of all applicable pins				45	
		ΣIOAL(11)	Ports 1, E	Total of all applicable pins				45	
		ΣIOAL(12)	Ports 1, E, F	Total of all applicable pins				80	
Maximum power dissipation		Pd max	QIP100E(14×20)	Ta=-40 to +85°C				320	mW
Operating ambient temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: Average output current is average of current in 100ms interval.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Electrical Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				VDD[V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF V _{IN} =V _{DD} (including the off-leak current of the output Tr.)	2.2 to 5.5			1	μA
	I _{IH} (2)	XT1, XT2	Using as an input port V _{IN} =V _{DD}	2.2 to 5.5			1	
	I _{IH} (3)	CF1	V _{IN} =V _{DD}	2.2 to 5.5			15	
Low level input current	I _{IL} (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF V _{IN} =V _{SS} (including the off-leak current of the output Tr.)	2.2 to 5.5	-1			μA
	I _{IL} (2)	XT1, XT2	Using as an input port V _{IN} =V _{SS}	2.2 to 5.5	-1			
	I _{IL} (3)	CF1	V _{IN} =V _{SS}	2.2 to 5.5	-15			
High level output voltage	V _{OH} (1)	Ports 0, 1, 2, 3	I _{OH} =-1.0mA	4.5 to 5.5	V _{DD} -1			V
	V _{OH} (2)	Ports A, B, C, E, F SI2P0 to SI2P	I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (3)		I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (4)	Ports 71, 72, 73	I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (5)		I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (6)	PWM0, PWM1 P30, P31(PWM4, 5 output mode)	I _{OH} =-10mA	4.5 to 5.5	V _{DD} -1.5			
	V _{OH} (7)		I _{OH} =-1.6mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (8)		I _{OH} =-1.0mA	2.2 to 5.5	V _{DD} -0.4			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 2, 3	I _{OL} =10mA	4.5 to 5.5			1.5	V
	V _{OL} (2)	Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1,	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (3)		I _{OL} =1.0mA	2.2 to 5.5			0.4	
	V _{OL} (4)	P00, P01	I _{OL} =30mA	4.5 to 5.5			1.5	
	V _{OL} (5)		I _{OL} =5.0mA	3.0 to 5.5			0.4	
	V _{OL} (6)		I _{OL} =2.5mA	2.2 to 5.5			0.4	
	V _{OL} (7)	Ports 7, 8, XT2	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (8)		I _{OL} =1.0mA	2.2 to 5.5			0.4	
Pull-up resistation	Rpu(1)	Ports 0, 1, 2, 3	V _{OH} =0.9V _{DD}	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)	Port 7 Ports A, B, C, E, F		2.2 to 5.5	15	35	120	
Hysteresis voltage	VHYS	RES Ports 1, 2, 7 SI2P0 to SI2P3		2.2to 5.5		0.1V _{DD}		V
Pin capacitance	CP	All pins	- For pins other than that under test: V_{IN}=V_{SS} - f=1MHz - Ta=25°C	2.2 to 5.5		10		pF

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Serial I/O Characteristics at Ta = -40°C to +85°C, V_{SS1} = V_{SS2} = V_{SS3} = V_{SS4} = 0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pins /Remarks	Conditions	V _{DD} [V]	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		4					
			tSCKHA(1b)							
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected. • See Fig. 6.	2.2 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)		tSCKH(2) +2tCYC			tSCKH(2) +(10/3) tCYC	tCYC	
			tSCKHA(2b)		tSCKH(2) +2tCYC			tSCKH(2) +(16/3) tCYC		
Serial input	Data setup time		tsDI(1)	SIO(P11), SB0(P11)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.2 to 5.5	0.03			
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11),	• Continuous data transmission/reception mode • (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05	μs
			tdD0(2)		• Synchronous 8-bit mode. • (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdD0(3)		• (Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIO₀RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

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2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pins/ Remarks	Conditions	V _{DD} [V]	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	Tsck(3)	SCK1(P15)	• See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected. • See Fig. 6.	2.2 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time	tsDI(2)	SI1(P14), SB1(P14)	• Must be specified with respect to rising edge of SIOCLK • See fig. 6.	2.2 to 5.5	0.03				μs
	Data hold time	thDI(2)				0.03				
Serial output	Output delay time	tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.2 to 5.5				(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

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Pulse Input Conditions at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	VDD[V]	Specification			
					min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P20 to P23), INT5(P24 to P27), INT6(P20) INT7(P24)	- Interrupt source flag can be set. - Event inputs for timer 0 or 1 are enabled.	2.2 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1.	- Interrupt source flag can be set. - Event inputs for timer 0 are enabled.	2.2 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73)(The noise rejection clock is selected to 1/32.)	- Interrupt source flag can be set. - Event inputs for timer 0 are enabled.	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73)(The noise rejection clock is selected to 1/128.)	- Interrupt source flag can be set. - Event inputs for timer 0 are enabled.	2.2 to 5.5	256			
	tPIL(5)	RES	Reset acceptable.	2.2 to 5.5	200			μs

AD Converter Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	VDD[V]	Specification			
					min	typ	max	unit
Resolution	N	AN0(P80) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN7(P87), AN8(P70),	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD	AN9(P71), AN10(XT1), AN11(XT2), AN12(PA3), AN13(PA4), AN14(PA5)	AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	11.74 (tCYC= 0.367μs)		97.92 (tCYC= 3.06μs)	μs
				3.0 to 5.5	23.53 (tCYC= 0.735μs)		97.92 (tCYC= 3.06μs)	
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.245μs)		97.92 (tCYC= 1.53μs)	
				3.0 to 5.5	23.49 (tCYC= 0.367μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	3.0 to 5.5			1	μA
	IAINL		VAIN=VSS	3.0 to 5.5	-1			

Note 6-1: The quantization error (±1/2 LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the complete digital value corresponding to the analog input value is loaded in the required register.

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Consumption Current Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				VDD[V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	VDD1 =VDD2 =VDD3 =VDD4	- FmCF=12MHz ceramic oscillation mode - FmX'tal=32.768kHz by crystal oscillation mode - System clock set to 12MHz side - Internal RC oscillation stopped - frequency variable RC oscillation stopped 1/1 frequency division ratio.	4.5 to 5.5		9.5	20.5	mA
				2.8 to 4.5		5.5	14.8	
	IDDOP(2)		- FmCF=8MHz ceramic oscillation mode - FmX'tal=32.768kHz by crystal oscillation mode - System clock set to 8MHz side - Internal RC oscillation stopped - frequency variable RC oscillation stopped 1/1 frequency division ratio.	4.5 to 5.5		8	15.5	
				2.5 to 4.5		4	11	
	IDDOP(3)		- FmCF=4MHz ceramic oscillation mode - FmX'tal=32.768kHz by crystal oscillation mode - System clock set to 4MHz side - Internal RC oscillation stopped - frequency variable RC oscillation stopped 1/1 frequency division ratio.	4.5 to 5.5		2.8	6.6	
				2.2 to 4.5		1.5	4.2	
	IDDOP(4)		- FmCF=0Hz (oscillation stopped) - FmX'tal=32.768kHz by crystal oscillation mode - System clock set to internal RC oscillation - frequency variable RC oscillation stopped 1/2 frequency division ratio.	4.5 to 5.5		1	4.8	
				2.2 to 4.5		0.55	3.3	
	IDDOP(5)		- FmCF=0Hz (oscillation stopped) - FmX'tal=32.768kHz by crystal oscillation mode. - System clock set to 1MHz with frequency variable RC oscillation - Internal RC oscillation stopped 1/2 frequency division ratio.	4.5 to 5.5		1.3	5.7	
				2.2 to 4.5		0.7	4.6	
	IDDOP(6)		- FmCF=0Hz (oscillation stopped) - FmX'tal=32.768kHz by crystal oscillation mode. - System clock set to 32.768kHz side. - Internal RC oscillation stopped - frequency variable RC oscillation stopped 1/2 frequency division ratio.	4.5 to 5.5		40	120	μA
				2.2 to 4.5		20	77	
HALT mode consumption current (Note 7-1)	IDDHALT(1)	VDD1 =VDD2 =VDD3 =VDD4	- HALT mode - FmCF=12MHz ceramic oscillation mode - FmX'tal=32.768kHz by crystal oscillation mode - System clock set to 12MHz side - Internal RC oscillation stopped - frequency variable RC oscillation stopped 1/1 frequency division ratio.	4.5 to 5.5		3.6	8.3	mA
				2.8 to 5.5		2.1	4.4	
	IDDHALT(2)		- HALT mode - FmCF=8MHz ceramic oscillation mode - FmX'tal=32.768kHz by crystal oscillation mode - System clock set to 8MHz side - Internal RC oscillation stopped - frequency variable RC oscillation stopped 1/1 frequency division ratio.	4.5 to 5.5		2.7	5.8	
				2.5 to 4.5		1.4	3.1	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

Continued on next page.

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Continued from preceding page.

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(4)	V _{DD1} =V _{DD2} =V _{DD3} =V _{DD4}	• HALT mode • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		1.1	2.6	mA
	IDDHALT(5)		• System clock set to 4MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio.	2.2 to 4.5		0.57	1.5	
	IDDHALT(6)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		0.36	1.0	
	IDDHALT(7)		• System clock set to internal RC oscillation • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	2.2 to 4.5		0.19	0.8	
	IDDHALT(8)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode.	4.5 to 5.5		1.15	4.2	
	IDDHALT(9)		• System clock set to 1MHz with frequency variable RC oscillation • Internal RC oscillation stopped • 1/2 frequency division ratio.	2.2 to 4.5		0.57	3.0	
	IDDHALT(10)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode.	4.5 to 5.5		20	77	μA
	IDDHALT(11)		• System clock set to 32.768kHz side. • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	2.2 to 4.5		6	70	
HOLD mode consumption current	IDDHOLD(1)	V _{DD1}	• HOLD mode	4.5 to 5.5		0.04	20	
	IDDHOLD(2)		• CF1=V _{DD} or open (External clock mode)	2.2 to 4.5		0.02	15	
Timer HOLD mode consumption current	IDDHOLD(3)		• Timer HOLD mode	4.5 to 5.5		17	70	
	IDDHOLD(4)		• FmX'tal=32.768kHz by crystal oscillation mode	2.2 to 4.5		4	55	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

F-ROM Programming Characteristics at Ta = +10°C to +55°C, V_{SS1} = V_{SS2} = V_{SS3} = V_{SS4} = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	V _{DD1}	• Without CPU current	2.70 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing	2.7 to 5.5		20	30	ms
	tFW(2)		• programming	2.7 to 5.5		40	60	μs

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	470	2.5 to 5.5	0.03	0.5	Internal C1,C2
10MHz		CSTCE10M0G52-R0	(10)	(10)	Open	680	2.4 to 5.5	0.03	0.5	Internal C1,C2
		CSTLS10M0G53-B0	(15)	(15)	Open	680	2.5 to 5.5	0.03	0.5	Internal C1,C2
8MHz		CSTCE8M00G52-R0	(10)	(10)	Open	1k	2.3 to 5.5	0.03	0.5	Internal C1,C2
		CSTLS8M00G53-B0	(15)	(15)	Open	1k	2.5 to 5.5	0.03	0.5	Internal C1,C2
4MHz		CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.03	0.5	Internal C1,C2
		CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.03	0.5	Internal C1,C2

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Fig. 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	Open	560k	2.2 to 5.5	1.5	3.0	Applicable CL value=12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure. 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

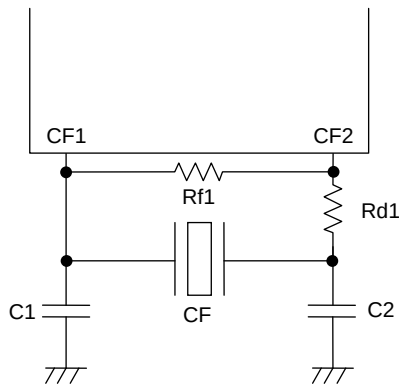


Figure 1 Ceramic Oscillator Circuit

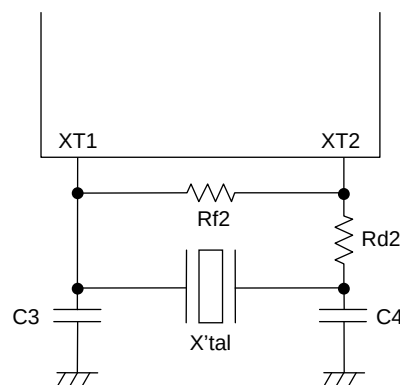


Figure 2 Crystal Oscillator Circuit

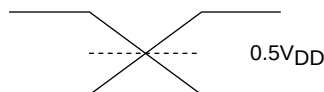
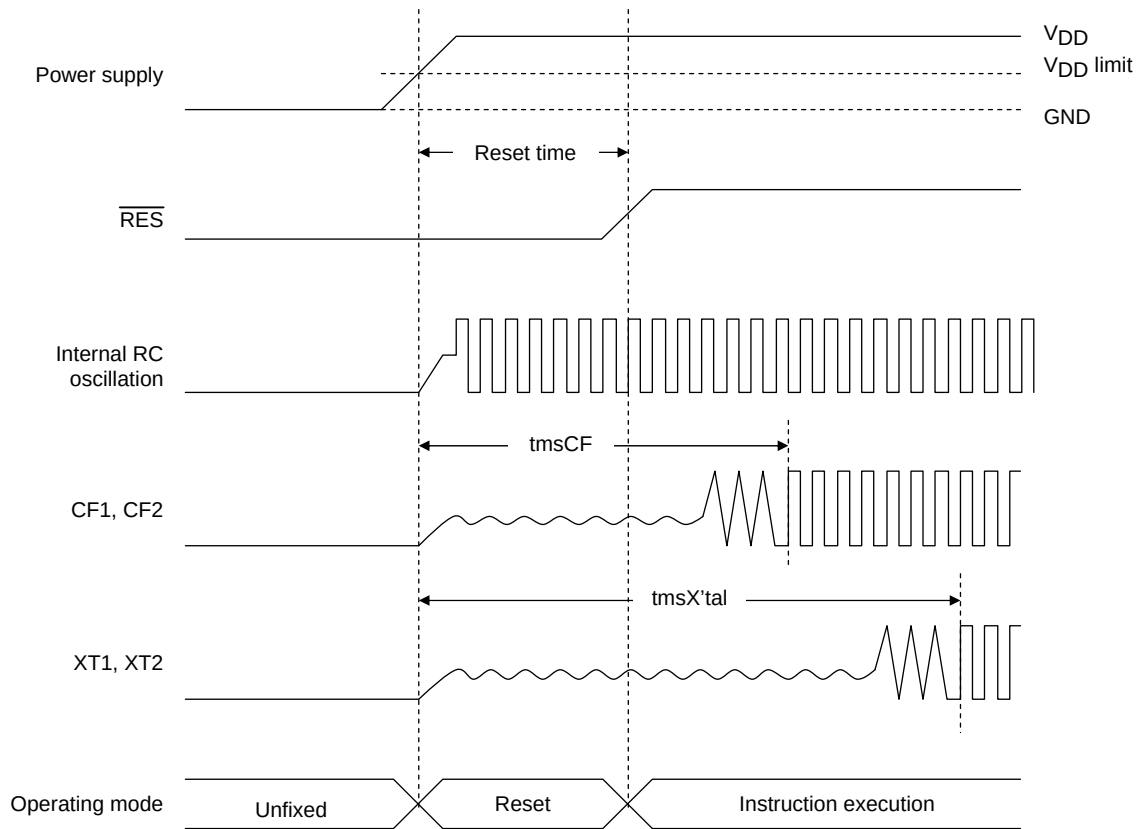
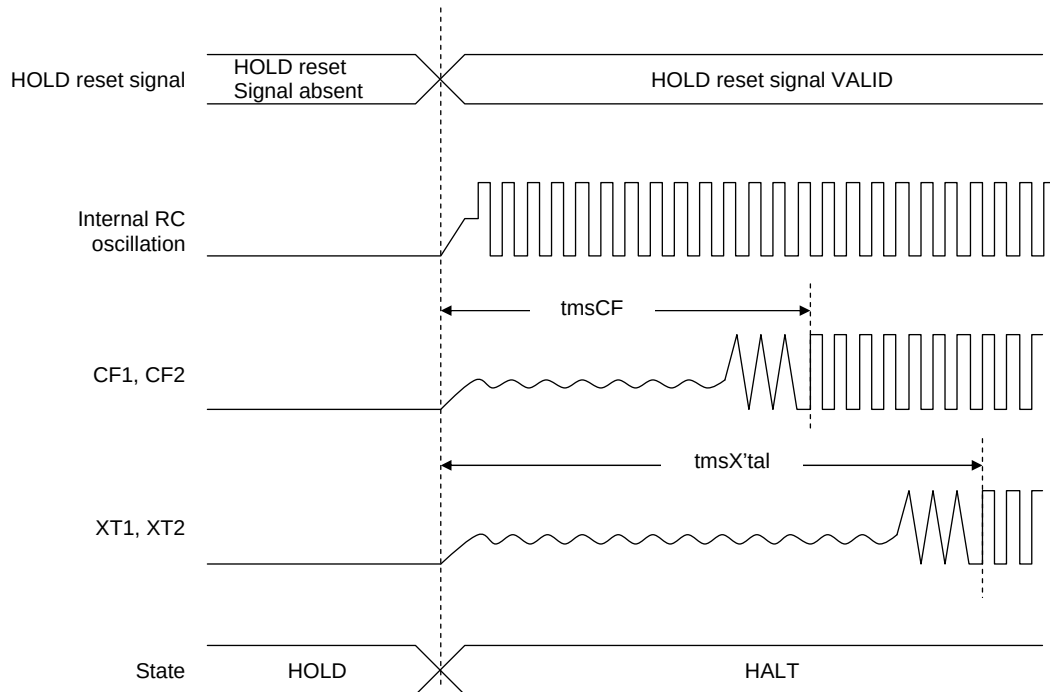


Figure 3 AC Timing Measurement Point

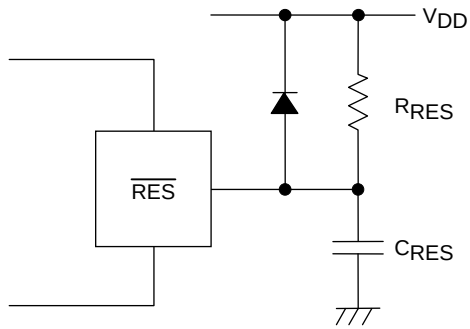


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note:
Select C_{RES} and R_{RES} value to assure that at least $200\mu\text{s}$ reset time is generated after the V_{DD} becomes higher than the minimum operating voltage..

Figure 5 Reset Circuit

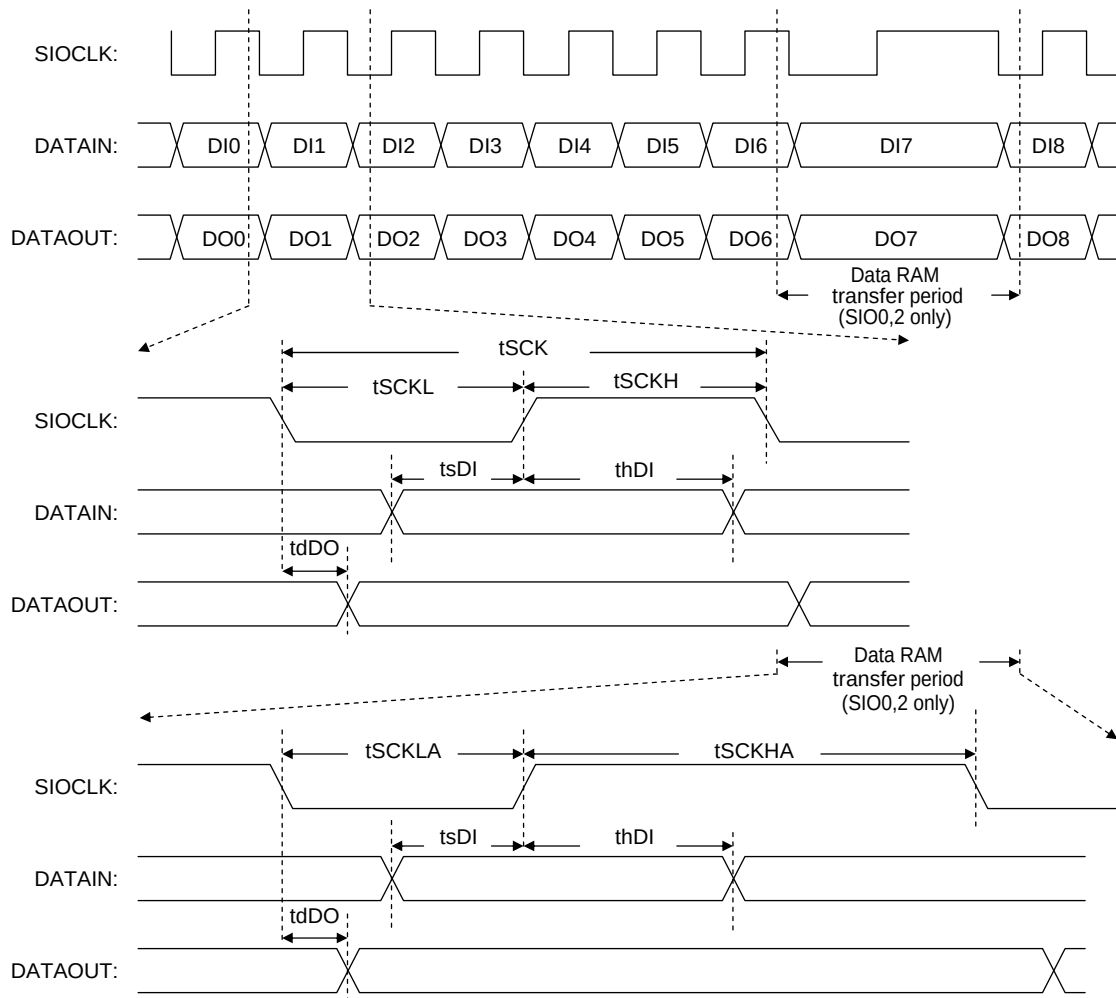


Figure 6 Serial I/O Waveforms

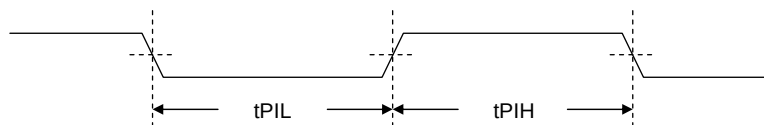


Figure 7 Pulse Input Timing Signal Waveform

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