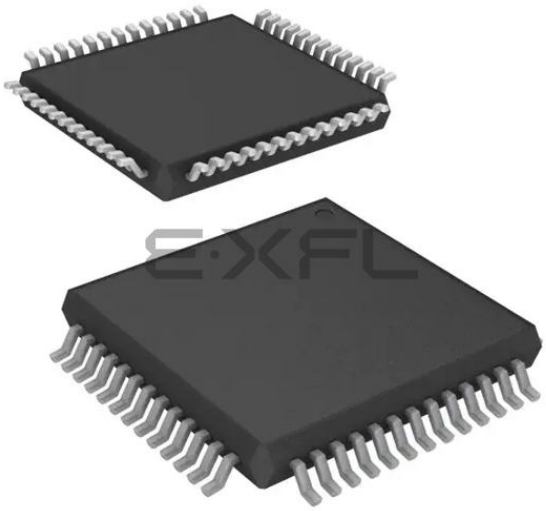
Renesas Electronics America Inc - R5F2135AMNFP#X4 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	47
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2135amnfp-x4

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/35M Group.

Table 1.1 Specifications for R8C/35M Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.3 Product List for R8C/35M Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 47, selectable pull-up resistor • High current drive ports: 47
Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 9 ($\overline{\text{INT}}$ × 5, Key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 33 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

1.2 Product List

Table 1.3 lists Product List for R8C/35M Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/35M Group.

Table 1.3 Product List for R8C/35M Group **Current of Jun 2011**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21354MNFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0052JA-A	N version
R5F21355MNFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0052JA-A	
R5F21356MNFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0052JA-A	
R5F21357MNFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0052JA-A	
R5F21358MNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0052JA-A	
R5F2135AMNFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0052JA-A	
R5F2135CMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	
R5F21354MDFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0052JA-A	D version
R5F21355MDFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0052JA-A	
R5F21356MDFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0052JA-A	
R5F21357MDFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0052JA-A	
R5F21358MDFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0052JA-A	
R5F2135AMDFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0052JA-A	
R5F2135CMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	

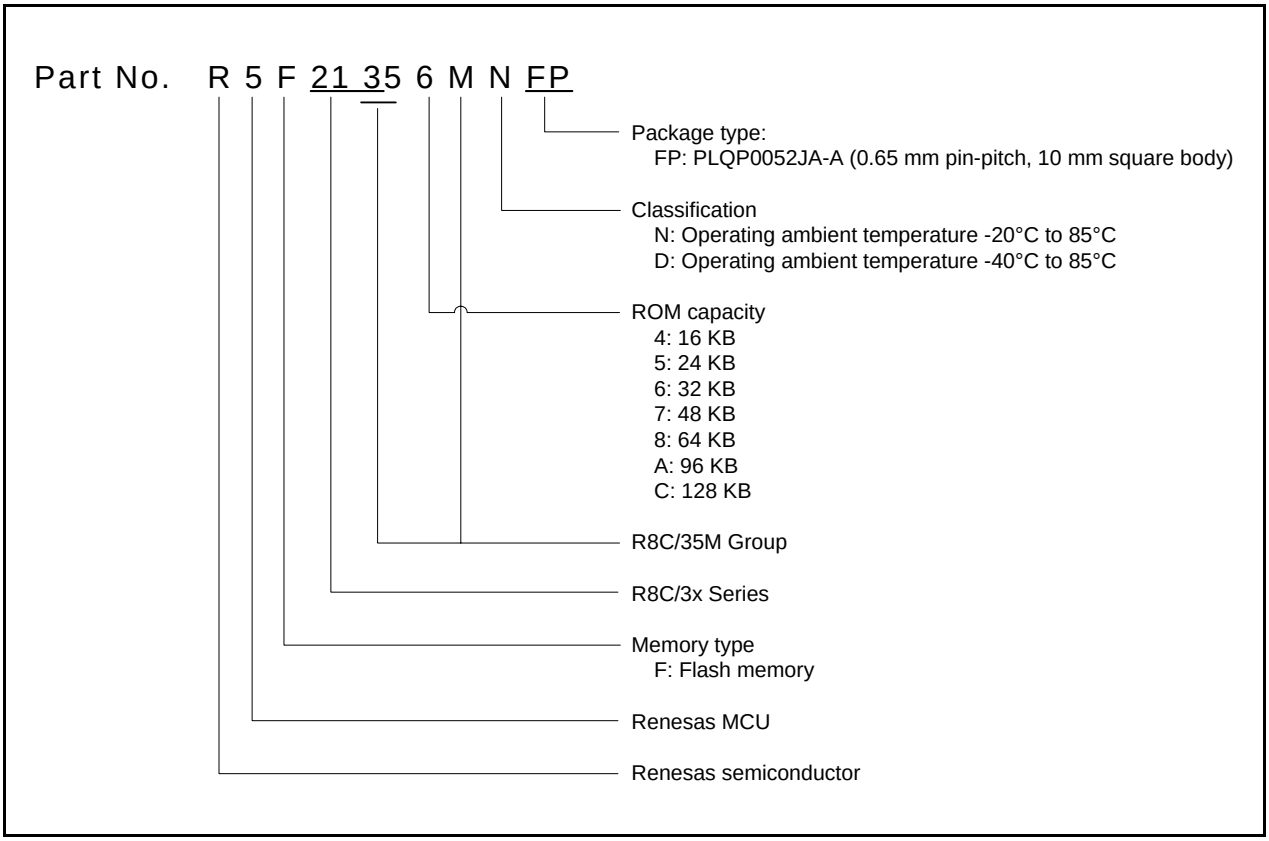


Figure 1.1 Part Number, Memory Size, and Package of R8C/35M Group

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

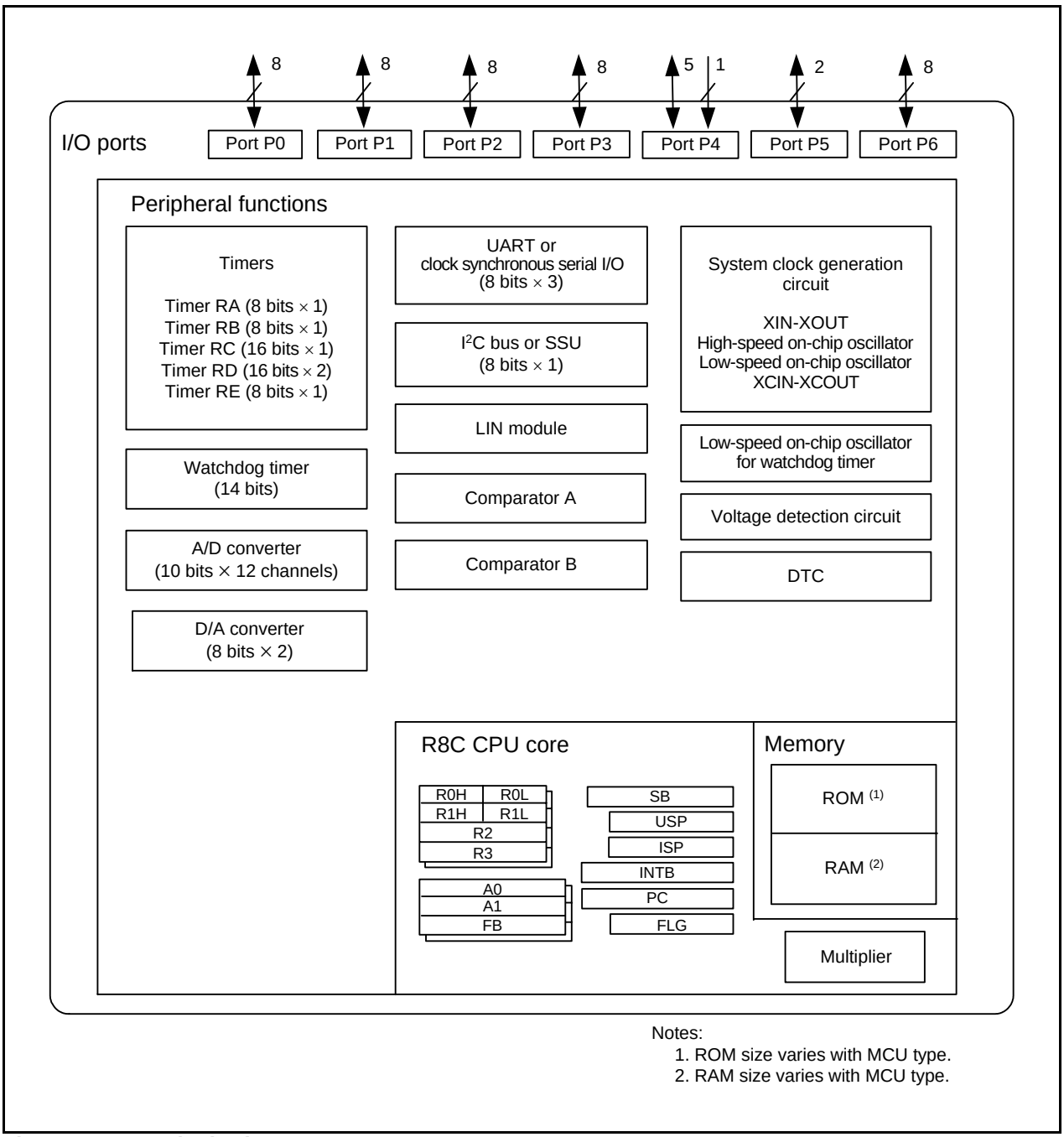
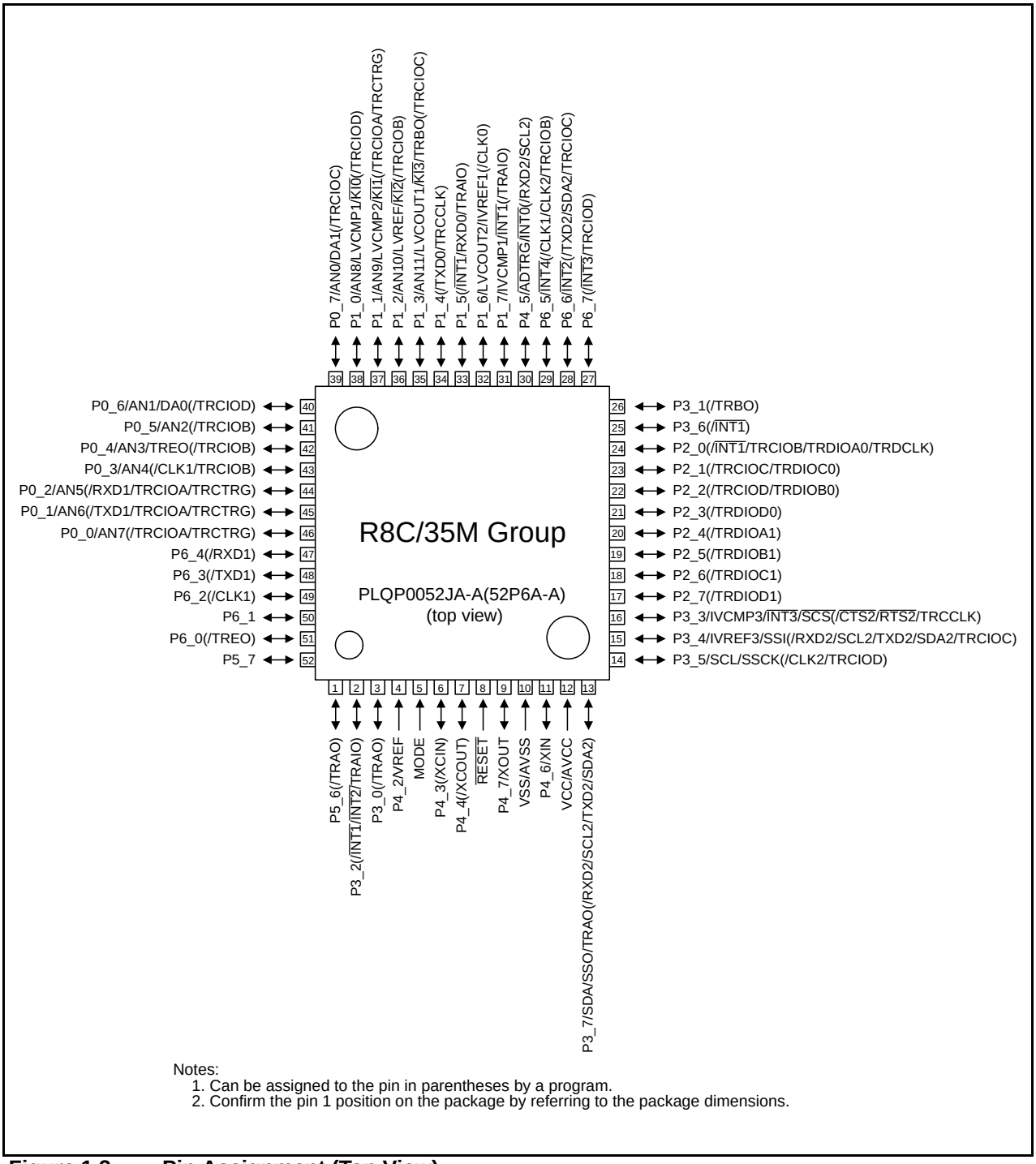


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows the Pin Assignment (Top View). Tables 1.4 and 1.5 outline the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparator A, Comparator B
1		P5_6		(TRAO)				
2		P3_2	($\overline{INT1}$/$\overline{INT2}$)	(TRAIO)				
3		P3_0		(TRAO)				
4		P4_2						VREF
5	MODE							
6	(XCIN)	P4_3						
7	(XCOUT)	P4_4						
8	$\overline{RESET}$							
9	XOUT	P4_7						
10	VSS/AVSS							
11	XIN	P4_6						
12	VCC/AVCC							
13		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
14		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
15		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
16		P3_3	$\overline{INT3}$	(TRCCLK)	($\overline{CTS2}$/$\overline{RTS2}$)	$\overline{SCS}$		IVCMP3
17		P2_7		(TRDIOD1)				
18		P2_6		(TRDIOC1)				
19		P2_5		(TRDIOB1)				
20		P2_4		(TRDIOA1)				
21		P2_3		(TRDIOD0)				
22		P2_2		(TRCIOD/ TRDIOB0)				
23		P2_1		(TRCIOC/ TRDIOC0)				
24		P2_0	($\overline{INT1}$)	(TRCIOB/ TRDIOA0/ TRDCLK)				
25		P3_6	($\overline{INT1}$)					
26		P3_1		(TRBO)				
27		P6_7	($\overline{INT3}$)	(TRCIOD)				
28		P6_6	$\overline{INT2}$	(TRCIOC)	(TXD2/SDA2)			
29		P6_5	$\overline{INT4}$	(TRCIOB)	(CLK1/CLK2)			
30		P4_5	$\overline{INT0}$		(RXD2/SCL2)			$\overline{ADTRG}$
31		P1_7	$\overline{INT1}$	(TRAIO)				IVCMP1
32		P1_6			(CLK0)			LVCOUT2/IVREF1
33		P1_5	($\overline{INT1}$)	(TRAIO)	(RXD0)			
34		P1_4		(TRCCLK)	(TXD0)			
35		P1_3	$\overline{KI3}$	TRBO (/TRCIOC)				AN11/LVCOUT1

Note:
1. Can be assigned to the pin in parentheses by a program.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version) / –40 to 85 (D version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
I_{Vref}	V_{ref} current		V_{CC} = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
V_{ref}	Reference voltage				2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.11 Voltage Detection 2 Circuit Electrical Characteristics

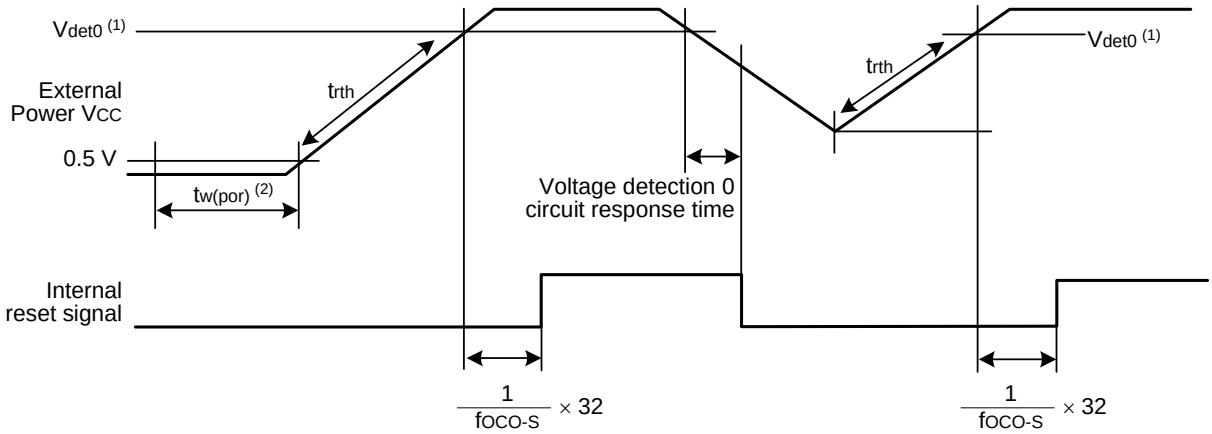
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0 (2)	At the falling of V_{CC}	3.70	4.00	4.30	V
	Voltage detection level Vdet2_EXT (2)	At the falling of LVCMP2	1.20	1.34	1.48	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		–	0.10	–	V
–	Voltage detection 2 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
3. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.12 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	–	50,000	mV/ms

Notes:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

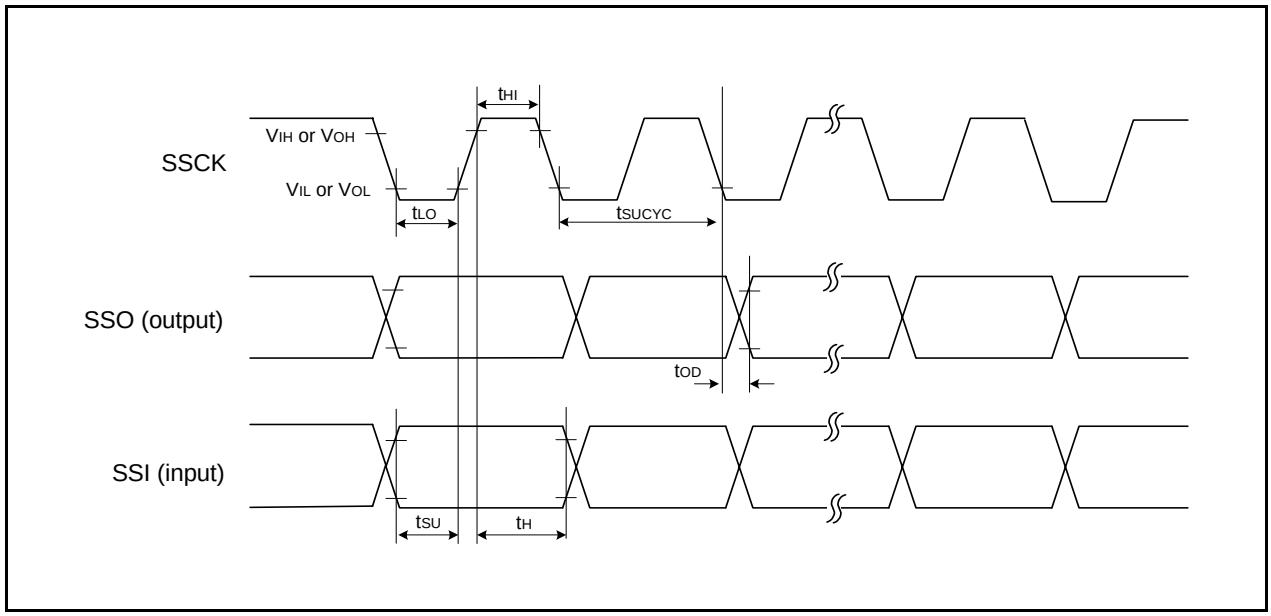


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.18 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity Low V_{CC} = 5 V	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	V_{CC} = 5 V	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity Low V_{CC} = 5 V	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	V_{CC} = 5 V	I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V_{CC} = 5.0 V		0.1	1.2	–	V
		$\overline{RESET}$	V_{CC} = 5.0 V		0.1	1.2	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5.0 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V		–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			–	0.3	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	8	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.24 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 5 mA	–	–	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	–	–	0.5	V
		XOUT		I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V_{CC} = 3.0 V		0.1	0.4	–	V
		$\overline{RESET}$	V_{CC} = 3.0 V		0.1	0.5	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3.0 V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3.0 V		–	–	–4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			–	0.3	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	8	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 2.7 V ≤ V_{CC} < 4.2 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Timing Requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C)

Table 5.26 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

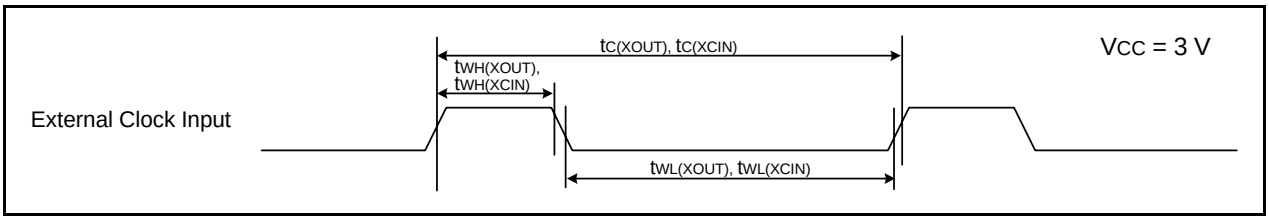


Figure 5.12 External Clock Input Timing Diagram when VCC = 3 V

Table 5.27 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

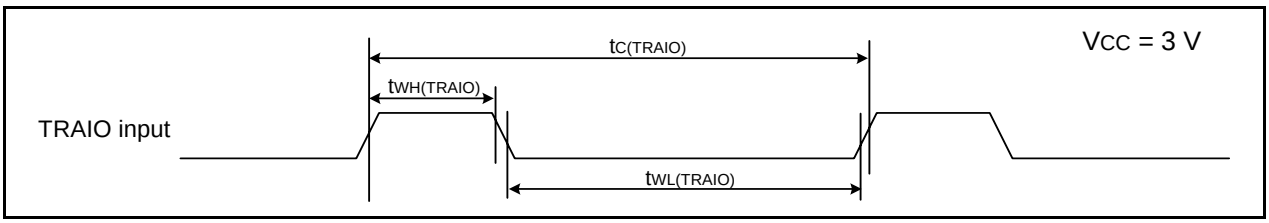


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.30 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –2 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	–	–	0.5	V
		XOUT		I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, $\overline{TRCCLK}$, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V_{CC} = 2.2 V		0.05	0.2	–	V
		$\overline{RESET}$	V_{CC} = 2.2 V		0.05	0.20	–	V
I_{IH}	Input “H” current		VI = 2.2 V, V_{CC} = 2.2 V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 2.2 V		–	–	–4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			–	0.3	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	8	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 1.8 V ≤ V_{CC} < 2.7 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Timing Requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.32 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

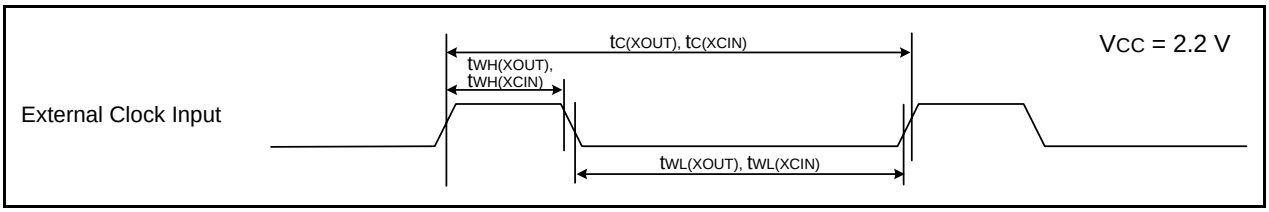


Figure 5.16 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.33 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

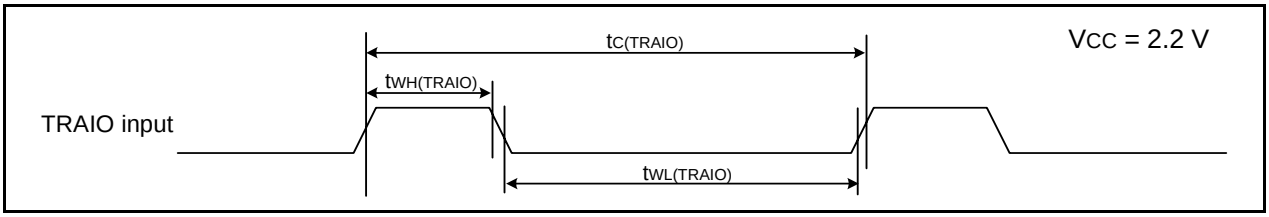


Figure 5.17 TRAIO Input Timing Diagram when Vcc = 2.2 V

REVISION HISTORY	R8C/35M Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Sep 28, 2010	–	First Edition issued
0.20	Feb 15, 2011	35	Table 5.11 revised, Note 2 added
		36	Table 5.13 and Table 5.14 revised
		42	Table 5.18 revised
		50	Table 5.30 revised
1.00	Jun 20, 2011	All pages	“Preliminary”, “Under development” deleted
		4	Table 1.3 “(D): Under development”, “(P): Under planning” deleted
		28	Table 5.2 revised
		35	Table 5.11 revised
		36	Table 5.13 revised
		43	Table 5.19 revised
		44	Table 5.20 revised
		45	Table 5.22 Note 1 revised
		47	Table 5.25 revised
		48	Table 5.26 revised
		49	Table 5.28 Note 1 revised
		51	Table 5.31 revised
		52	Table 5.32 revised
		53	Table 5.34 Note 1 revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.