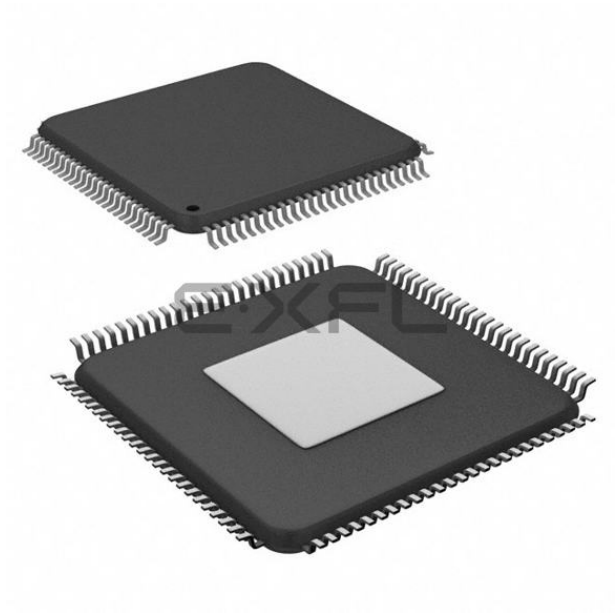
# Infineon Technologies - SAF-XE164F-48F66L AC Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 66MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 75 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 34K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-100-3 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164f-48f66l-ac |

# 1 Summary of Features

For a quick overview and easy reference, the features of the XE164 are summarized here.

- High-performance CPU with five-stage pipeline
  - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
- Interrupt system with 16 priority levels for up to 83 sources
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- On-chip memory modules
  - 1 Kbyte on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 64 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 768 Kbytes on-chip program memory (Flash memory)
- On-Chip Peripheral Modules
  - Two Synchronizable A/D Converters with up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check)
  - 16-channel general purpose capture/compare unit (CAPCOM2)
  - Up to three capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers

2) Specific inormation about the on-chip Flash memory in **Table 2**.
3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM (12 Kbytes for devices with 192 Kbytes of Flash).
4) Specific information about the available channels in **Table 3**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

# 2 General Device Information

The XE164 series of real time signal controllers is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

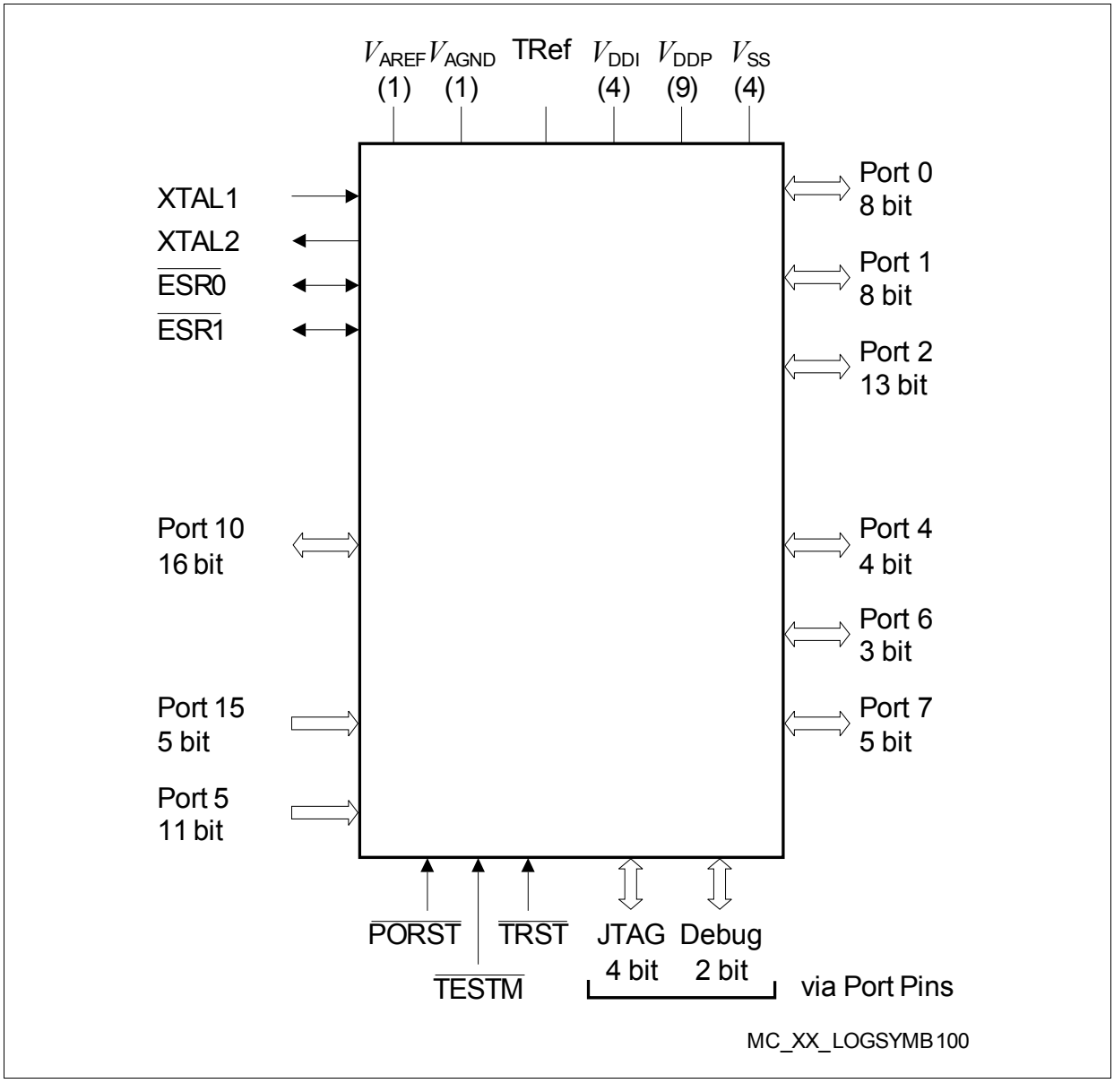


**Figure 1 Logic Symbol**

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 43 | P2.3 | O0 / I | St/B | **Bit 3 of Port 2, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CC2_16 | O3 / I | St/B | **CAPCOM2 CC16IO Capture Inp./ Compare Out.** |
| | A16 | OH | St/B | **External Bus Interface Address Line 16** |
| | ESR2_0 | I | St/B | **ESR2 Trigger Input 0** |
| | U0C0_DX0E | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX0D | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | RxDC0A | I | St/B | **CAN Node 0 Receive Data Input** |
| 44 | P4.1 | O0 / I | St/B | **Bit 1 of Port 4, General Purpose Input/Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CC2_25 | O3 / I | St/B | **CAPCOM2 CC25IO Capture Inp./ Compare Out.** |
| | $\overline{CS1}$ | OH | St/B | **External Bus Interface Chip Select 1 Output** |
| 45 | P2.4 | O0 / I | St/B | **Bit 4 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CC2_17 | O3 / I | St/B | **CAPCOM2 CC17IO Capture Inp./ Compare Out.** |
| | A17 | OH | St/B | **External Bus Interface Address Line 17** |
| | ESR1_0 | I | St/B | **ESR1 Trigger Input 0** |
| | U0C0_DX0F | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | RxDC1A | I | St/B | **CAN Node 1 Receive Data Input** |
| 46 | P2.5 | O0 / I | St/B | **Bit 5 of Port 2, General Purpose Input/Output** |
| | U0C0_ SCLKOUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CC2_18 | O3 / I | St/B | **CAPCOM2 CC18IO Capture Inp./ Compare Out.** |
| | A18 | OH | St/B | **External Bus Interface Address Line 18** |
| | U0C0_DX1D | I | St/B | **USIC0 Channel 0 Shift Clock Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 79 | P10.8 | O0 / I | St/B | **Bit 8 of Port 10, General Purpose Input/Output** |
| | U0C0_ MCLKOUT | O1 | St/B | **USIC0 Channel 0 Master Clock Output** |
| | U0C1_ SELO0 | O2 | St/B | **USIC0 Channel 1 Select/Control 0 Output** |
| | AD8 | OH / I | St/B | **External Bus Interface Address/Data Line 8** |
| | CCU60_ CCPOS1A | I | St/B | **CCU60 Position Input 1** |
| | U0C0_DX1C | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | $\overline{\text{BRKIN\_B}}$ | I | St/B | **OCDS Break Signal Input** |
| 80 | P10.9 | O0 / I | St/B | **Bit 9 of Port 10, General Purpose Input/Output** |
| | U0C0_ SELO4 | O1 | St/B | **USIC0 Channel 0 Select/Control 4 Output** |
| | U0C1_ MCLKOUT | O2 | St/B | **USIC0 Channel 1 Master Clock Output** |
| | AD9 | OH / I | St/B | **External Bus Interface Address/Data Line 9** |
| | CCU60_ CCPOS2A | I | St/B | **CCU60 Position Input 2** |
| | TCK_B | I | St/B | **JTAG Clock Input** |
| 81 | P1.1 | O0 / I | St/B | **Bit 1 of Port 1, General Purpose Input/Output** |
| | CCU62_ COUT62 | O1 | St/B | **CCU62 Channel 2 Output** |
| | U1C0_ SELO5 | O2 | St/B | **USIC1 Channel 0 Select/Control 5 Output** |
| | U2C1_DOUT | O3 | St/B | **USIC2 Channel 1 Shift Data Output** |
| | A9 | OH | St/B | **External Bus Interface Address Line 9** |
| | ESR2_3 | I | St/B | **ESR2 Trigger Input 3** |
| | EX1BINA | I | St/B | **External Interrupt Trigger Input** |
| | U2C1_DX0C | I | St/B | **USIC2 Channel 1 Shift Data Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 82 | P10.10 | O0 / I | St/B | **Bit 10 of Port 10, General Purpose Input/Output** |
| | U0C0_ SELO0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | CCU60_ COUT63 | O2 | St/B | **CCU60 Channel 3 Output** |
| | AD10 | OH / I | St/B | **External Bus Interface Address/Data Line 10** |
| | U0C0_DX2C | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | TDI_B | I | St/B | **JTAG Test Data Input** |
| | U0C1_DX1A | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| 83 | P10.11 | O0 / I | St/B | **Bit 11 of Port 10, General Purpose Input/Output** |
| | U1C0_ SCLKOUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | $\overline{\text{BRKOUT}}$ | O2 | St/B | **OCDS Break Signal Output** |
| | AD11 | OH / I | St/B | **External Bus Interface Address/Data Line 11** |
| | U1C0_DX1D | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | RxDC2B | I | St/B | **CAN Node 2 Receive Data Input** |
| | TMS_B | I | St/B | **JTAG Test Mode Selection Input** |
| 84 | P1.2 | O0 / I | St/B | **Bit 2 of Port 1, General Purpose Input/Output** |
| | CCU62_ CC62 | O1 / I | St/B | **CCU62 Channel 2 Input/Output** |
| | U1C0_ SELO6 | O2 | St/B | **USIC1 Channel 0 Select/Control 6 Output** |
| | U2C1_ SCLKOUT | O3 | St/B | **USIC2 Channel 1 Shift Clock Output** |
| | A10 | OH | St/B | **External Bus Interface Address Line 10** |
| | ESR1_4 | I | St/B | **ESR1 Trigger Input 4** |
| | CCU61_ T12HRB | I | St/B | **External Run Control Input for T12 of CCU61** |
| | EX2AINA | I | St/B | **External Interrupt Trigger Input** |
| | U2C1_DX0D | I | St/B | **USIC2 Channel 1 Shift Data Input** |
| | U2C1_DX1C | I | St/B | **USIC2 Channel 1 Shift Clock Input** |

# 3 Functional Description

The architecture of the XE164 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE164.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE164.

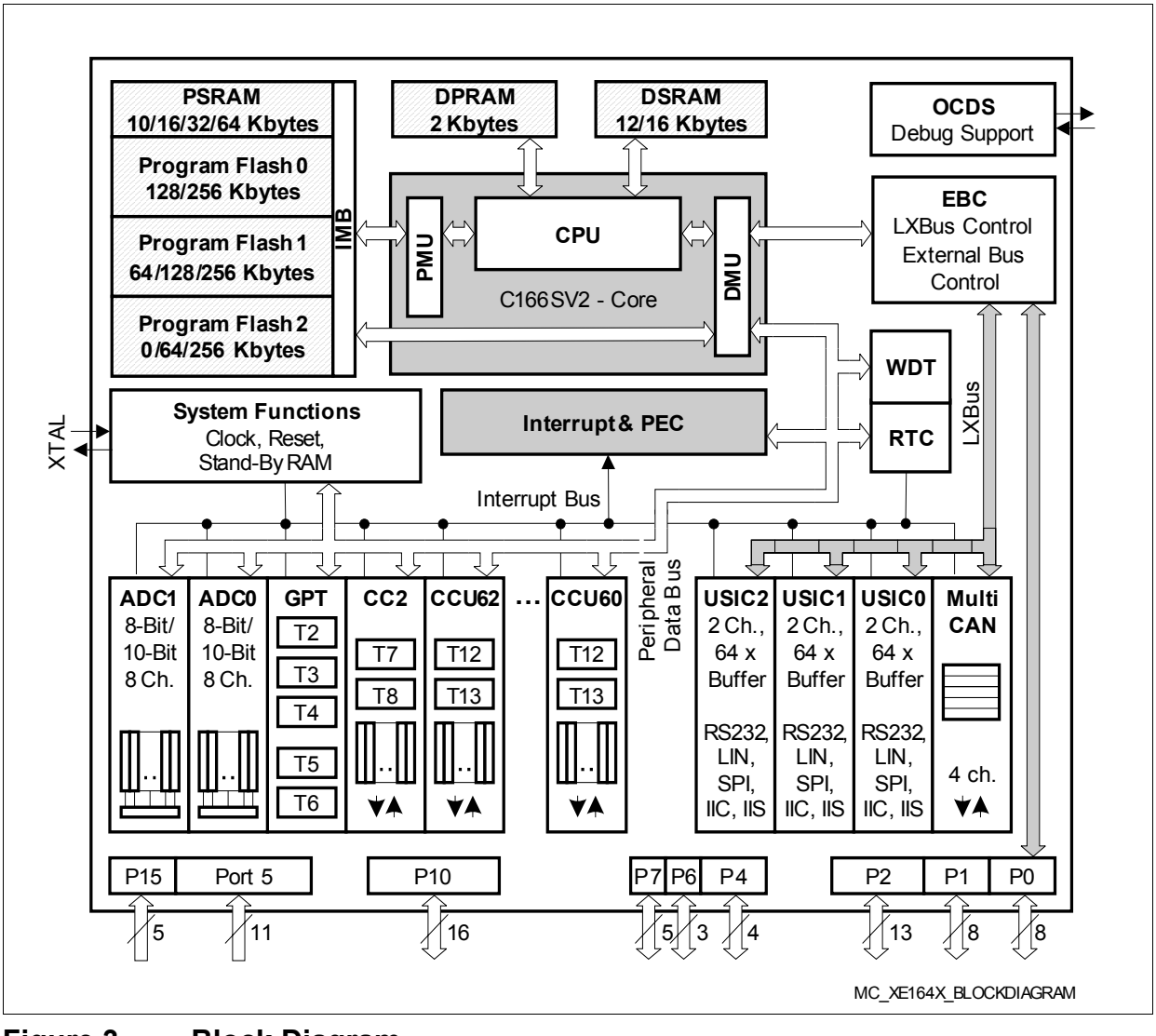


**Figure 3 Block Diagram**

**Table 6 XE164 Interrupt Nodes** (cont'd)

| Source of Interrupt or PEC Service Request | Control Register | Vector Location[1)] | Trap Number |
|---|---|---|---|
| USIC2 Cannel 1, Request 0 | U2C1_0IC | xx'017C$_H$ | 5F$_H$ / 95$_D$ |
| USIC2 Cannel 1, Request 1 | U2C1_1IC | xx'0180$_H$ | 60$_H$ / 96$_D$ |
| USIC2 Cannel 1, Request 2 | U2C1_2IC | xx'0184$_H$ | 61$_H$ / 97$_D$ |
| Unassigned node | – | xx'0188$_H$ | 62$_H$ / 98$_D$ |
| Unassigned node | – | xx'018C$_H$ | 63$_H$ / 99$_D$ |
| Unassigned node | – | xx'0190$_H$ | 64$_H$ / 100$_D$ |
| Unassigned node | – | xx'0194$_H$ | 65$_H$ / 101$_D$ |
| Unassigned node | – | xx'0198$_H$ | 66$_H$ / 102$_D$ |
| Unassigned node | – | xx'019C$_H$ | 67$_H$ / 103$_D$ |
| Unassigned node | – | xx'01A0$_H$ | 68$_H$ / 104$_D$ |
| Unassigned node | – | xx'01A4$_H$ | 69$_H$ / 105$_D$ |
| Unassigned node | – | xx'01A8$_H$ | 6A$_H$ / 106$_D$ |
| SCU Request 1 | SCU_1IC | xx'01AC$_H$ | 6B$_H$ / 107$_D$ |
| SCU Request 0 | SCU_0IC | xx'01B0$_H$ | 6C$_H$ / 108$_D$ |
| Program Flash Modules | PFM_IC | xx'01B4$_H$ | 6D$_H$ / 109$_D$ |
| RTC | RTC_IC | xx'01B8$_H$ | 6E$_H$ / 110$_D$ |
| End of PEC Subchannel | EOPIC | xx'01BC$_H$ | 6F$_H$ / 111$_D$ |

1) Register VECSEG defines the segment where the vector table is located.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting with a distance of 4 (two words) between two vectors.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD[1)]). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE164 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

1) Exception: T5EUD is not connected to a pin.

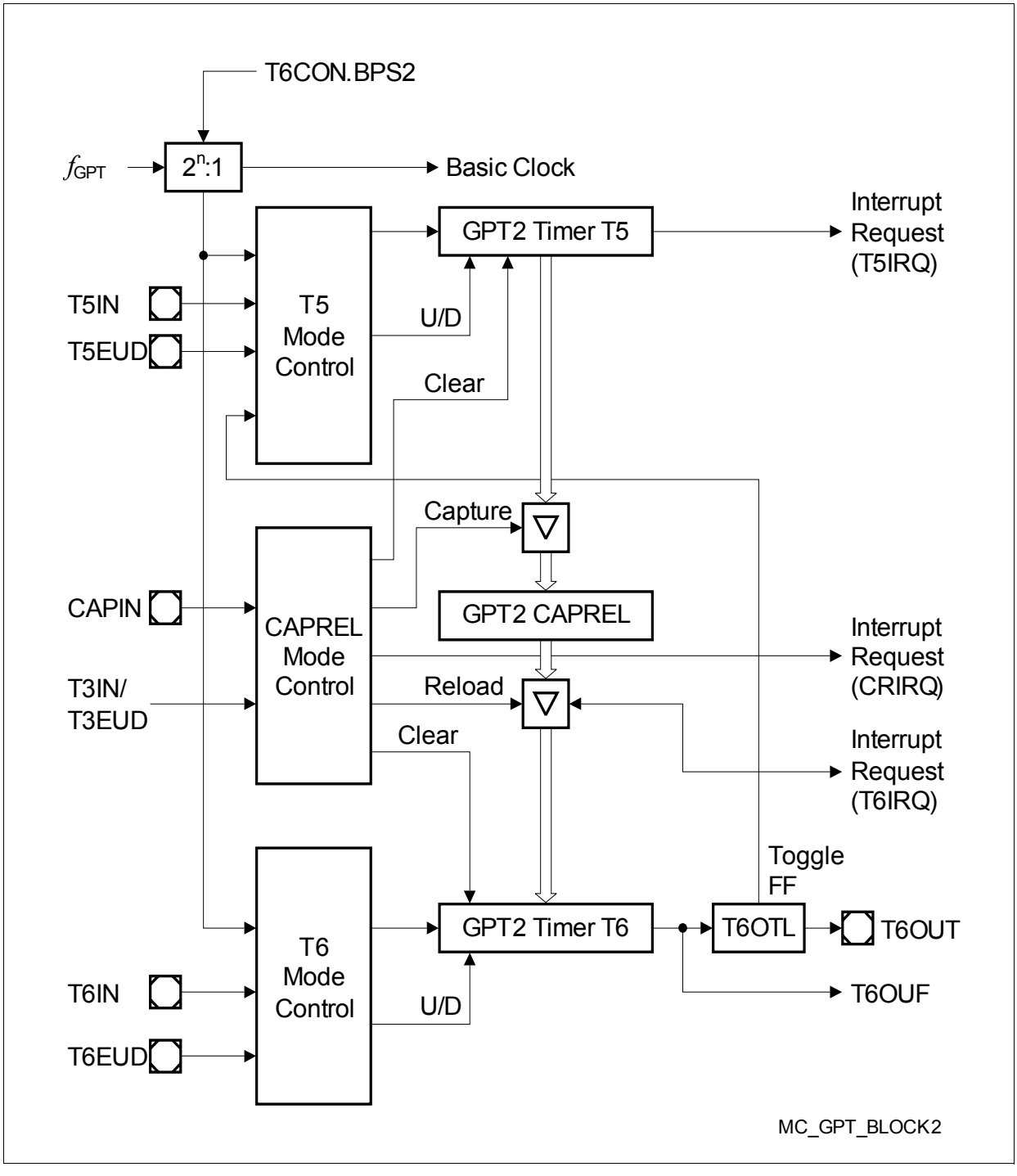


**Figure 8 Block Diagram of GPT2**

### Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - maximum baud rate: $f_{SYS}$ / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - maximum baud rate: $f_{SYS}$ / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
  - maximum baud rate in slave mode: $f_{SYS}$
  - maximum baud rate in master mode: $f_{SYS}$ / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - maximum baud rate: $f_{SYS}$ / 2 for transmitter, $f_{SYS}$ for receiver

*Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).*

## 3.15 Parallel Ports

The XE164 provides up to 75 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 9**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

**Table 9 Summary of the XE164's Parallel Ports**

| Port | Width | Alternate Functions |
|---|---|---|
| Port 0 | 8 | Address lines,<br>Serial interface lines of USIC1, CAN0, and CAN1,<br>Input/Output lines for CCU61 |
| Port 1 | 8 | Address lines,<br>Serial interface lines of USIC1 and USIC2,<br>Input/Output lines for CCU62,<br>OCDS control, interrupts |
| Port 2 | 13 | Address and/or data lines, bus control,<br>Serial interface lines of USIC0, CAN0, and CAN1,<br>Input/Output lines for CCU60 and CAPCOM2,<br>Timer control signals,<br>JTAG, interrupts, system clock output |
| Port 4 | 8 | Chip select signals,<br>Serial interface lines of CAN2,<br>Input/Output lines for CAPCOM2,<br>Timer control signals |
| Port 5 | 16 | Analog input channels to ADC0,<br>Input/Output lines for CCU6x,<br>Timer control signals,<br>JTAG, OCDS control, interrupts |

**Table 9 Summary of the XE164's Parallel Ports** (cont'd)

| Port | Width | Alternate Functions |
|---|---|---|
| Port 6 | 4 | ADC control lines,<br>Serial interface lines of USIC1,<br>Timer control signals,<br>OCDS control |
| Port 7 | 5 | ADC control lines,<br>Serial interface lines of USIC0,<br>Input/Output lines for CCU62,<br>Timer control signals,<br>JTAG, OCDS control,system clock output |
| Port 10 | 16 | Address and/or data lines, bus control,<br>Serial interface lines of USIC0, USIC1, CAN2 and CAN3,<br>Input/Output lines for CCU60,<br>JTAG, OCDS control |
| Port 15 | 8 | Analog input channels to ADC1,<br>Timer control signals |

**Table 18 A/D Converter Characteristics** (cont'd)
**(Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Switched capacitance of the reference input | $C_{AREFS}$ | CC | – | 7 | pF | 6)7) |
| Resistance of the reference input path | $R_{AREF}$ | CC | – | 2 | kΩ | 6)7) |

1) TUE is tested at $V_{AREFx}$ = $V_{DDPA}$, $V_{AGND}$ = 0 V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see $I_{OV}$ specification) does not exceed 10 mA, and if $V_{AREF}$ and $V_{AGND}$ remain stable during the measurement time.
2) $V_{AIN}$ may exceed $V_{AGND}$ or $V_{AREFx}$ up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
3) The limit values for $f_{ADCI}$ must not be exceeded when selecting the peripheral frequency and the prescaler setting.
4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock $t_{ADCI}$ depend on programming and are found in **Table 19**.
5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.
6) Not subject to production test - verified by design/characterization.
7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, $R_{AINtyp}$ = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

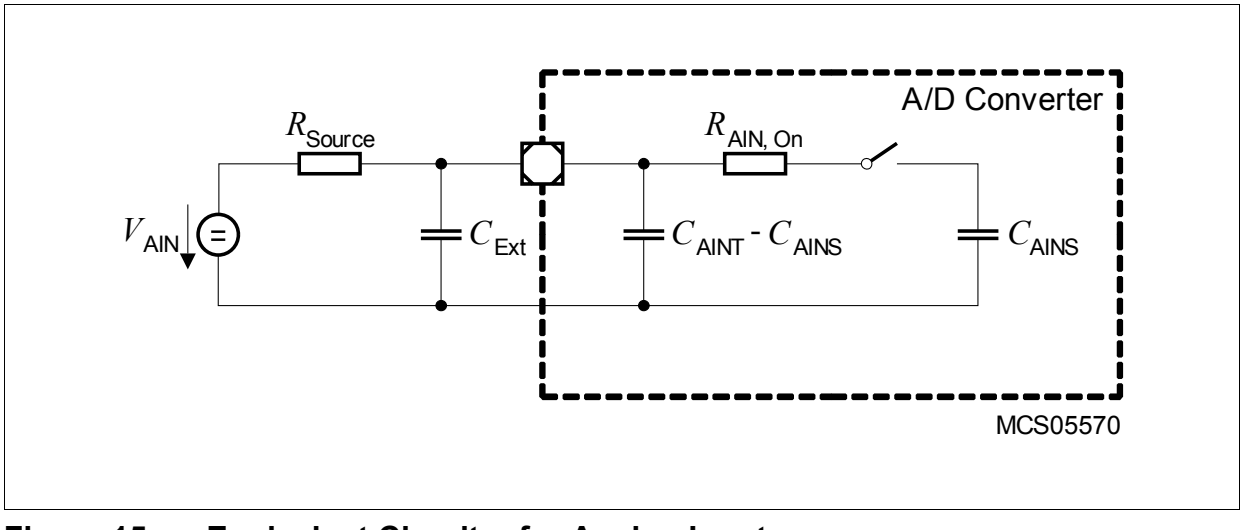


**Figure 15 Equivalent Circuitry for Analog Inputs**

## 4.5 Flash Memory Parameters

The XE164 is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE164's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 23 Flash Characteristics (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Programming time per 128-byte page | $t_{PR}$ | – | 3[1)] | 3.5 | ms | ms |
| Erase time per sector/page | $t_{ER}$ | – | 4[1)] | 5 | ms | ms |
| Data retention time | $t_{RET}$ | 20 | – | – | years | 1,000 erase / program cycles |
| Flash erase endurance for user sectors[2)] | $N_{ER}$ | 15,000 | – | – | cycles | Data retention time 5 years |
| Flash erase endurance for security pages | $N_{SEC}$ | 10 | – | – | cycles | Data retention time 20 years |
| Drain disturb limit | $N_{DD}$ | 64 | – | – | cycles | 3) |

1) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.
In the XE164 erased areas must be programmed completely (with actual code/data or dummy values) before that area is read.

2) A maximum of 64 Flash sectors can be cycled 15,000 times. For all other sectors the limit is 1,000 cycles.

3) This parameter limits the number of subsequent programming operations within a physical sector. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated.

Access to the XE164 Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

### 4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels $V_{IL}$ and $V_{IH}$. In connected to XTAL1, a minimum amplitude $V_{AX1}$ (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

*Note: The given clock timing parameters ($t_1$ … $t_4$) are only valid for an external clock input signal.*

**Table 26 External Clock Input Characteristics (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input voltage range limits for signal on XTAL1 | $V_{IX1}$ SR | -1.7 + $V_{DDI}$ | – | 1.7 | V | 1) |
| Input voltage (amplitude) on XTAL1 | $V_{AX1}$ SR | 0.3 × $V_{DDI}$ | – | – | V | Peak-to-peak voltage2) |
| XTAL1 input current | $I_{IL}$ CC | – | – | ±20 | µA | 0 V < $V_{IN}$ < $V_{DDI}$ |
| Oscillator frequency | $f_{OSC}$ CC | 4 | – | 40 | MHz | Clock signal |
| | | 4 | – | 16 | MHz | Crystal or Resonator |
| High time | $t_1$ SR | 6 | – | – | ns | |
| Low time | $t_2$ SR | 6 | – | – | ns | |
| Rise time | $t_3$ SR | – | 8 | 8 | ns | |
| Fall time | $t_4$ SR | – | 8 | 8 | ns | |

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage $V_{AX1}$ refers to the offset voltage $V_{OFF}$. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by $V_{IX1}$.

### Variable Memory Cycles

External bus cycles of the XE164 are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

**Table 28 Programmable Bus Cycle Phases (see timing diagrams)**

| Bus Cycle Phase | Parameter | Valid Values | Unit |
|---|---|---|---|
| Address setup phase, the standard duration of this phase (1 … 2 TCS) can be extended by 0 … 3 TCS if the address window is changed | tpAB | 1 … 2 (5) | TCS |
| Command delay phase | tpC | 0 … 3 | TCS |
| Write Data setup/MUX Tristate phase | tpD | 0 … 1 | TCS |
| Access phase | tpE | 1 … 32 | TCS |
| Address/Write Data hold phase | tpF | 0 … 3 | TCS |

*Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).*

Timing values are listed in **Table 29** and **Table 30**. The shaded parameters have been verified by characterization. They are not subject to production test.

**Table 30 External Bus Cycle Timing for Lower Voltage Range (Operating Conditions apply)**

| Parameter | Symbol | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output valid delay for: RD, WR(L/H) | $t_{10}$ CC | – | | 20 | ns | |
| Output valid delay for: BHE, ALE | $t_{11}$ CC | – | | 20 | ns | |
| Output valid delay for: A23 … A16, A15 … A0 (on P0/P1) | $t_{12}$ CC | – | | 22 | ns | |
| Output valid delay for: A15 … A0 (on P2/P10) | $t_{13}$ CC | – | | 22 | ns | |
| Output valid delay for: CS | $t_{14}$ CC | – | | 20 | ns | |
| Output valid delay for: D15 … D0 (write data, MUX-mode) | $t_{15}$ CC | – | | 21 | ns | |
| Output valid delay for: D15 … D0 (write data, DEMUX-mode) | $t_{16}$ CC | – | | 21 | ns | |
| Output hold time for: RD, WR(L/H) | $t_{20}$ CC | 0 | | 10 | ns | |
| Output hold time for: BHE, ALE | $t_{21}$ CC | 0 | | 10 | ns | |
| Output hold time for: A23 … A16, A15 … A0 (on P2/P10) | $t_{23}$ CC | 0 | | 10 | ns | |
| Output hold time for: CS | $t_{24}$ CC | 0 | | 10 | ns | |
| Output hold time for: D15 … D0 (write data) | $t_{25}$ CC | 0 | | 10 | ns | |
| Input setup time for: READY, D15 … D0 (read data) | $t_{30}$ SR | 29 | | – | ns | |
| Input hold time for: READY, D15 … D0 (read data)[1)] | $t_{31}$ SR | -6 | | – | ns | |

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

# 5 Package and Reliability

In addition to the electrical parameters, the following specifcations ensure proper integration of the XE164 into the target system.

## 5.1 Packaging

These parameters specify the packaging rather than the silicon.

**Table 34 Package Parameters (PG-LQFP-100-3)**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Exposed Pad Dimension | Ex × Ey | – | 6.2 × 6.2 | mm | – |
| Power Dissipation | $P_{DISS}$ | – | 1.0 | W | – |
| Thermal resistance Junction-Ambient | $R_{\Theta JA}$ | – | 49 | K/W | No thermal via[1)] |
| | | | 37 | K/W | 4-layer, no pad[2)] |
| | | | 22 | K/W | 4-layer, pad[3)] |

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) or a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.