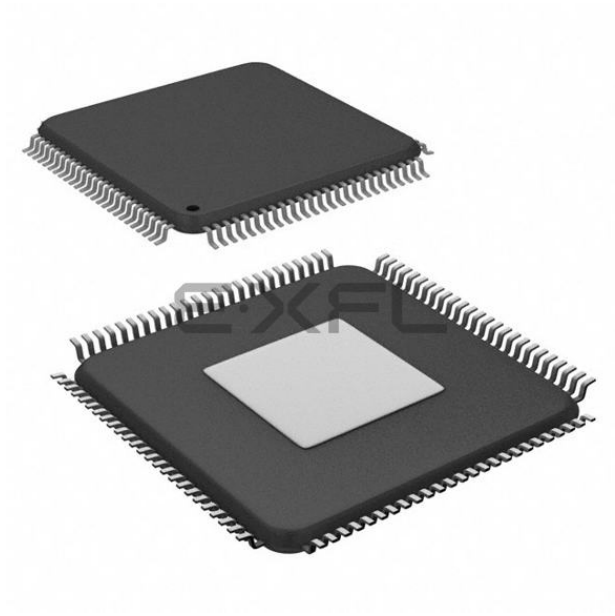
Infineon Technologies - SAF-XE164H-24F66L AC Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164h-24f66l-ac

XE164

16-Bit Single-Chip Real Time Signal Controller

Microcontrollers

Never stop thinking

The XE164 types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

Table 2 Flash Memory Allocation

Total Flash Size	Flash Area A[1)]	Flash Area B	Flash Area C
768 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $CB'FFFF_H$	n.a.
576 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C8'FFFF_H$	n.a.
384 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C5'FFFF_H$	n.a.
192 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'FFFF_H$	$C4'0000_H$ … $C4'FFFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE164 types are offered with different interface options. **Table 3** lists the available channels for each option.

Table 3 Interface Channel Association

Total Number	Available Channels
11 ADC0 channels	CH0, CH2 … CH5, CH8 … CH11, CH13, CH15
6 ADC0 channels	CH0, CH2, CH3, CH4, CH5, CH8
5 ADC1 channels	CH0, CH2, CH4, CH5, CH6
4 CAN nodes	CAN0, CAN1, CAN2, CAN3
2 CAN nodes	CAN0, CAN1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1
4 serial channels	U0C0, U0C1, U1C0, U1C1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_ CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	I	St/B	**JTAG Test Mode Selection Input**
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
8	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	CCU62_ CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**
9	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_ SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU62_ CCPOS2A	I	St/B	**CCU62 Position Input 2**
	TCK_C	I	St/B	**JTAG Clock Input**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**
11	P6.0	O0 / I	St/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	St/A	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	St/A	**OCDS Break Signal Output**
	ADCx_ REQGTyC	I	St/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	St/A	**USIC1 Channel 1 Shift Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
54	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_ SELO0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_ SELO1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	A20	OH	St/B	**External Bus Interface Address Line 20**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
55	P0.1	O0 / I	St/B	**Bit 1 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_ CC61	O3 / I	St/B	**CCU61 Channel 1 Input/Output**
	A1	OH	St/B	**External Bus Interface Address Line 1**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
56	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_ SCLKOUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output** 1)
	CC2_21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	A21	OH	DP/B	**External Bus Interface Address Line 21**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**
57	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	A22	OH	St/B	**External Bus Interface Address Line 22**
	CLKIN1	I	St/B	**Clock Signal Input**
	TCK_A	I	St/B	**JTAG Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
93	P1.6	O0 / I	St/B	**Bit 6 of Port 1, General Purpose Input/Output**
	CCU62_ CC61	O1 / I	St/B	**CCU62 Channel 1 Input/Output**
	U1C1_ SELO2	O2	St/B	**USIC1 Channel 1 Select/Control 2 Output**
	U2C0_DOUT	O3	St/B	**USIC2 Channel 0 Shift Data Output**
	A14	OH	St/B	**External Bus Interface Address Line 14**
	U2C0_DX0D	I	St/B	**USIC2 Channel 0 Shift Data Input**
94	P1.7	O0 / I	St/B	**Bit 7 of Port 1, General Purpose Input/Output**
	CCU62_ CC60	O1 / I	St/B	**CCU62 Channel 0 Input/Output**
	U1C1_ MCLKOUT	O2	St/B	**USIC1 Channel 1 Master Clock Output**
	U2C0_ SCLKOUT	O3	St/B	**USIC2 Channel 0 Shift Clock Output**
	A15	OH	St/B	**External Bus Interface Address Line 15**
	U2C0_DX1C	I	St/B	**USIC2 Channel 0 Shift Clock Input**
95	XTAL2	O	Sp/1	**Crystal Oscillator Amplifier Output**
96	XTAL1	I	Sp/1	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDI1}.
97	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XE164 completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pullup device will hold this pin high when nothing is driving it.

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to four external $\overline{CS}$ signals (three windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

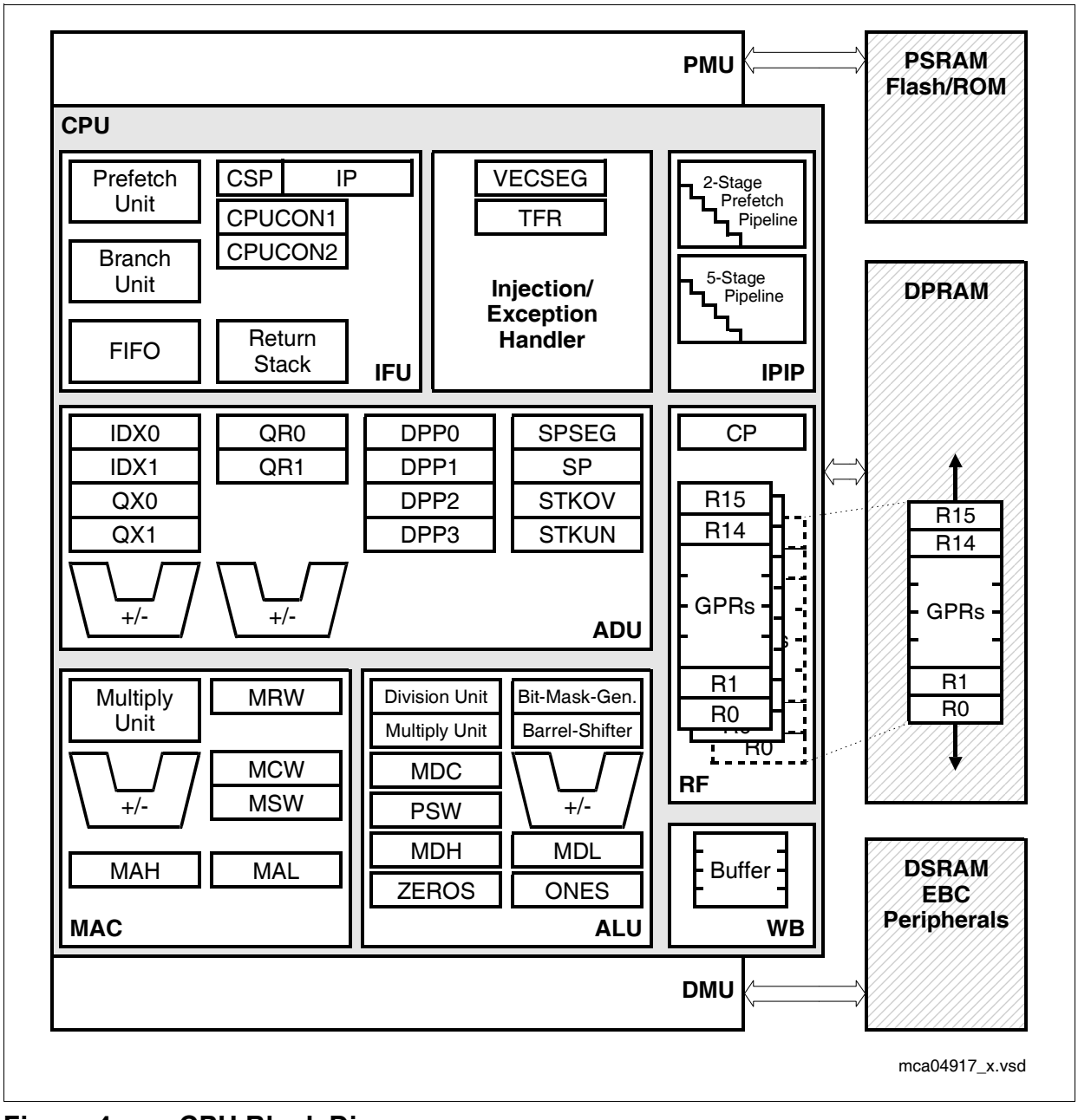

Figure 4 CPU Block Diagram

Table 6 XE164 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAN Request 1	CAN_1IC	xx'0104$_H$	41$_H$ / 65$_D$
CAN Request 2	CAN_2IC	xx'0108$_H$	42$_H$ / 66$_D$
CAN Request 3	CAN_3IC	xx'010C$_H$	43$_H$ / 67$_D$
CAN Request 4	CAN_4IC	xx'0110$_H$	44$_H$ / 68$_D$
CAN Request 5	CAN_5IC	xx'0114$_H$	45$_H$ / 69$_D$
CAN Request 6	CAN_6IC	xx'0118$_H$	46$_H$ / 70$_D$
CAN Request 7	CAN_7IC	xx'011C$_H$	47$_H$ / 71$_D$
CAN Request 8	CAN_8IC	xx'0120$_H$	48$_H$ / 72$_D$
CAN Request 9	CAN_9IC	xx'0124$_H$	49$_H$ / 73$_D$
CAN Request 10	CAN_10IC	xx'0128$_H$	4A$_H$ / 74$_D$
CAN Request 11	CAN_11IC	xx'012C$_H$	4B$_H$ / 75$_D$
CAN Request 12	CAN_12IC	xx'0130$_H$	4C$_H$ / 76$_D$
CAN Request 13	CAN_13IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAN Request 14	CAN_14IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAN Request 15	CAN_15IC	xx'013C$_H$	4F$_H$ / 79$_D$
USIC0 Cannel 0, Request 0	U0C0_0IC	xx'0140$_H$	50$_H$ / 80$_D$
USIC0 Cannel 0, Request 1	U0C0_1IC	xx'0144$_H$	51$_H$ / 81$_D$
USIC0 Cannel 0, Request 2	U0C0_2IC	xx'0148$_H$	52$_H$ / 82$_D$
USIC0 Cannel 1, Request 0	U0C1_0IC	xx'014C$_H$	53$_H$ / 83$_D$
USIC0 Cannel 1, Request 1	U0C1_1IC	xx'0150$_H$	54$_H$ / 84$_D$
USIC0 Cannel 1, Request 2	U0C1_2IC	xx'0154$_H$	55$_H$ / 85$_D$
USIC1 Cannel 0, Request 0	U1C0_0IC	xx'0158$_H$	56$_H$ / 86$_D$
USIC1 Cannel 0, Request 1	U1C0_1IC	xx'015C$_H$	57$_H$ / 87$_D$
USIC1 Cannel 0, Request 2	U1C0_2IC	xx'0160$_H$	58$_H$ / 88$_D$
USIC1 Cannel 1, Request 0	U1C1_0IC	xx'0164$_H$	59$_H$ / 89$_D$
USIC1 Cannel 1, Request 1	U1C1_1IC	xx'0168$_H$	5A$_H$ / 90$_D$
USIC1 Cannel 1, Request 2	U1C1_2IC	xx'016C$_H$	5B$_H$ / 91$_D$
USIC2 Cannel 0, Request 0	U2C0_0IC	xx'0170$_H$	5C$_H$ / 92$_D$
USIC2 Cannel 0, Request 1	U2C0_1IC	xx'0174$_H$	5D$_H$ / 93$_D$
USIC2 Cannel 0, Request 2	U2C0_2IC	xx'0178$_H$	5E$_H$ / 94$_D$

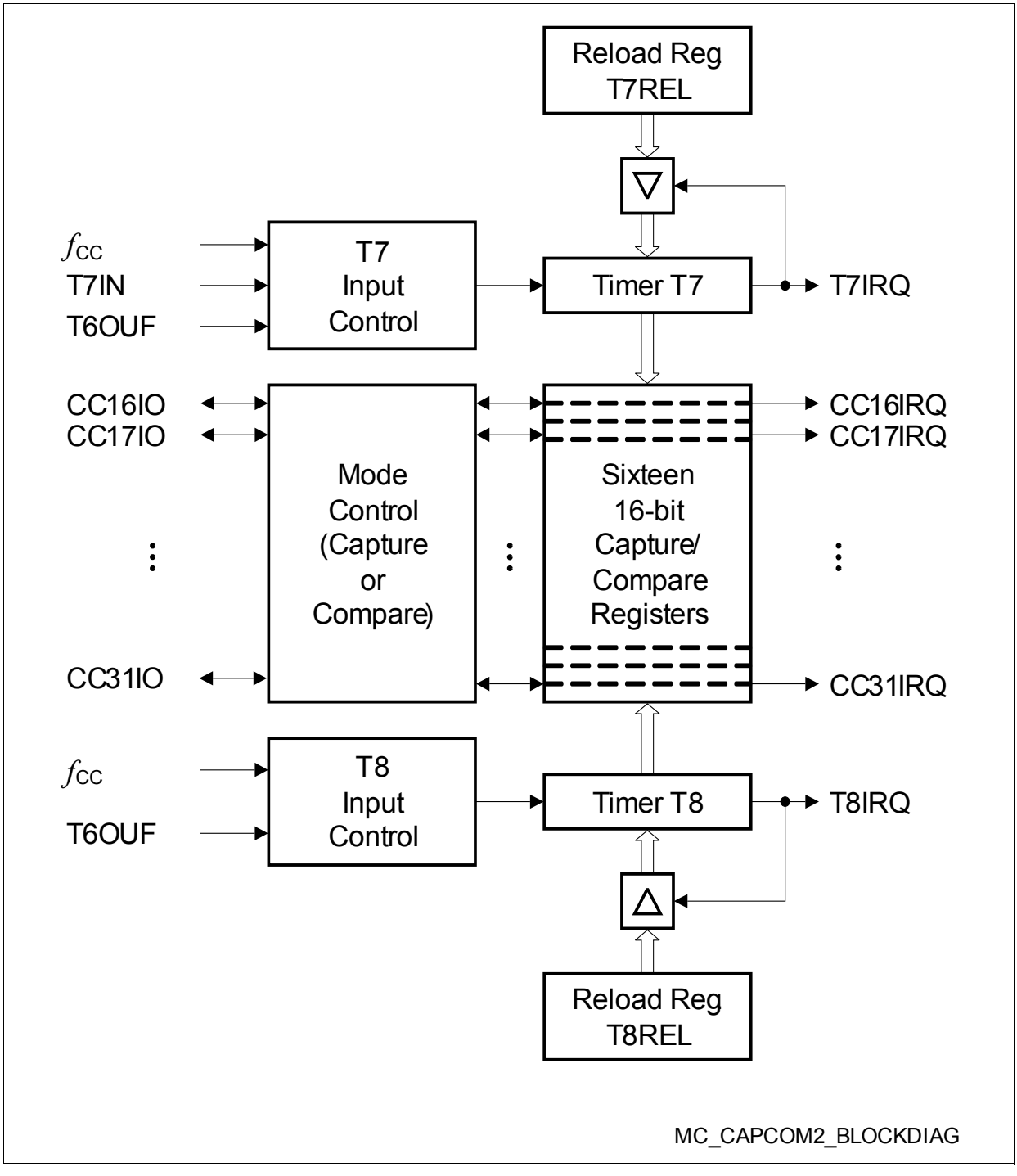

Figure 5 CAPCOM2 Unit Block Diagram

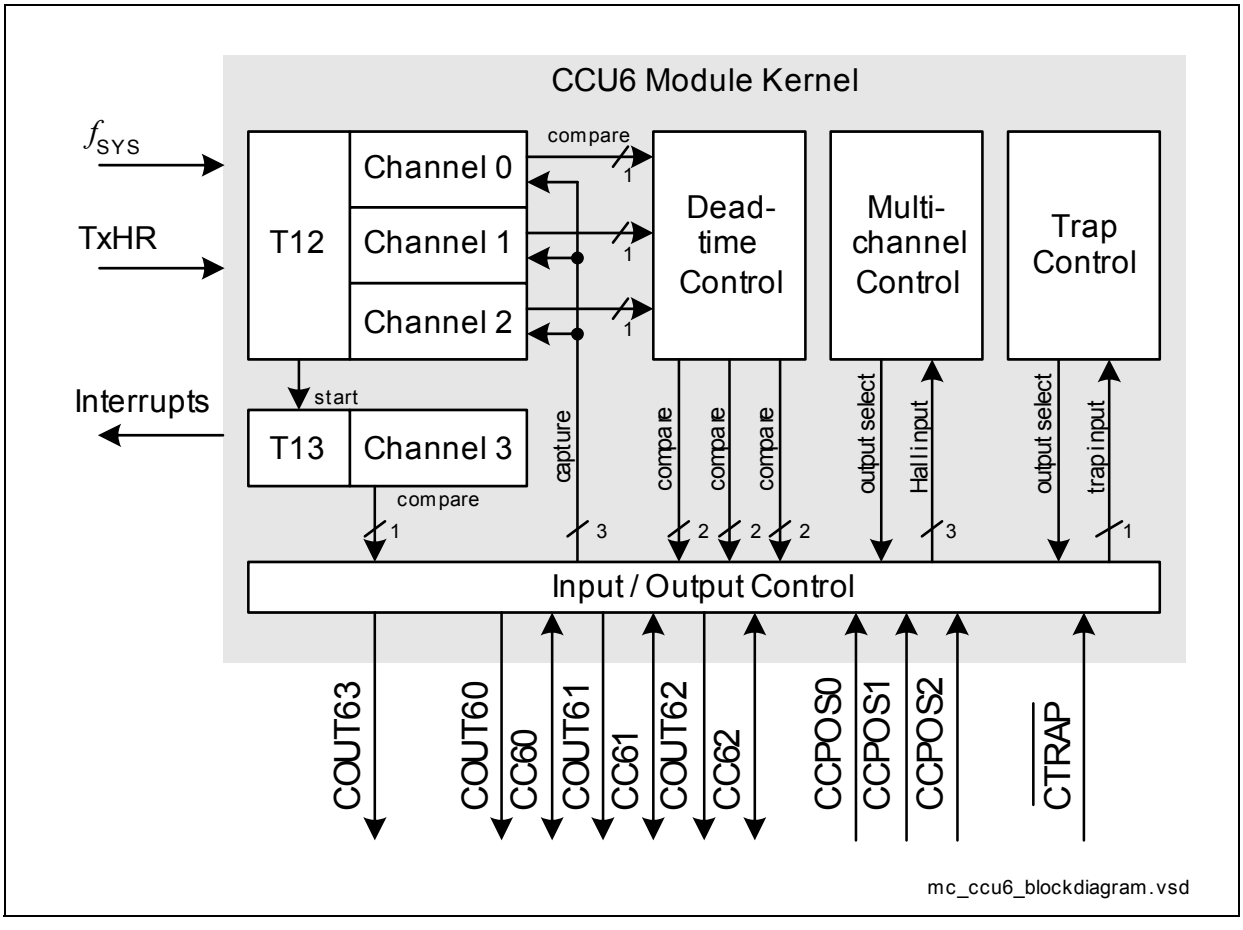

Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD[1)]). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE164 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

1) Exception: T5EUD is not connected to a pin.

3.16 Instruction Set Summary

Table 10 lists the instructions of the XE164.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 10 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 12 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital core supply voltage	V_{DDI}	1.4	–	1.6	V	
Core Supply Voltage Difference	ΔVDDI	-10	–	+10	mV	V_{DDIM} - V_{DDI1} 1)
Digital supply voltage for IO pads and voltage regulators, upper voltage range	V_{DDPA}, V_{DDPB}	4.5	–	5.5	V	2)
Digital supply voltage for IO pads and voltage regulators, lower voltage range	V_{DDPA}, V_{DDPB}	3.0	–	4.5	V	2)
Digital ground voltage	V_{SS}	0	–	0	V	Reference voltage
Overload current	I_{OV}	-5	–	5	mA	Per IO pin 3)4)
		-2	–	5	mA	Per analog input pin 3)4)
Overload positive current coupling factor for analog inputs 5)	K_{OVA}	–	1.0×10^{-6}	1.0×10^{-4}	–	$I_{OV} > 0$
Overload negative current coupling factor for analog inputs 5)	K_{OVA}	–	2.5×10^{-4}	1.5×10^{-3}	–	$I_{OV} < 0$
Overload positive current coupling factor for digital I/O pins 5)	K_{OVD}	–	1.0×10^{-4}	5.0×10^{-3}	–	$I_{OV} > 0$
Overload negative current coupling factor for digital I/O pins 5)	K_{OVD}	–	1.0×10^{-2}	3.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	Σ|IOV|	–	–	50	mA	4)

4.2.1 DC Parameters for Upper Voltage Area

These parameters apply to the upper IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Table 14 DC Characteristics for Upper Voltage Range (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input Hysteresis[2)]	HYS CC	0.11 × V_{DDP}	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \ge I_{OHmax}$[3)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5, Port 15)[6)]	I_{OZ1} CC	–	±10	±200	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±5	µA	$T_J \le$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Pull level keep current	I_{PLK}	–	–	±30	µA	$V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn)
Pull level force current	I_{PLF}	±250	–	–	µA	$V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn)
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
The leakage current value is not tested in the lower voltage range but only in the upper voltage range. This parameter is ensured by correlation.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.03 \times e^{(1.35 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 1.65 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.3 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

Table 16 Switching Power Consumption XE164 (Operating Conditions apply)

Parameter	Sym-bol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT}	–	10 + 0.6×f_{SYS}	10 + 1.0×f_{SYS}	mA	Active mode[1)2)] f_{SYS} in [MHz]
Power supply current in stopover mode, EVVRs on	I_{SSO}	–	1.0	2.0	mA	Stopover Mode[2)]

1) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers' input stages are switched.

2) The pad supply voltage has only a minor influence on this parameter.

Table 18 A/D Converter Characteristics (cont'd)
(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Switched capacitance of the reference input	C_{AREFS}	CC	–	7	pF	6)7)
Resistance of the reference input path	R_{AREF}	CC	–	2	kΩ	6)7)

1) TUE is tested at V_{AREFx} = V_{DDPA}, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.
2) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{ADCI} depend on programming and are found in **Table 19**.
5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.
6) Not subject to production test - verified by design/characterization.
7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

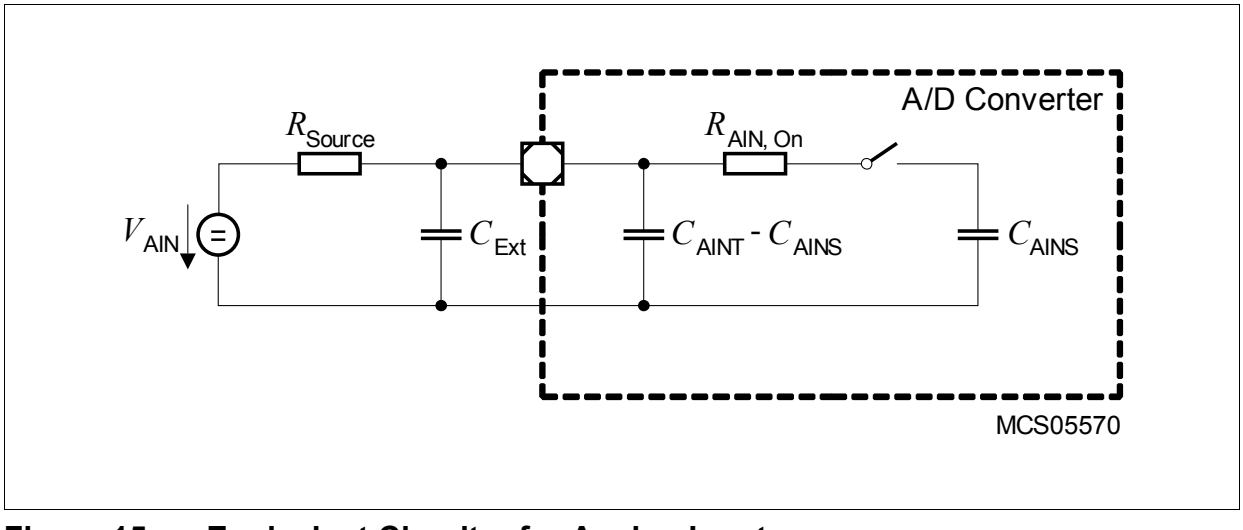

Figure 15 Equivalent Circuitry for Analog Inputs

4.5 Flash Memory Parameters

The XE164 is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE164's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 23 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Programming time per 128-byte page	t_{PR}	–	3[1)]	3.5	ms	ms
Erase time per sector/page	t_{ER}	–	4[1)]	5	ms	ms
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles
Flash erase endurance for user sectors[2)]	N_{ER}	15,000	–	–	cycles	Data retention time 5 years
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	Data retention time 20 years
Drain disturb limit	N_{DD}	64	–	–	cycles	3)

1) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.
In the XE164 erased areas must be programmed completely (with actual code/data or dummy values) before that area is read.

2) A maximum of 64 Flash sectors can be cycled 15,000 times. For all other sectors the limit is 1,000 cycles.

3) This parameter limits the number of subsequent programming operations within a physical sector. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated.

Access to the XE164 Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$f_{SYS} = f_{IN}$.

The frequency of f_{SYS} is the same as the frequency of f_{IN}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN}.

Selecting Bypass Operation from the XTAL1[1)] input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$f_{SYS} = f_{OSC}$ / K1.

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$f_{SYS} = f_{OSC}$ / 1024.

Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times$ **F**).
F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):
(**F** = N / (P $\times$ K2)).

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN}. The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDI1}.

5.2 Thermal Considerations

When operating the XE164 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 125 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (see **Section 4.2.3**).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers