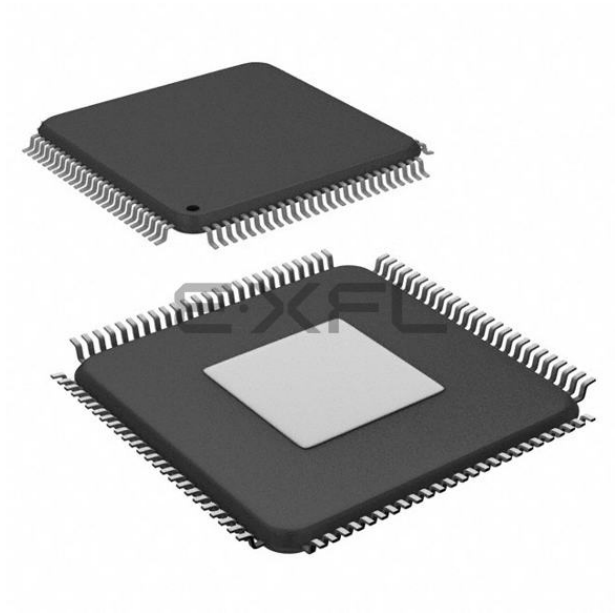
Infineon Technologies - SAF-XE164H-48F66L AC Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164h-48f66l-ac

XE164

16-Bit Single-Chip Real Time Signal Controller

Microcontrollers

Never stop thinking

Table 1 XE164 Derivative Synopsis

Derivative[1]	Temp. Range	Program Memory[2]	PSRAM[3]	CCU6 Mod.	ADC[4] Chan.	Interfaces[4]
SAF-XE164F-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164G-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164H-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164K-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.

1) This Data Sheet is valid for devices starting with and including design step AC.

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
23	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**
24	P5.3	I	In/A	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/A	**Analog Input Channel 3 for ADC0**
	T3IN	I	In/A	**GPT1 Timer T3 Count/Gate Input**
28	P5.4	I	In/A	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/A	**Analog Input Channel 4 for ADC0**
	T3EUD	I	In/A	**GPT1 Timer T3 External Up/Down Control Input**
	TMS_A	I	In/A	**JTAG Test Mode Selection Input**
29	P5.5	I	In/A	**Bit 5 of Port 5, General Purpose Input**
	ADC0_CH5	I	In/A	**Analog Input Channel 5 for ADC0**
	CCU60_ T12HRB	I	In/A	**External Run Control Input for T12 of CCU60**
30	P5.8	I	In/A	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/A	**Analog Input Channel 8 for ADC0**
	CCU6x_ T12HRC	I	In/A	**External Run Control Input for T12 of CCU6x**
	CCU6x_ T13HRC	I	In/A	**External Run Control Input for T13 of CCU6x**
31	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
32	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	$\overline{\text{BRKIN\_A}}$	I	In/A	**OCDS Break Signal Input**
33	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
34	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
	EX0BINB	I	In/A	**External Interrupt Trigger Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
73	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_ COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD7	OH / I	St/B	**External Bus Interface Address/Data Line 7**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_ CCPOS0A	I	St/B	**CCU60 Position Input 0**
74	P0.7	O0 / I	St/B	**Bit 7 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	U1C0_ SELO3	O2	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	A7	OH	St/B	**External Bus Interface Address Line 7**
	U1C1_DX0B	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_ CTRAPB	I	St/B	**CCU61 Emergency Trap Input**
78	P1.0	O0 / I	St/B	**Bit 0 of Port 1, General Purpose Input/Output**
	U1C0_ MCLKOUT	O1	St/B	**USIC1 Channel 0 Master Clock Output**
	U1C0_ SELO4	O2	St/B	**USIC1 Channel 0 Select/Control 4 Output**
	A8	OH	St/B	**External Bus Interface Address Line 8**
	ESR1_3	I	St/B	**ESR1 Trigger Input 3**
	EX0BINA	I	St/B	**External Interrupt Trigger Input**
	CCU62_ CTRAPB	I	St/B	**CCU62 Emergency Trap Input**

3 Functional Description

The architecture of the XE164 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE164.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE164.

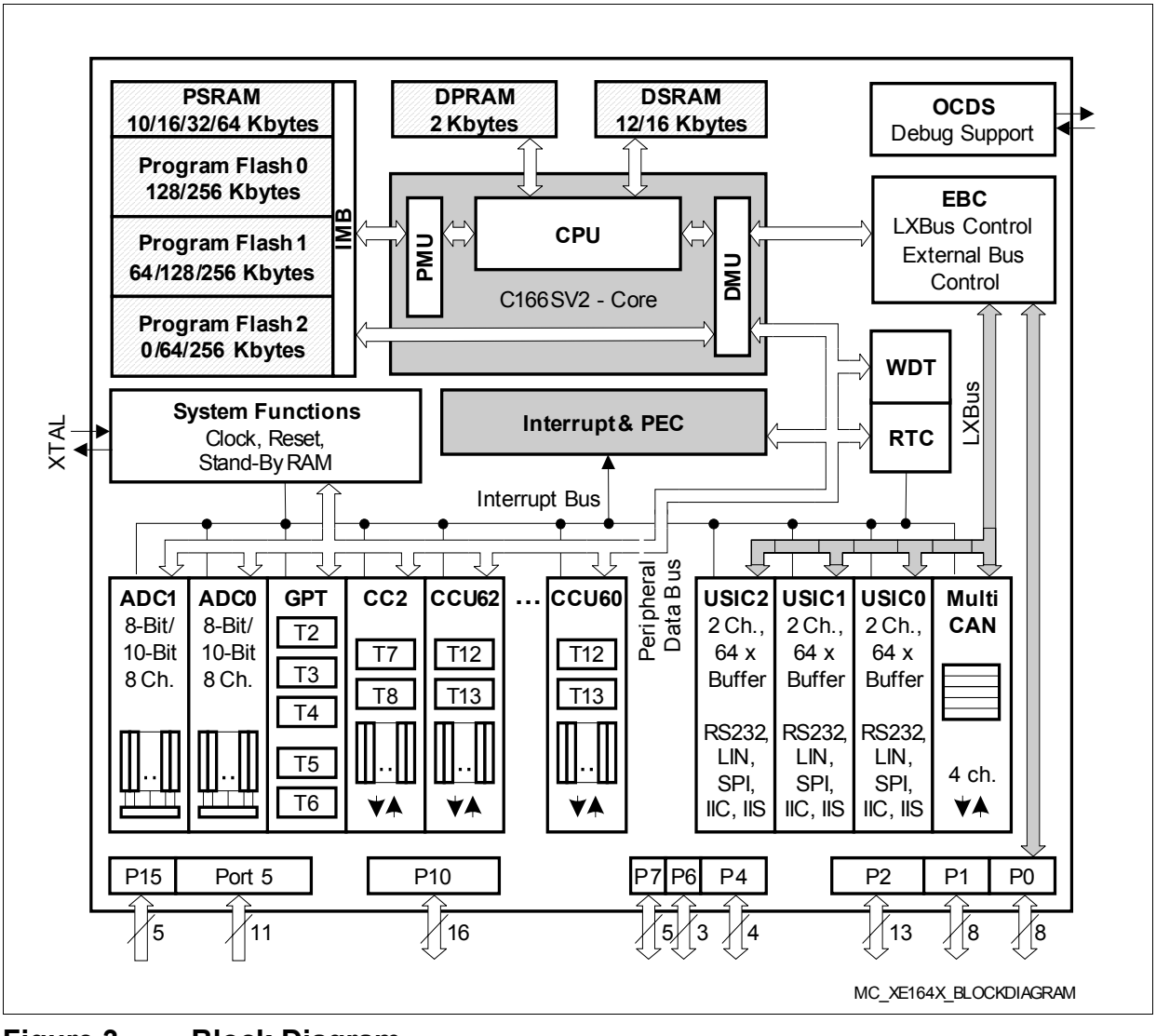

Figure 3 Block Diagram

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

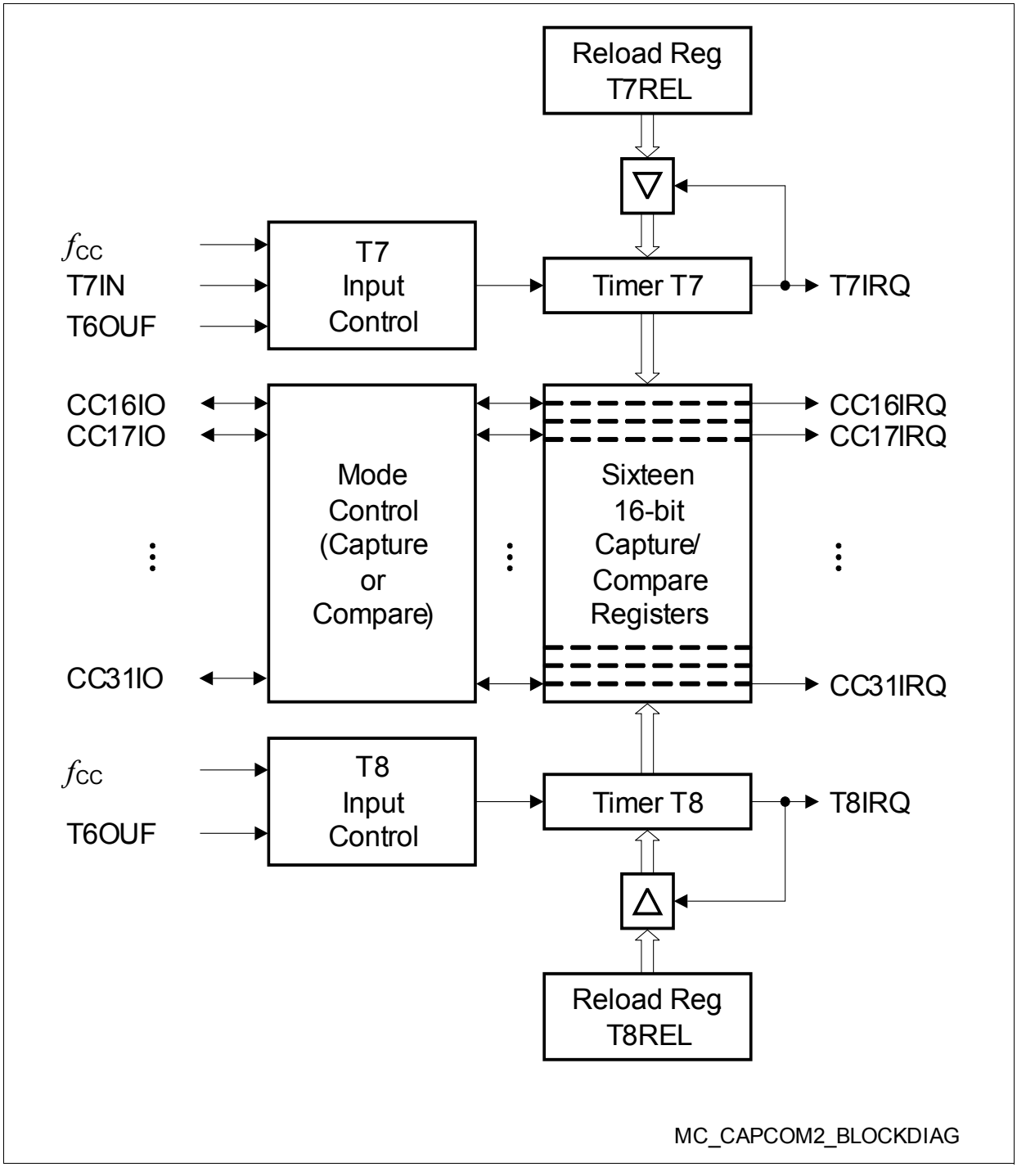

Figure 5 CAPCOM2 Unit Block Diagram

4 Electrical Parameters

The operating range for the XE164 is defined by its electrical parameters. For proper operation the specified limits must be respected during system design.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature	T_{ST}	-65	–	150	°C	–
Junction temperature	T_J	-40	–	125	°C	under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDIM}, V_{DDI1}	-0.5	–	1.65	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDPA}, V_{DDPB}	-0.5	–	6.0	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} < V_{DDPmax}$
Input current on any pin during overload condition	–	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	–	–	–	|100|	mA	–
Output current on any pin	I_{OH}, I_{OL}	–	–	|30|	mA	–

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Pullup/Pulldown Device Behavior

Most pins of the XE164 feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 12** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

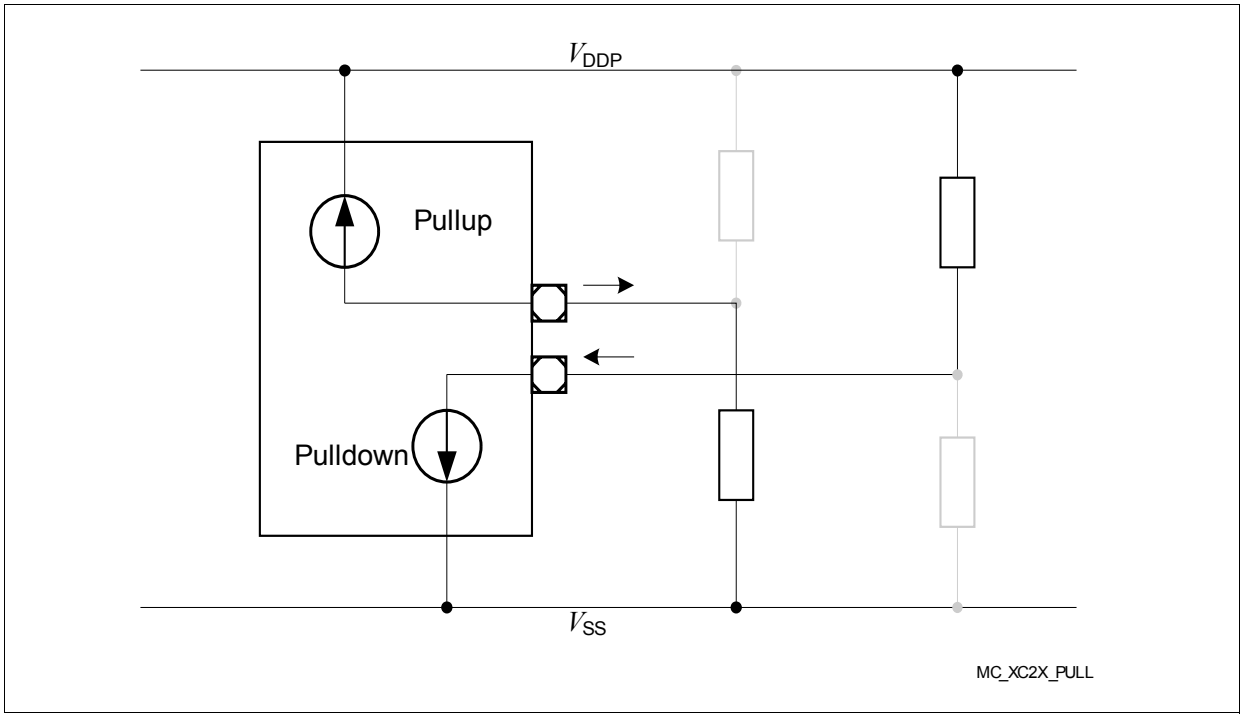

Figure 12 Pullup/Pulldown Current Definition

4.2.1 DC Parameters for Upper Voltage Area

These parameters apply to the upper IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Table 14 DC Characteristics for Upper Voltage Range (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input Hysteresis[2)]	HYS CC	0.11 × V_{DDP}	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \ge I_{OHmax}$[3)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5, Port 15)[6)]	I_{OZ1} CC	–	±10	±200	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±5	µA	$T_J \le$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Pull level keep current	I_{PLK}	–	–	±30	µA	$V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn)
Pull level force current	I_{PLF}	±250	–	–	µA	$V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn)
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

4.2.2 DC Parameters for Lower Voltage Area

These parameters apply to the lower IO voltage range, 3.0 V ≤ V_{DDP} ≤ 4.5 V.

Table 15 DC Characteristics for Lower Voltage Range (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input Hysteresis[2)]	HYS CC	0.07 × V_{DDP}	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \ge I_{OHmax}$[3)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5, Port 15)[6)]	I_{OZ1} CC	–	±10	±200	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±2.5	µA	$T_J \le$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Pull level keep current	I_{PLK}	–	–	±10	µA	$V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn)
Pull level force current	I_{PLF}	±150	–	–	µA	$V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn)
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

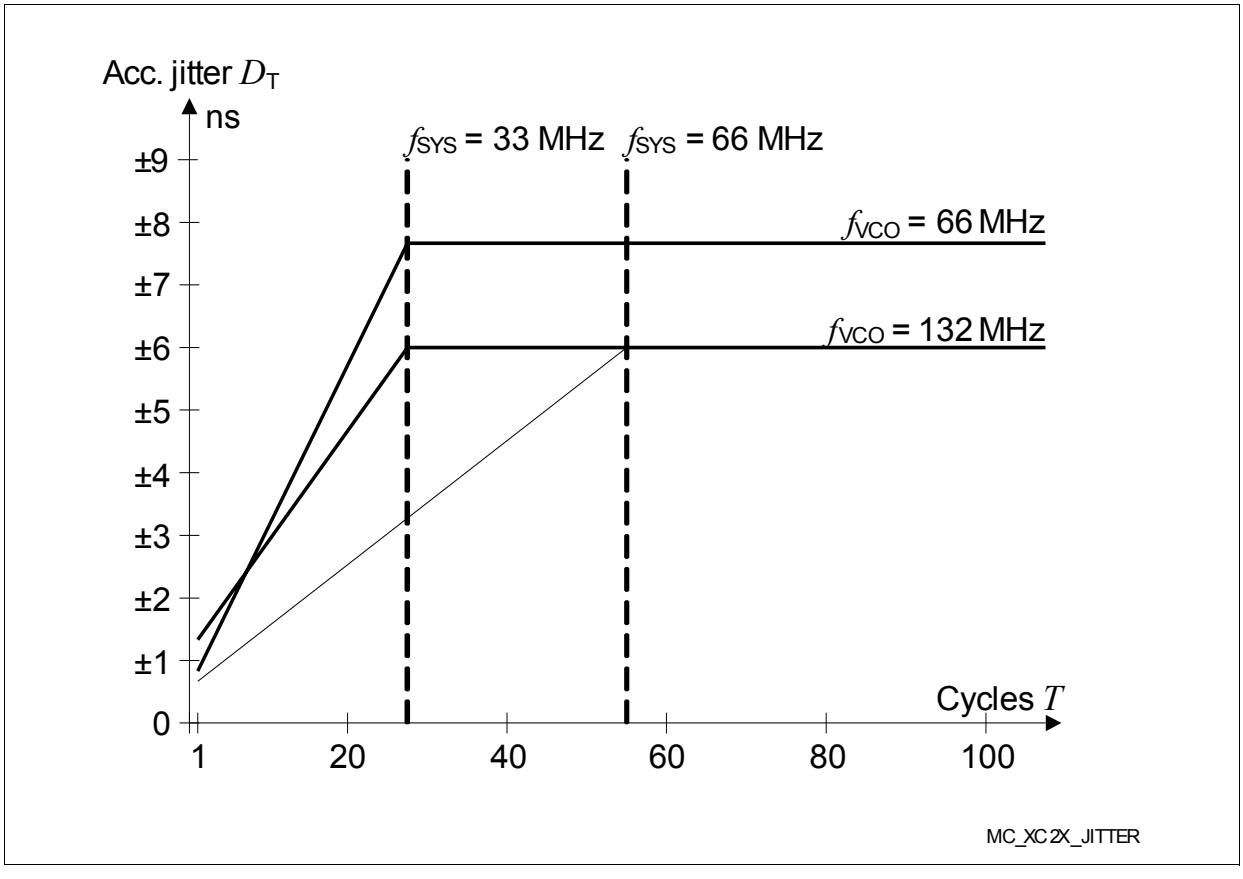

Figure 19 Approximated Accumulated PLL Jitter

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF (see **Table 12**).*
The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100/144 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 25 VCO Bands for PLL Operation[1)]

PLLCON0.VCOSEL	VCO Frequency Range	Base Frequency Range
00	50 … 110 MHz	10 … 40 MHz
01	100 … 160 MHz	20 … 80 MHz
1X	Reserved	

1) Not subject to production test - verified by design/characterization.

Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

Table 32 SSC Master/Slave Mode Timing for Lower Voltage Range (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	–	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0.5 × t_{BIT}	–	3)	ns	2)
Transmit data output valid time	t_3 CC	-13	–	16	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	48	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-11	–	–	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	12	–	–	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	8	–	–	ns	4)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	12	–	–	ns	4)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	8	–	–	ns	4)
Data output DOUT valid time	t_{14} CC	11	–	44	ns	4)

1) The maximum value further depends on the settings for the slave select output leading delay.

2) $t_{SYS} = 1/f_{SYS}$ (= 12.5 ns @ 80 MHz)

3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

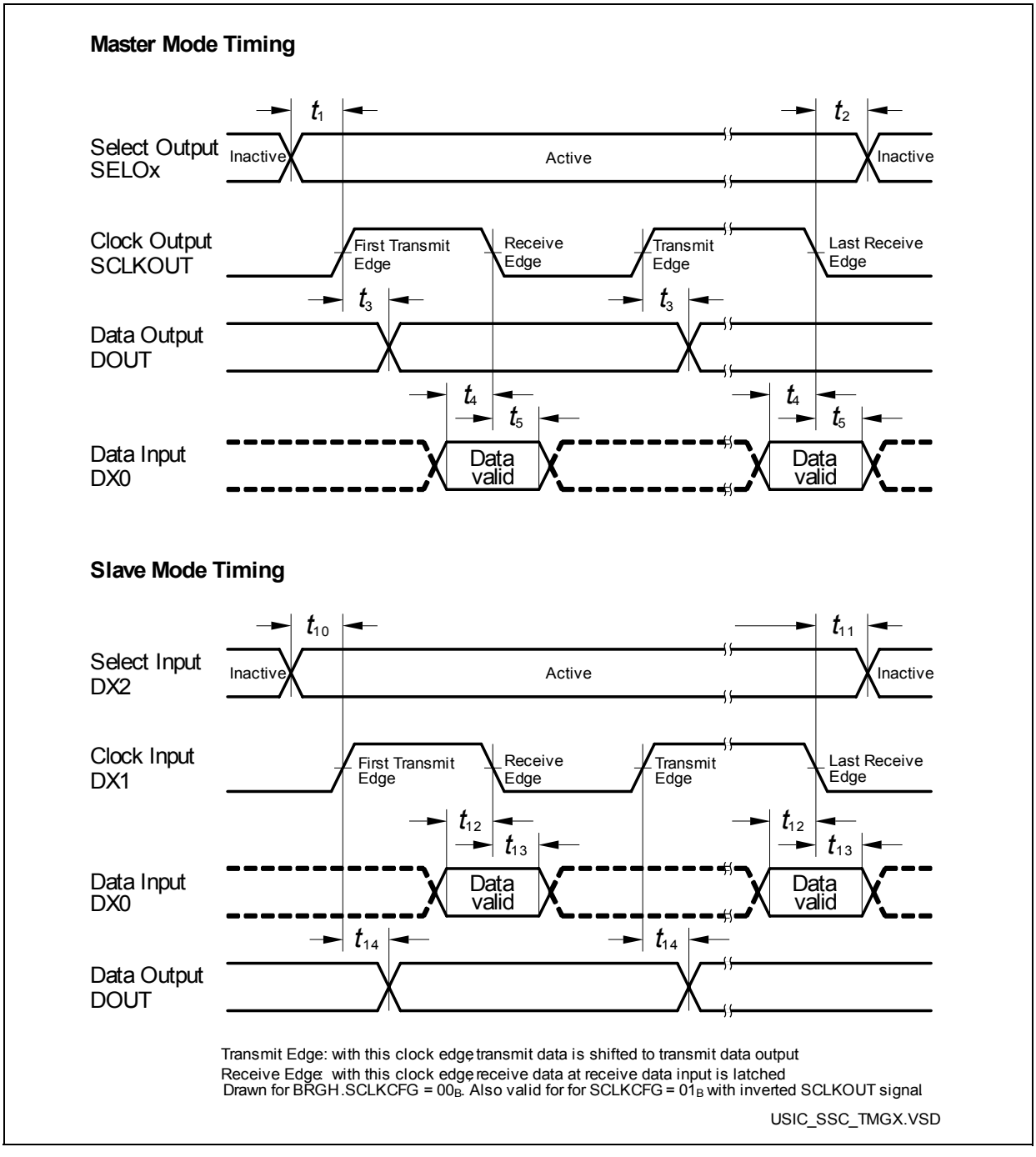

Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

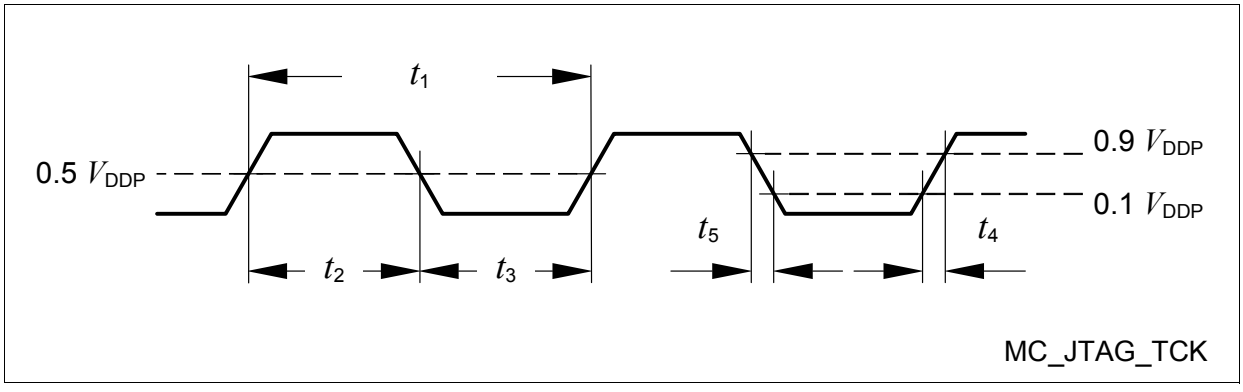

Figure 26 Test Clock Timing (TCK)

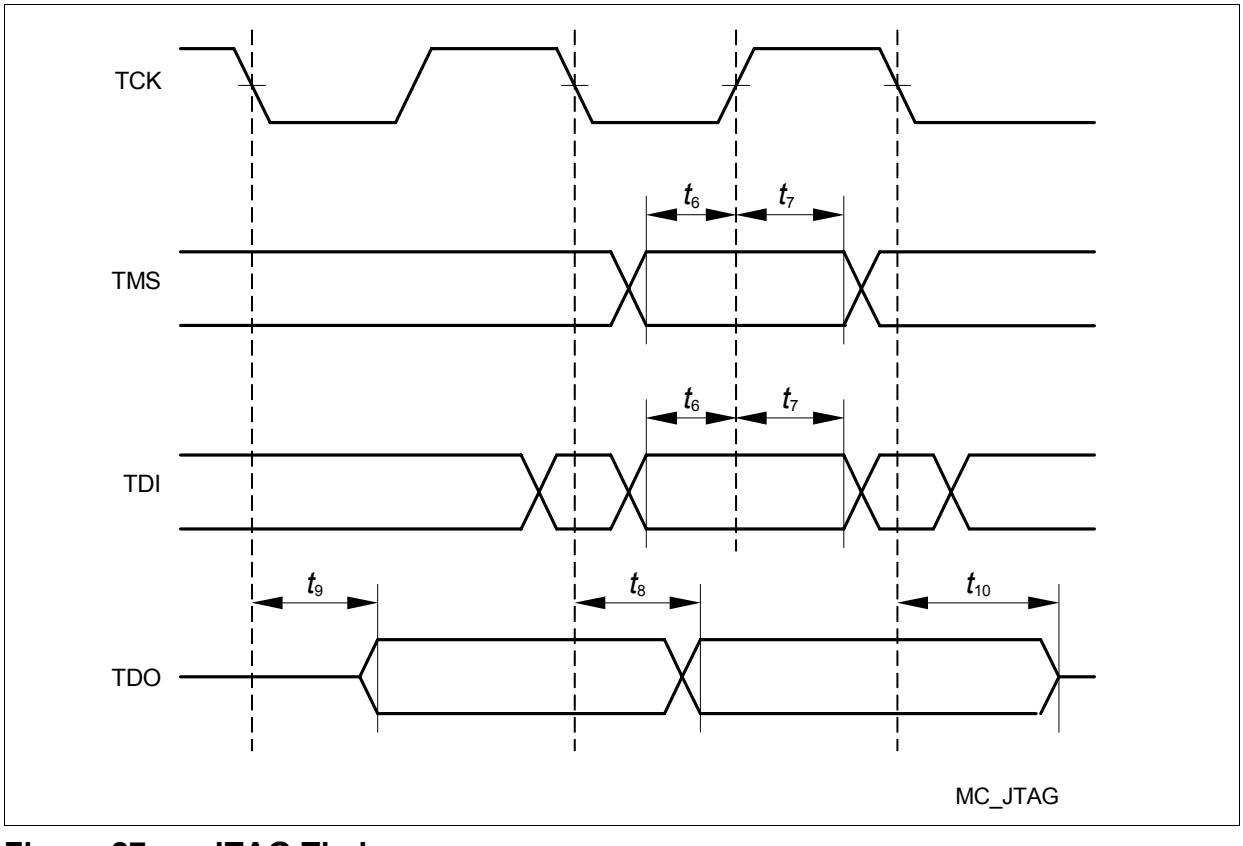

Figure 27 JTAG Timing

Package Outlines

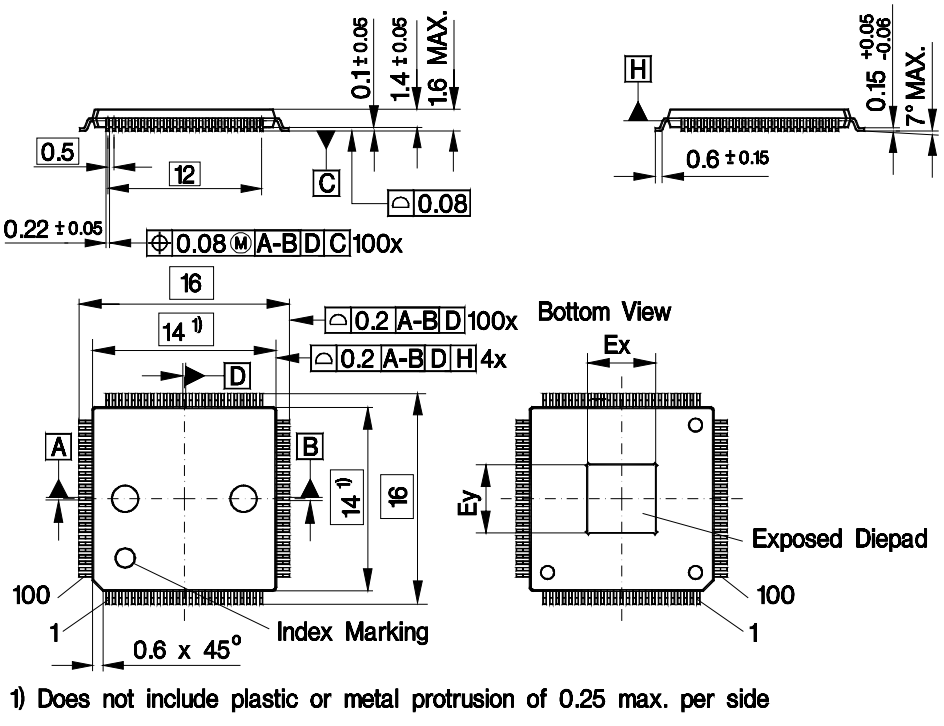

Figure 28 PG-LQFP-100-3 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

5.2 Thermal Considerations

When operating the XE164 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 125 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (see **Section 4.2.3**).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers