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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164h-72f66l-ac

Summary of Features

Table 1 XE164 Derivative Synopsis

Derivative¹⁾	Temp. Range	Program Memory²⁾	PSRAM³⁾	CCU6 Mod.	ADC⁴⁾ Chan.	Interfaces⁴⁾
SAF-XE164F-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164G-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164H-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164K-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.

1) This Data Sheet is valid for devices starting with and including design step AC.

Summary of Features

- 2) Specific information about the on-chip Flash memory in [Table 2](#).
- 3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM (12 Kbytes for devices with 192 Kbytes of Flash).
- 4) Specific information about the available channels in [Table 3](#).
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Notes to Pin Definitions

1. **Ctrl.:** The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bitfield PC to 1x00_B, output O1 is selected by 1x01_B, etc.
Output signal OH is controlled by hardware.
2. **Type:** Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	CCU62_ CCPOS0A	I	St/B	CCU62 Position Input 0
	TDI_C	I	St/B	JTAG Test Data Input
5	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE164's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT1 Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT2 Timer T6 Toggle Latch Output
	TDO_A	OH	St/B	JTAG Test Data Output
	ESR2_1	I	St/B	ESR2 Trigger Input 1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_ CCPOS1A	I	St/B	CCU62 Position Input 1
	TMS_C	I	St/B	JTAG Test Mode Selection Input
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	CCU62_ CTRAPA	I	St/B	CCU62 Emergency Trap Input
	$\overline{\text{BRKIN_C}}$	I	St/B	OCDS Break Signal Input
9	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_ SCLKOUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	CCU62_ CCPOS2A	I	St/B	CCU62 Position Input 2
	TCK_C	I	St/B	JTAG Clock Input
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input
11	P6.0	O0 / I	St/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	St/A	External Analog MUX Control Output 0 (ADC0)
	$\overline{\text{BRKOUT}}$	O3	St/A	OCDS Break Signal Output
	ADCx_ REQGTyC	I	St/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	St/A	USIC1 Channel 1 Shift Data Input

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
93	P1.6	O0 / I	St/B	Bit 6 of Port 1, General Purpose Input/Output
	CCU62_ CC61	O1 / I	St/B	CCU62 Channel 1 Input/Output
	U1C1_ SELO2	O2	St/B	USIC1 Channel 1 Select/Control 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	A14	OH	St/B	External Bus Interface Address Line 14
	U2C0_DX0D	I	St/B	USIC2 Channel 0 Shift Data Input
94	P1.7	O0 / I	St/B	Bit 7 of Port 1, General Purpose Input/Output
	CCU62_ CC60	O1 / I	St/B	CCU62 Channel 0 Input/Output
	U1C1_ MCLKOUT	O2	St/B	USIC1 Channel 1 Master Clock Output
	U2C0_ SCLKOUT	O3	St/B	USIC2 Channel 0 Shift Clock Output
	A15	OH	St/B	External Bus Interface Address Line 15
	U2C0_DX1C	I	St/B	USIC2 Channel 0 Shift Clock Input
95	XTAL2	O	Sp/1	Crystal Oscillator Amplifier Output
96	XTAL1	I	Sp/1	Crystal Oscillator Amplifier Input To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDI1} .
97	$\overline{\text{PORST}}$	I	In/B	Power On Reset Input A low level at this pin resets the XE164 completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pullup device will hold this pin high when nothing is driving it.

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections¹⁾:

- Address Bus Width with a range of 0 ... 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes ... 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to four external $\overline{\text{CS}}$ signals (three windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.

Access to very slow memories or modules with varying access times is supported by a special 'Ready' function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

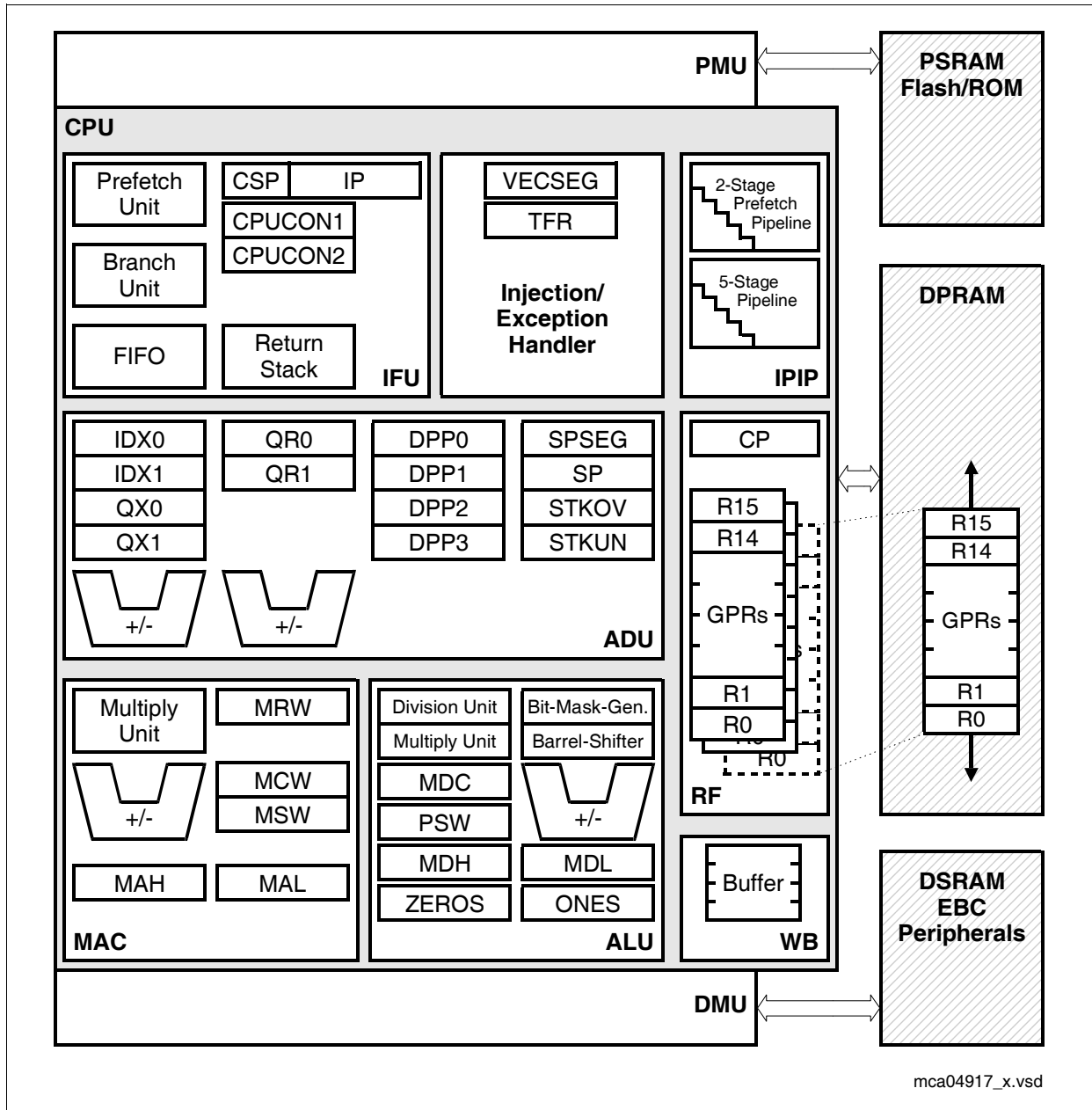


Figure 4 CPU Block Diagram

Functional Description

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

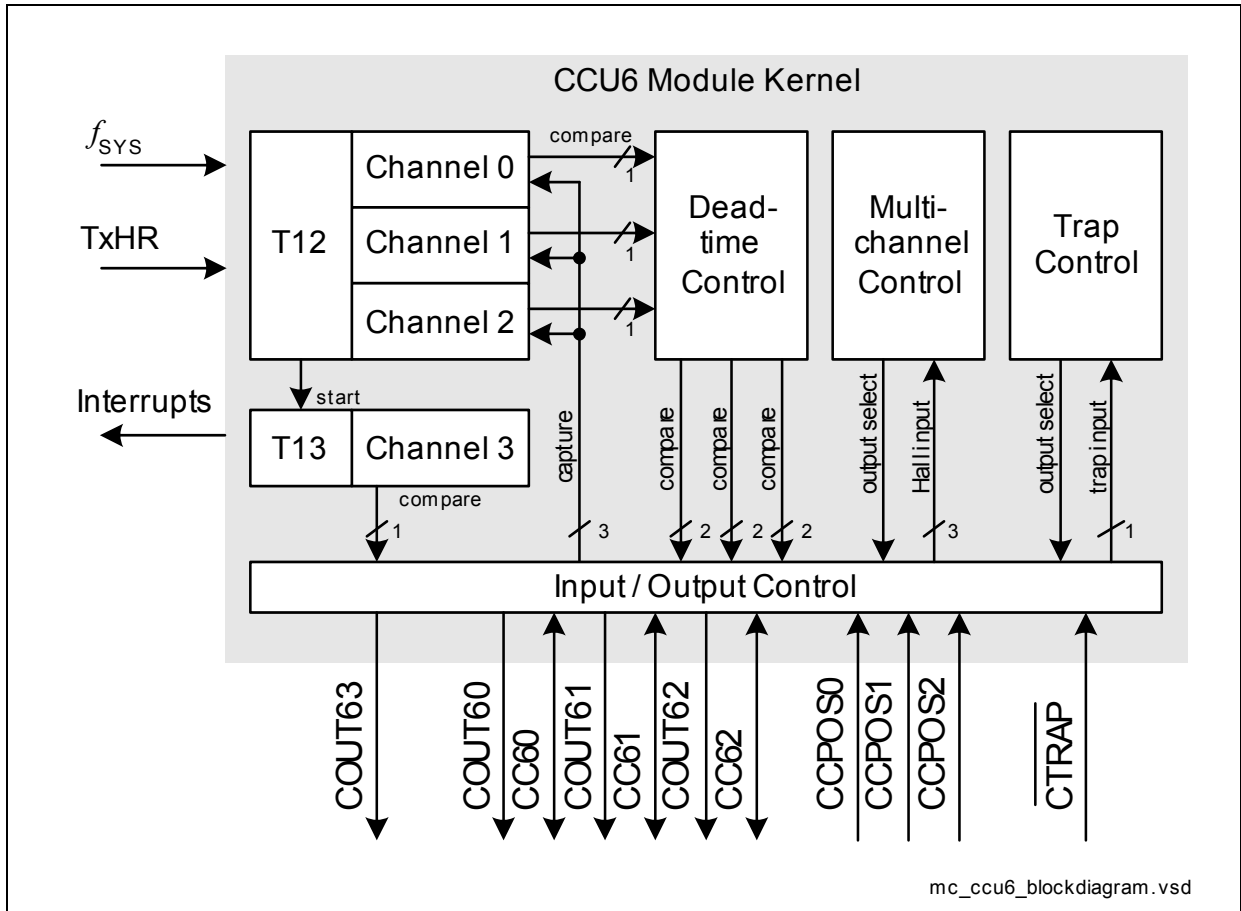


Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

3.11 Universal Serial Interface Channel Modules (USIC)

The XE164 includes up to three USIC modules (USIC0, USIC1, USIC2), each providing two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.



Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

Table 9 Summary of the XE164's Parallel Ports (cont'd)

Port	Width	Alternate Functions
Port 6	4	ADC control lines, Serial interface lines of USIC1, Timer control signals, OCDS control
Port 7	5	ADC control lines, Serial interface lines of USIC0, Input/Output lines for CCU62, Timer control signals, JTAG, OCDS control, system clock output
Port 10	16	Address and/or data lines, bus control, Serial interface lines of USIC0, USIC1, CAN2 and CAN3, Input/Output lines for CCU60, JTAG, OCDS control
Port 15	8	Analog input channels to ADC1, Timer control signals

Pullup/Pulldown Device Behavior

Most pins of the XE164 feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 12** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

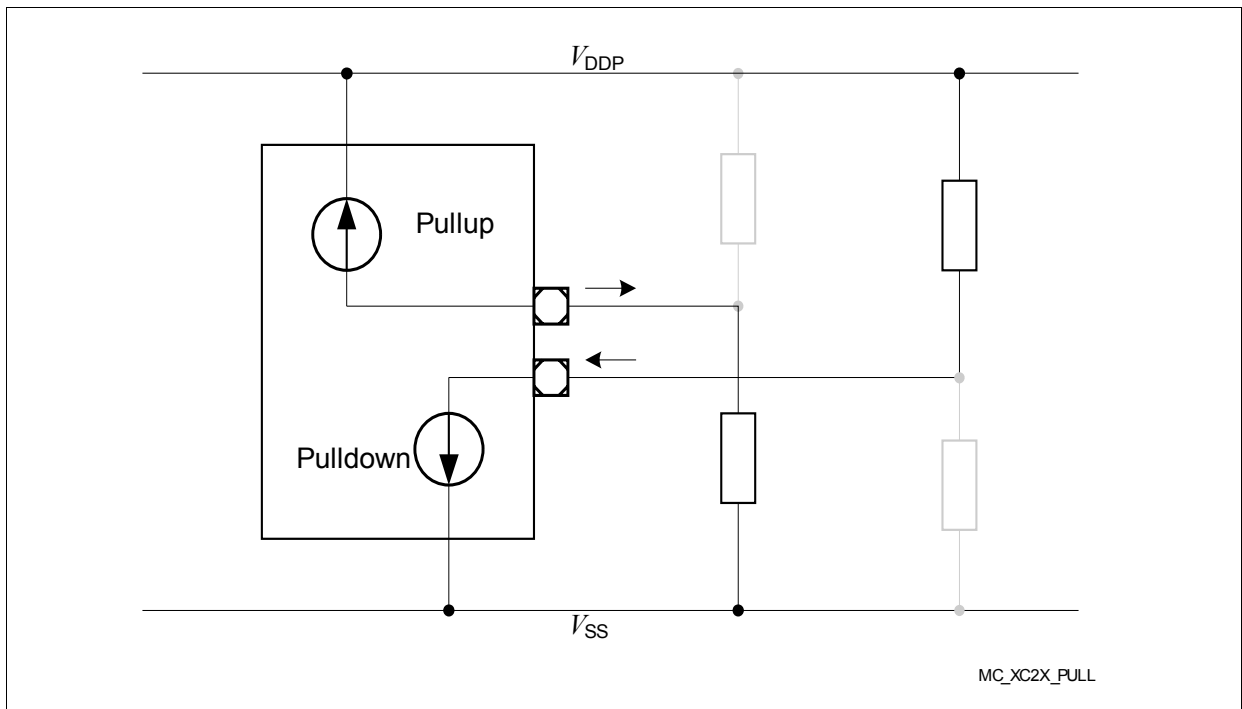


Figure 12 Pullup/Pulldown Current Definition

Table 16 Switching Power Consumption XE164
(Operating Conditions apply)

Parameter	Sym- bol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT}	–	10 + $0.6 \times f_{\text{SYS}}$	10 + $1.0 \times f_{\text{SYS}}$	mA	Active mode ¹⁾²⁾ f_{SYS} in [MHz]
Power supply current in stopover mode, EVVRs on	I_{SSO}	–	1.0	2.0	mA	Stopover Mode ²⁾

1) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers' input stages are switched.

2) The pad supply voltage has only a minor influence on this parameter.

Electrical Parameters

Sample time and conversion time of the XE164's A/D converters are programmable. The timing above can be calculated using [Table 19](#).

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 19 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time t_s
000000 _B	f_{SYS}	00 _H	$t_{\text{ADCI}} \times 2$
000001 _B	$f_{\text{SYS}} / 2$	01 _H	$t_{\text{ADCI}} \times 3$
000010 _B	$f_{\text{SYS}} / 3$	02 _H	$t_{\text{ADCI}} \times 4$
:	$f_{\text{SYS}} / (\text{DIVA}+1)$:	$t_{\text{ADCI}} \times (\text{STC}+2)$
111110 _B	$f_{\text{SYS}} / 63$	FE _H	$t_{\text{ADCI}} \times 256$
111111 _B	$f_{\text{SYS}} / 64$	FF _H	$t_{\text{ADCI}} \times 257$

Converter Timing Example A:

Assumptions: $f_{\text{SYS}} = 80 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 12.5 \text{ ns}$), $\text{DIVA} = 03_{\text{H}}$, $\text{STC} = 00_{\text{H}}$
 Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 4 = 20 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 50 \text{ ns}$
 Sample time $t_s = t_{\text{ADCI}} \times 2 = 100 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 13 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 13 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.675 \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 11 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 11 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.575 \mu\text{s}$$

Converter Timing Example B:

Assumptions: $f_{\text{SYS}} = 40 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 25 \text{ ns}$), $\text{DIVA} = 02_{\text{H}}$, $\text{STC} = 03_{\text{H}}$
 Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 3 = 13.3 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 75 \text{ ns}$
 Sample time $t_s = t_{\text{ADCI}} \times 5 = 375 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 16 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 16 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.25 \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 14 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 14 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.10 \mu\text{s}$$

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$$f_{\text{SYS}} = f_{\text{IN}}$$

The frequency of f_{SYS} is the same as the frequency of f_{IN} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN} .

Selecting Bypass Operation from the XTAL1¹⁾ input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$$f_{\text{SYS}} = f_{\text{OSC}} / K1.$$

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$$f_{\text{SYS}} = f_{\text{OSC}} / 1024.$$

Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{\text{SYS}} = f_{\text{IN}} \times \mathbf{F}$).

F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):

$$(\mathbf{F} = N / (P \times K2)).$$

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN} . The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDI1} .

Electrical Parameters

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.

The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and [Figure 19](#)).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS} . The number of VCO cycles is $K2 \times T$, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

$$D_{Tmax} [ns] = \pm(220 / (K2 \times f_{SYS}) + 4.3)$$

This maximum value is applicable, if either the number of clock cycles $T > (f_{SYS} / 1.2)$ or the prescaler value $K2 > 17$.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

$$D_T [ns] = D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$$

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

$$D_{max} = \pm(220 / (4 \times 33) + 4.3) = 5.97 \text{ ns (Not applicable directly in this case!)}$$

$$\begin{aligned} D_3 &= 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4] \\ &= 5.97 \times [0.768 \times 2 / 26.39 + 0.232] \\ &= 1.7 \text{ ns} \end{aligned}$$

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

$$D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63 \text{ ns (Not applicable directly in this case!)}$$

$$\begin{aligned} D_3 &= 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 2] \\ &= 7.63 \times [0.884 \times 2 / 26.39 + 0.116] \\ &= 1.4 \text{ ns} \end{aligned}$$

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH} . In connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters ($t_1 \dots t_4$) are only valid for an external clock input signal.

Table 26 External Clock Input Characteristics
(Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range limits for signal on XTAL1	V_{IX1} SR	$-1.7 + V_{DDI}$	–	1.7	V	1)
Input voltage (amplitude) on XTAL1	V_{AX1} SR	$0.3 \times V_{DDI}$	–	–	V	Peak-to-peak voltage ²⁾
XTAL1 input current	I_{IL} CC	–	–	± 20	μA	$0 V < V_{IN} < V_{DDI}$
Oscillator frequency	f_{OSC} CC	4	–	40	MHz	Clock signal
		4	–	16	MHz	Crystal or Resonator
High time	t_1 SR	6	–	–	ns	
Low time	t_2 SR	6	–	–	ns	
Rise time	t_3 SR	–	8	8	ns	
Fall time	t_4 SR	–	8	8	ns	

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .

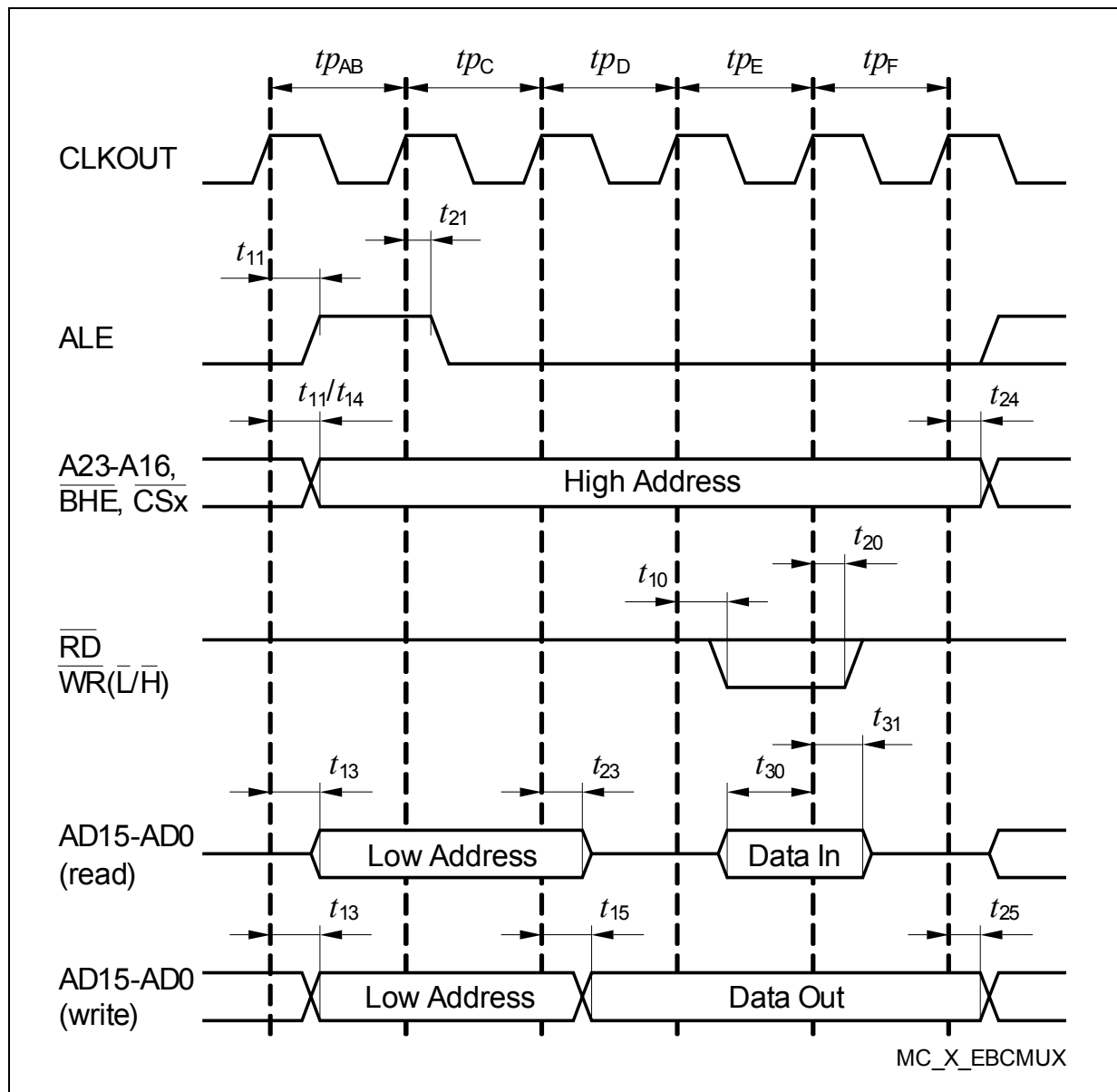


Figure 22 Multiplexed Bus Cycle

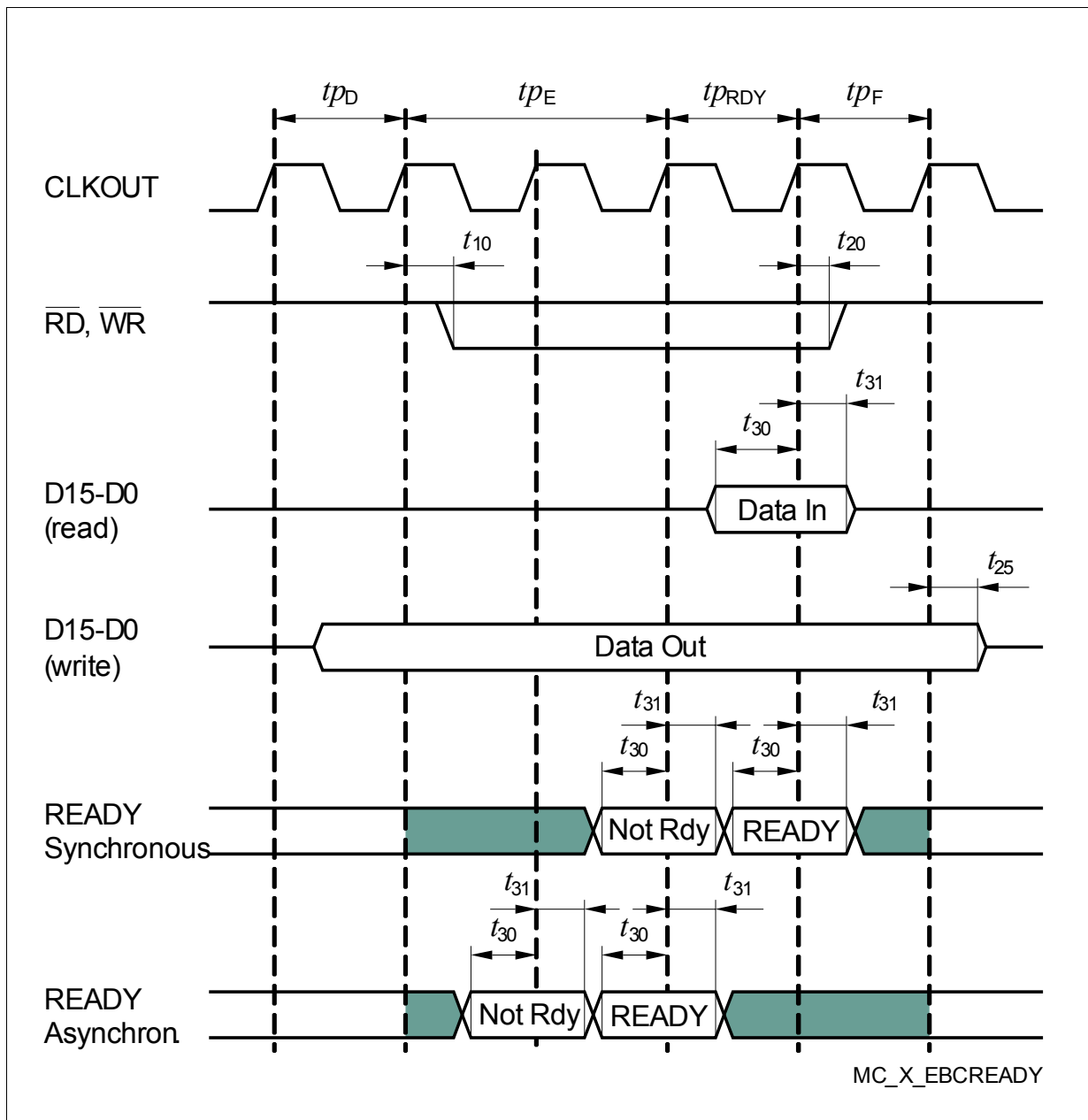
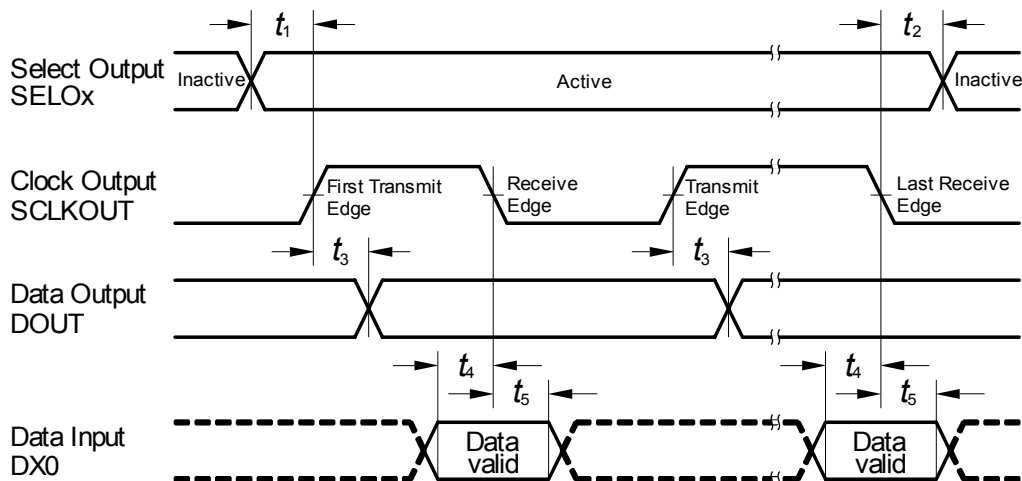


Figure 24 **READY Timing**

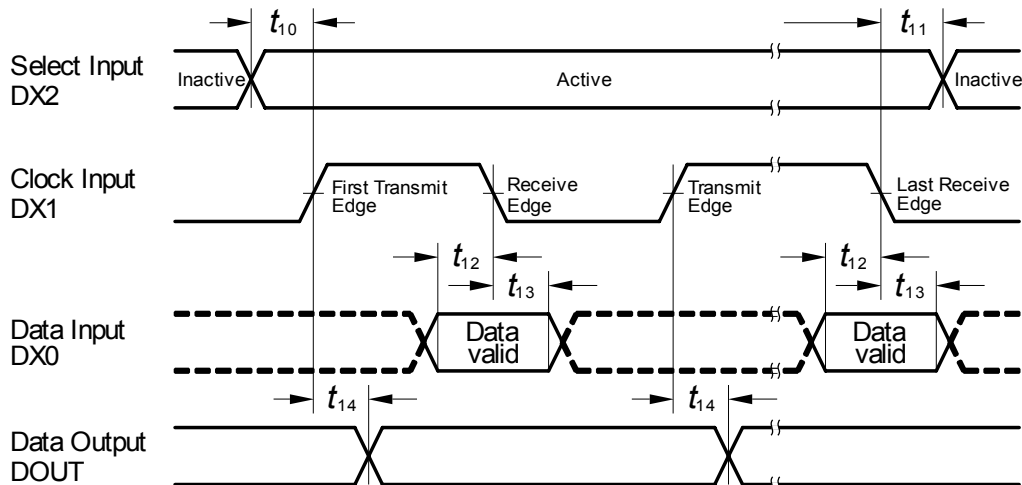
Note: If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (tp_{RDY}), sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle.

Note the different sampling points for synchronous and asynchronous READY. This example uses one mandatory waitstate (see tp_E) before the READY input value is used.

Master Mode Timing



Slave Mode Timing



Transmit Edge: with this clock edge transmit data is shifted to transmit data output

Receive Edge: with this clock edge receive data at receive data input is latched

Drawn for BRGH.SCLKCFG = 00_B. Also valid for for SCLKCFG = 01_B with inverted SCLKOUT signal

USIC_SSC_TMGX.VSD

Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.