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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164k-24f66l-ac

Summary of Features

- 2) Specific information about the on-chip Flash memory in [Table 2](#).
- 3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM (12 Kbytes for devices with 192 Kbytes of Flash).
- 4) Specific information about the available channels in [Table 3](#).
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

2 General Device Information

The XE164 series of real time signal controllers is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

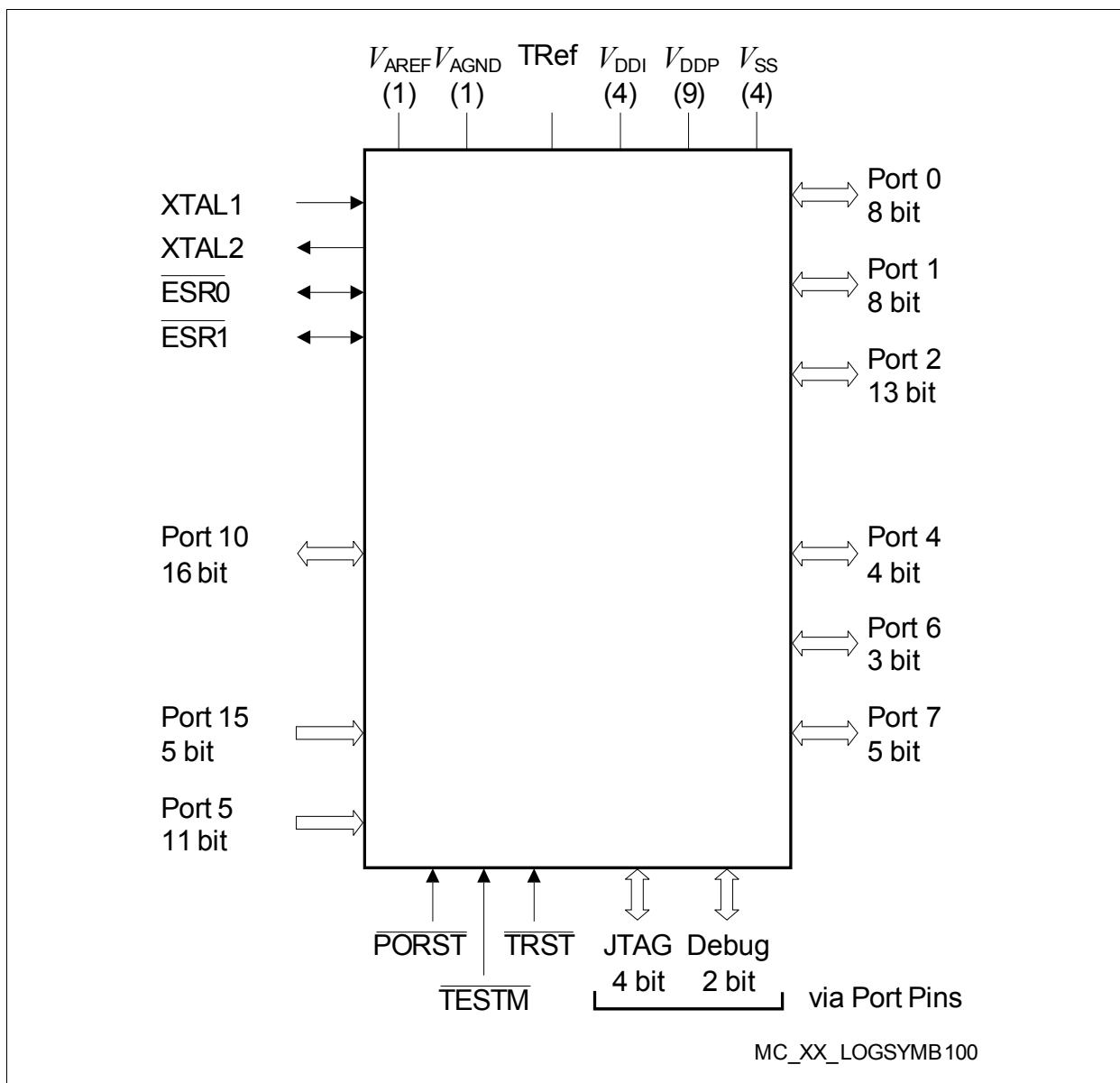


Figure 1 **Logic Symbol**

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.
	$\overline{\text{CS2}}$	OH	St/B	External Bus Interface Chip Select 2 Output
	T2IN	I	St/B	GPT1 Timer T2 Count/Gate Input
48	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
49	P4.3	O0 / I	St/B	Bit 3 of Port 4, General Purpose Input/Output
	CC2_27	O3 / I	St/B	CAPCOM2 CC27IO Capture Inp./ Compare Out.
	$\overline{\text{CS3}}$	OH	St/B	External Bus Interface Chip Select 3 Output
	RxDC2A	I	St/B	CAN Node 2 Receive Data Input
	T2EUD	I	St/B	GPT1 Timer T2 External Up/Down Control Input
53	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC60	O3 / I	St/B	CCU61 Channel 0 Input/Output
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
61	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output
	U1C0_SELO0	O1	St/B	USIC1 Channel 0 Select/Control 0 Output
	U1C1_SELO1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output
	CCU61_COUT60	O3	St/B	CCU61 Channel 0 Output
	A3	OH	St/B	External Bus Interface Address Line 3
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input
62	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC62	O2 / I	St/B	CCU60 Channel 2 Input/Output
	AD2	OH / I	St/B	External Bus Interface Address/Data Line 2
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
63	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COUT61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input
65	TRef	IO	Sp/1	Control Pin for Core Voltage Generation 2)

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P10.8	O0 / I	St/B	Bit 8 of Port 10, General Purpose Input/Output
	U0C0_MCLKOUT	O1	St/B	USIC0 Channel 0 Master Clock Output
	U0C1_SELO0	O2	St/B	USIC0 Channel 1 Select/Control 0 Output
	AD8	OH / I	St/B	External Bus Interface Address/Data Line 8
	CCU60_CCPOS1A	I	St/B	CCU60 Position Input 1
	U0C0_DX1C	I	St/B	USIC0 Channel 0 Shift Clock Input
	BRKIN_B	I	St/B	OCDS Break Signal Input
80	P10.9	O0 / I	St/B	Bit 9 of Port 10, General Purpose Input/Output
	U0C0_SELO4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_MCLKOUT	O2	St/B	USIC0 Channel 1 Master Clock Output
	AD9	OH / I	St/B	External Bus Interface Address/Data Line 9
	CCU60_CCPOS2A	I	St/B	CCU60 Position Input 2
	TCK_B	I	St/B	JTAG Clock Input
81	P1.1	O0 / I	St/B	Bit 1 of Port 1, General Purpose Input/Output
	CCU62_COUT62	O1	St/B	CCU62 Channel 2 Output
	U1C0_SELO5	O2	St/B	USIC1 Channel 0 Select/Control 5 Output
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output
	A9	OH	St/B	External Bus Interface Address Line 9
	ESR2_3	I	St/B	ESR2 Trigger Input 3
	EX1BINA	I	St/B	External Interrupt Trigger Input
	U2C1_DX0C	I	St/B	USIC2 Channel 1 Shift Data Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
93	P1.6	O0 / I	St/B	Bit 6 of Port 1, General Purpose Input/Output
	CCU62_ CC61	O1 / I	St/B	CCU62 Channel 1 Input/Output
	U1C1_ SELO2	O2	St/B	USIC1 Channel 1 Select/Control 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	A14	OH	St/B	External Bus Interface Address Line 14
	U2C0_DX0D	I	St/B	USIC2 Channel 0 Shift Data Input
94	P1.7	O0 / I	St/B	Bit 7 of Port 1, General Purpose Input/Output
	CCU62_ CC60	O1 / I	St/B	CCU62 Channel 0 Input/Output
	U1C1_ MCLKOUT	O2	St/B	USIC1 Channel 1 Master Clock Output
	U2C0_ SCLKOUT	O3	St/B	USIC2 Channel 0 Shift Clock Output
	A15	OH	St/B	External Bus Interface Address Line 15
	U2C0_DX1C	I	St/B	USIC2 Channel 0 Shift Clock Input
95	XTAL2	O	Sp/1	Crystal Oscillator Amplifier Output
96	XTAL1	I	Sp/1	Crystal Oscillator Amplifier Input To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDI1} .
97	$\overline{\text{PORST}}$	I	In/B	Power On Reset Input A low level at this pin resets the XE164 completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pullup device will hold this pin high when nothing is driving it.

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections¹⁾:

- Address Bus Width with a range of 0 ... 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes ... 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to four external $\overline{\text{CS}}$ signals (three windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.

Access to very slow memories or modules with varying access times is supported by a special 'Ready' function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

3.4 Interrupt System

With a minimum interrupt response time of $7/11^{1)}$ CPU clocks (in the case of internal program execution), the XE164 can react quickly to the occurrence of non-deterministic events.

The architecture of the XE164 supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164 has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

Each of the possible interrupt nodes has a separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield. Each node can be programmed by its related register to one of sixteen interrupt priority levels. Once accepted by the CPU, an interrupt service can only be interrupted by a higher-priority service request. For standard interrupt processing, each possible interrupt node has a dedicated vector location.

Fast external interrupt inputs can service external interrupts with high-precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 6 shows all of the possible XE164 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes) may be used to generate software-controlled interrupt requests by setting the respective interrupt request bit (xIR).

1) Depending if the jump cache is used or not.

Functional Description

Table 6 XE164 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location¹⁾	Trap Number
CAN Request 1	CAN_1IC	xx'0104 _H	41 _H / 65 _D
CAN Request 2	CAN_2IC	xx'0108 _H	42 _H / 66 _D
CAN Request 3	CAN_3IC	xx'010C _H	43 _H / 67 _D
CAN Request 4	CAN_4IC	xx'0110 _H	44 _H / 68 _D
CAN Request 5	CAN_5IC	xx'0114 _H	45 _H / 69 _D
CAN Request 6	CAN_6IC	xx'0118 _H	46 _H / 70 _D
CAN Request 7	CAN_7IC	xx'011C _H	47 _H / 71 _D
CAN Request 8	CAN_8IC	xx'0120 _H	48 _H / 72 _D
CAN Request 9	CAN_9IC	xx'0124 _H	49 _H / 73 _D
CAN Request 10	CAN_10IC	xx'0128 _H	4A _H / 74 _D
CAN Request 11	CAN_11IC	xx'012C _H	4B _H / 75 _D
CAN Request 12	CAN_12IC	xx'0130 _H	4C _H / 76 _D
CAN Request 13	CAN_13IC	xx'0134 _H	4D _H / 77 _D
CAN Request 14	CAN_14IC	xx'0138 _H	4E _H / 78 _D
CAN Request 15	CAN_15IC	xx'013C _H	4F _H / 79 _D
USIC0 Cannel 0, Request 0	U0C0_0IC	xx'0140 _H	50 _H / 80 _D
USIC0 Cannel 0, Request 1	U0C0_1IC	xx'0144 _H	51 _H / 81 _D
USIC0 Cannel 0, Request 2	U0C0_2IC	xx'0148 _H	52 _H / 82 _D
USIC0 Cannel 1, Request 0	U0C1_0IC	xx'014C _H	53 _H / 83 _D
USIC0 Cannel 1, Request 1	U0C1_1IC	xx'0150 _H	54 _H / 84 _D
USIC0 Cannel 1, Request 2	U0C1_2IC	xx'0154 _H	55 _H / 85 _D
USIC1 Cannel 0, Request 0	U1C0_0IC	xx'0158 _H	56 _H / 86 _D
USIC1 Cannel 0, Request 1	U1C0_1IC	xx'015C _H	57 _H / 87 _D
USIC1 Cannel 0, Request 2	U1C0_2IC	xx'0160 _H	58 _H / 88 _D
USIC1 Cannel 1, Request 0	U1C1_0IC	xx'0164 _H	59 _H / 89 _D
USIC1 Cannel 1, Request 1	U1C1_1IC	xx'0168 _H	5A _H / 90 _D
USIC1 Cannel 1, Request 2	U1C1_2IC	xx'016C _H	5B _H / 91 _D
USIC2 Cannel 0, Request 0	U2C0_0IC	xx'0170 _H	5C _H / 92 _D
USIC2 Cannel 0, Request 1	U2C0_1IC	xx'0174 _H	5D _H / 93 _D
USIC2 Cannel 0, Request 2	U2C0_2IC	xx'0178 _H	5E _H / 94 _D

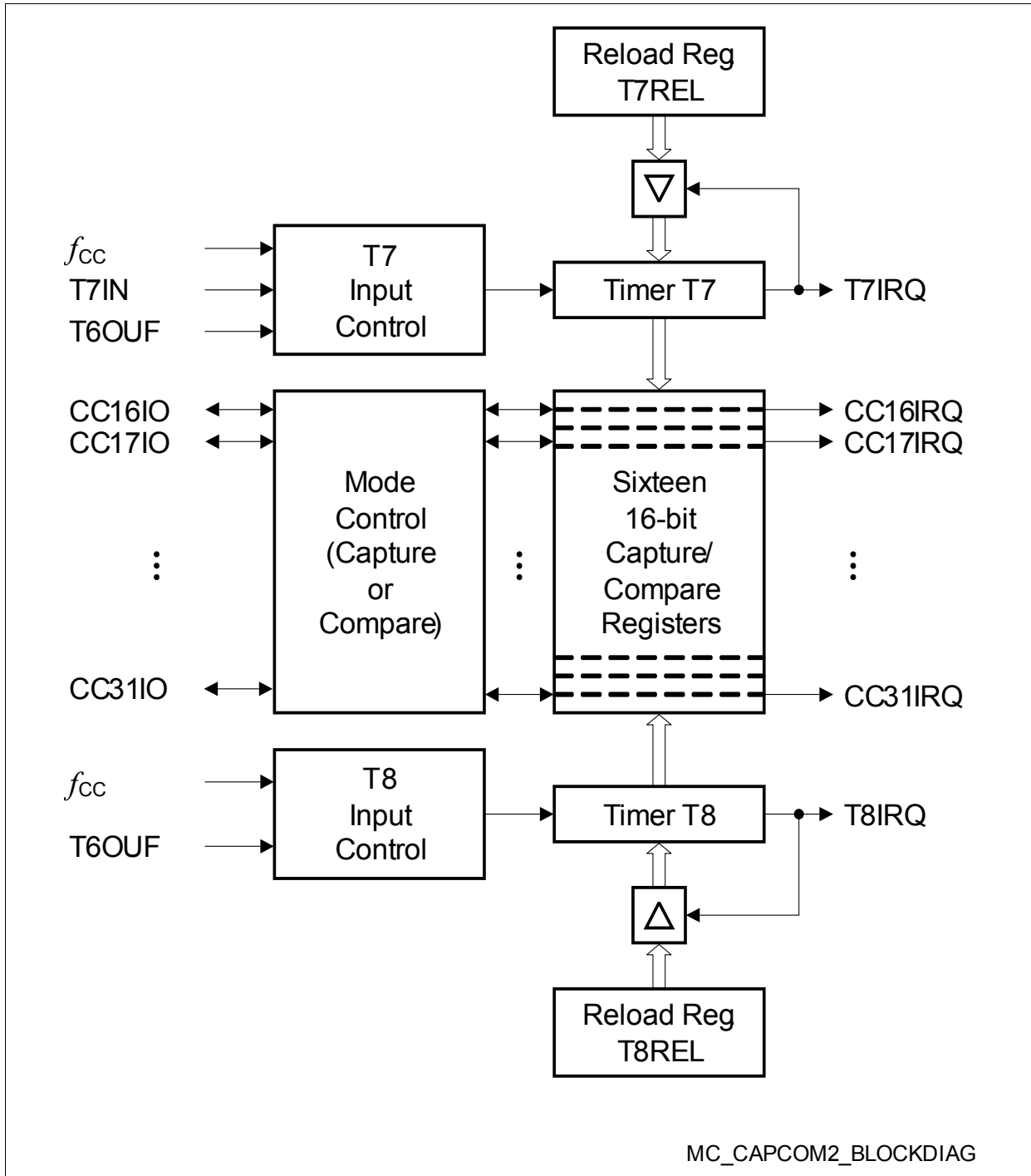


Figure 5 CAPCOM2 Unit Block Diagram

3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes each timer has one associated port pin (TxIN¹⁾) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD¹⁾), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers¹⁾ can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL.

1) Exception: Timer T4 is not connected to pins.

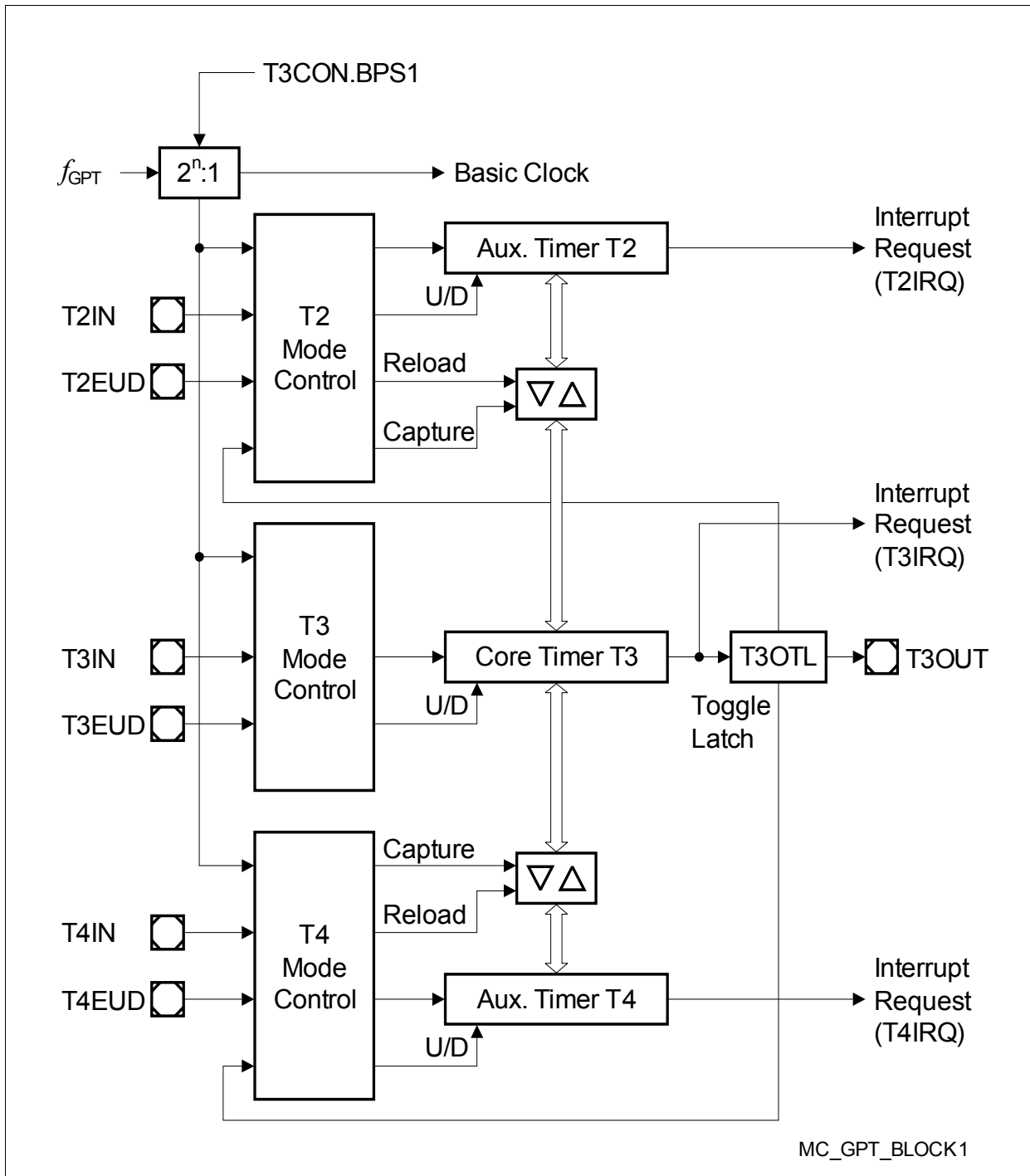


Figure 7 Block Diagram of GPT1

3.11 Universal Serial Interface Channel Modules (USIC)

The XE164 includes up to three USIC modules (USIC0, USIC1, USIC2), each providing two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

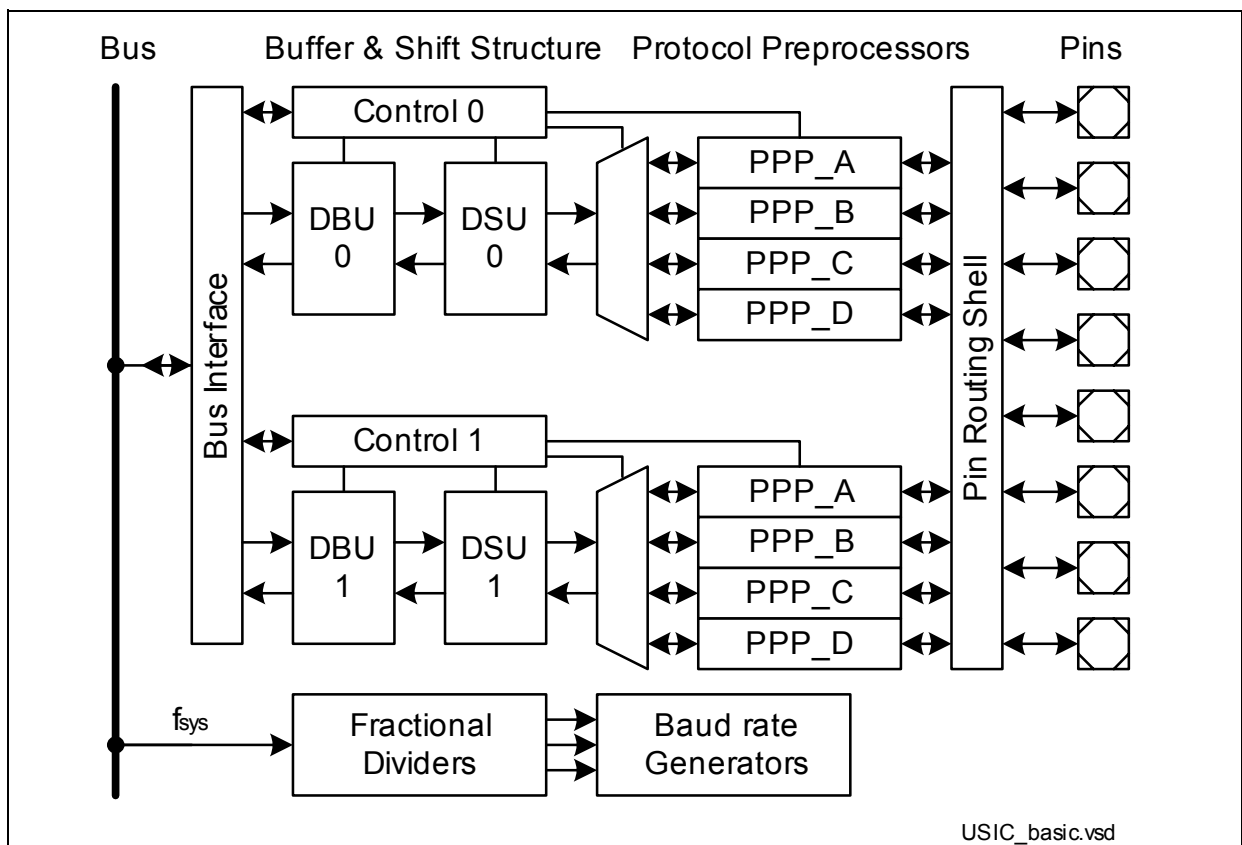


Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

Variable Memory Cycles

External bus cycles of the XE164 are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 28 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 ... 2 TCS) can be extended by 0 ... 3 TCS if the address window is changed	tpAB	1 ... 2 (5)	TCS
Command delay phase	tpC	0 ... 3	TCS
Write Data setup/MUX Tristate phase	tpD	0 ... 1	TCS
Access phase	tpE	1 ... 32	TCS
Address/Write Data hold phase	tpF	0 ... 3	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Timing values are listed in [Table 29](#) and [Table 30](#). The shaded parameters have been verified by characterization. They are not subject to production test.

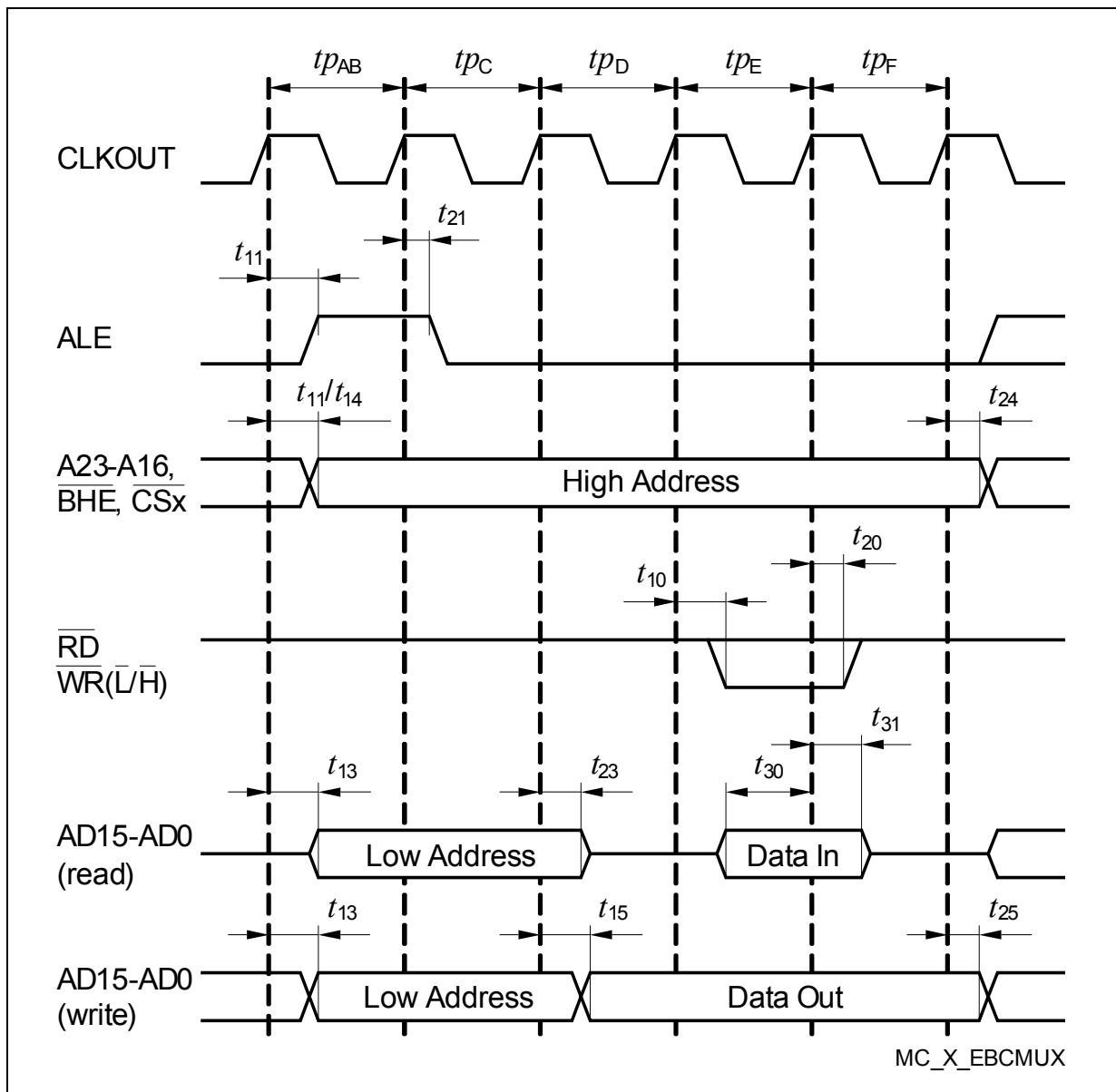


Figure 22 Multiplexed Bus Cycle

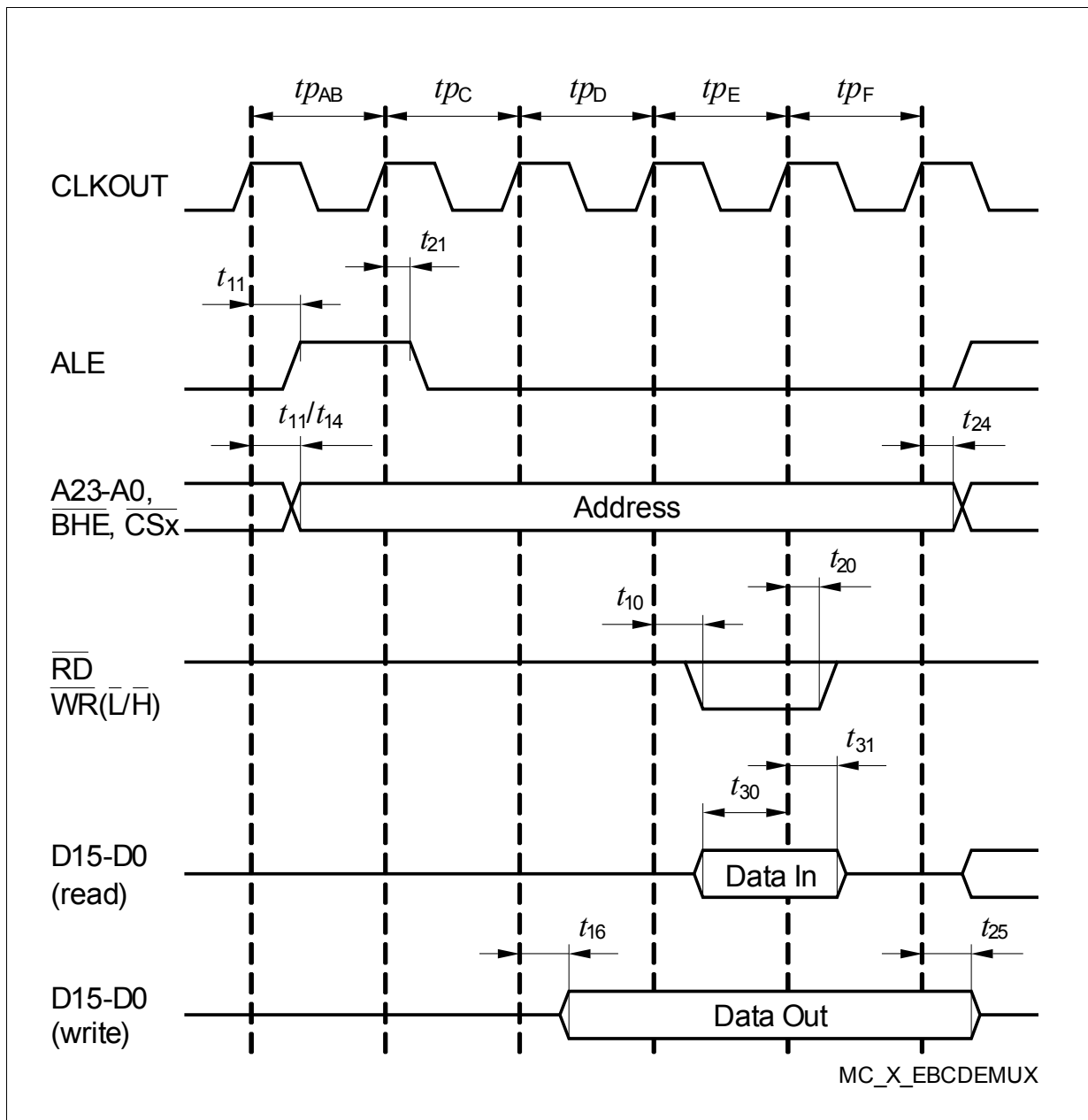


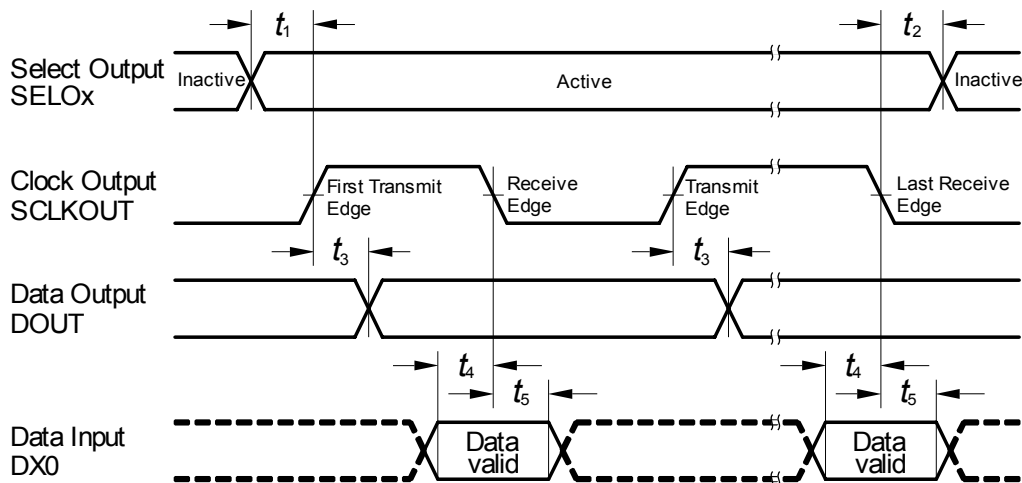
Figure 23 Demultiplexed Bus Cycle

Table 32 SSC Master/Slave Mode Timing for Lower Voltage Range
(Operating Conditions apply), $C_L = 50 \text{ pF}$

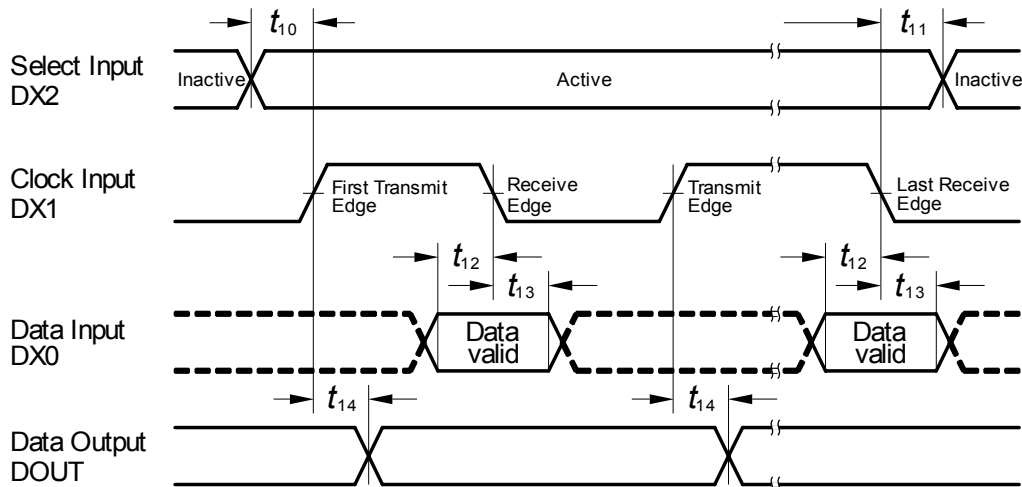
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	—	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$0.5 \times t_{\text{BIT}}$	—	3)	ns	2)
Transmit data output valid time	t_3 CC	-13	—	16	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	48	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-11	—	—	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	12	—	—	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	8	—	—	ns	4)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	12	—	—	ns	4)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	8	—	—	ns	4)
Data output DOUT valid time	t_{14} CC	11	—	44	ns	4)

- 1) The maximum value further depends on the settings for the slave select output leading delay.
- 2) $t_{\text{SYS}} = 1/f_{\text{SYS}} (= 12.5 \text{ ns @ } 80 \text{ MHz})$
- 3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.
- 4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Master Mode Timing



Slave Mode Timing



Transmit Edge: with this clock edge transmit data is shifted to transmit data output

Receive Edge: with this clock edge receive data at receive data input is latched

Drawn for BRGH.SCLKCFG = 00_B. Also valid for for SCLKCFG = 01_B with inverted SCLKOUT signal

USIC_SSC_TMGX.VSD

Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

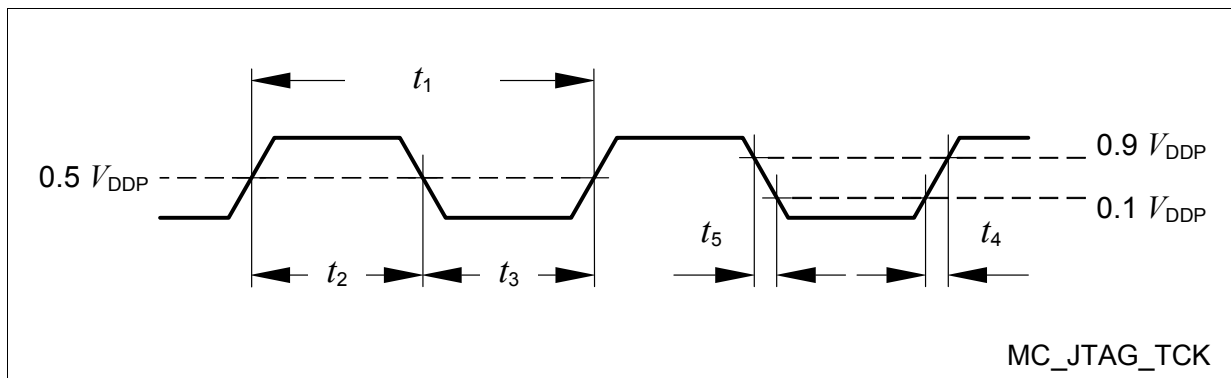


Figure 26 Test Clock Timing (TCK)

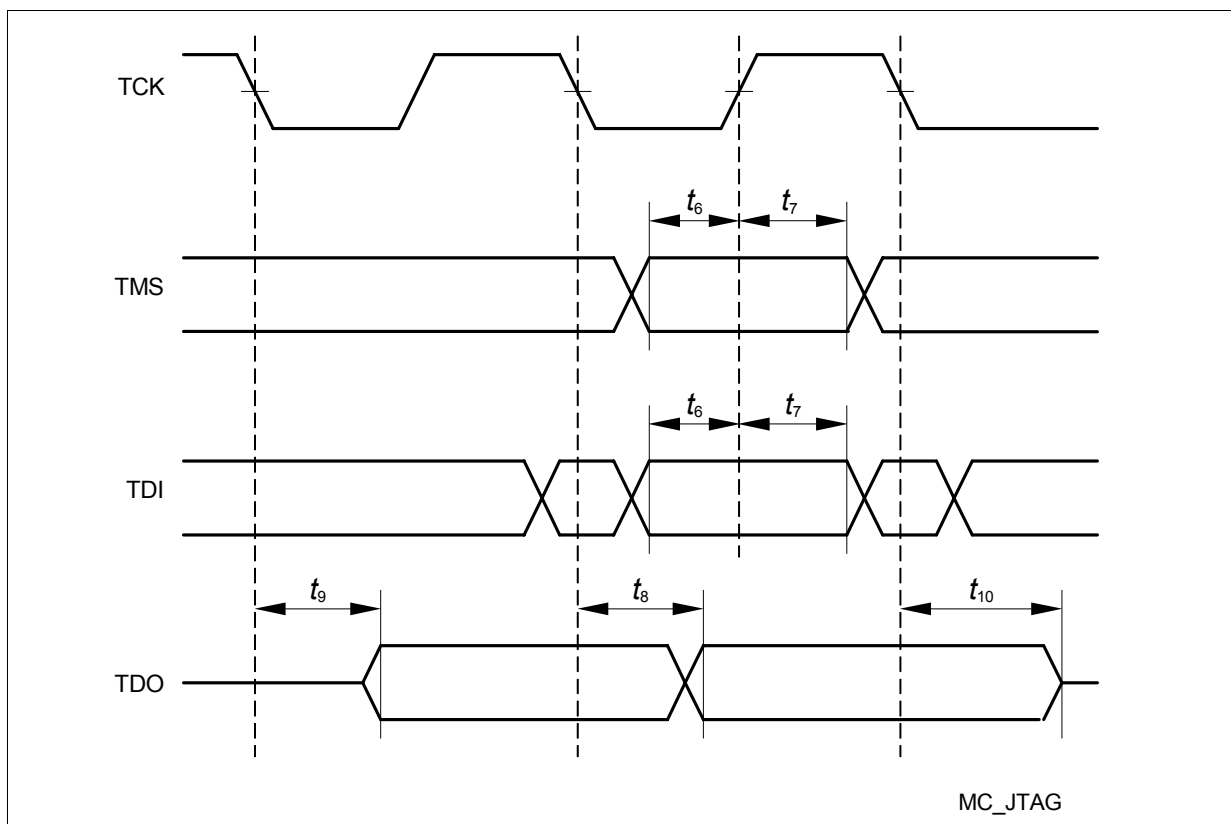


Figure 27 JTAG Timing

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