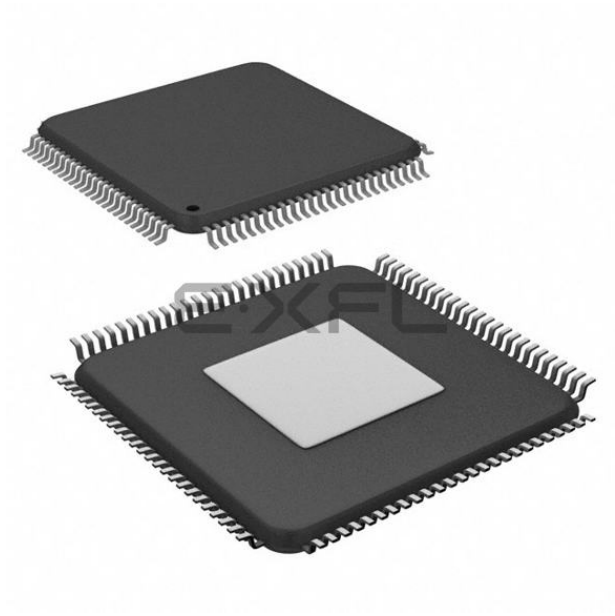
Infineon Technologies - SAF-XE164K-72F66L AC Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164k-72f66l-ac

Notes to Pin Definitions

1. ***Ctrl.**: The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bitfield PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.*
   Output signal OH is controlled by hardware.
2. ***Type**: Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).*

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	**Bit 2 of Port 7, General Purpose Input/Output**
	EMUX0	O1	St/B	**External Analog MUX Control Output 0 (ADC1)**
	CCU62_ CCPOS0A	I	St/B	**CCU62 Position Input 0**
	TDI_C	I	St/B	**JTAG Test Data Input**
5	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE164's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
6	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT1 Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT2 Timer T6 Toggle Latch Output**
	TDO_A	OH	St/B	**JTAG Test Data Output**
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
54	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_ SELO0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_ SELO1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	A20	OH	St/B	**External Bus Interface Address Line 20**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
55	P0.1	O0 / I	St/B	**Bit 1 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_ CC61	O3 / I	St/B	**CCU61 Channel 1 Input/Output**
	A1	OH	St/B	**External Bus Interface Address Line 1**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
56	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_ SCLKOUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output** 1)
	CC2_21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	A21	OH	DP/B	**External Bus Interface Address Line 21**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**
57	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	A22	OH	St/B	**External Bus Interface Address Line 22**
	CLKIN1	I	St/B	**Clock Signal Input**
	TCK_A	I	St/B	**JTAG Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
66	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_ SELO3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	A23	OH	St/B	**External Bus Interface Address Line 23**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPIN	I	St/B	**GPT2 Register CAPREL Capture Input**
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_ COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / I	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_ SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_ SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_ COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_ SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_ COUT61	O2	St/B	**CCU60 Channel 1 Output**
	AD4	OH / I	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**

3.7 Capture/Compare Units CCU6x

The XE164 features up to three CCU6 units (CCU60, CCU61, CCU62).

The CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

3.10 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 11 + 5 multiplexed input channels and a sample and hold circuit have been integrated on-chip. They use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically.

For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XE164 support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features, such as limit checking or result accumulation, reduce the number of required CPU access operations allowing the precise evaluation of analoginputs (high conversion rate) even at a low CPU speed.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately with registers P5_DIDIS and P15_DIDIS (Port x Digital Input Disable).

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to four independent CAN nodes
- 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.16 Instruction Set Summary

Table 10 lists the instructions of the XE164.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 10 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

4.2.3 Power Consumption

The power consumed by the XE164 depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S (**Table 16**) and leakage current I_{LK} (**Table 17**) must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
*After a power reset, the decoupling capacitors for V_{DDI} are charged with the maximum possible current, see parameter I_{CC} in **Table 20**.*

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Table 18 A/D Converter Characteristics (cont'd)
(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Switched capacitance of the reference input	C_{AREFS}	CC	–	7	pF	6)7)
Resistance of the reference input path	R_{AREF}	CC	–	2	kΩ	6)7)

1) TUE is tested at V_{AREFx} = V_{DDPA}, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.
2) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{ADCI} depend on programming and are found in **Table 19**.
5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.
6) Not subject to production test - verified by design/characterization.
7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

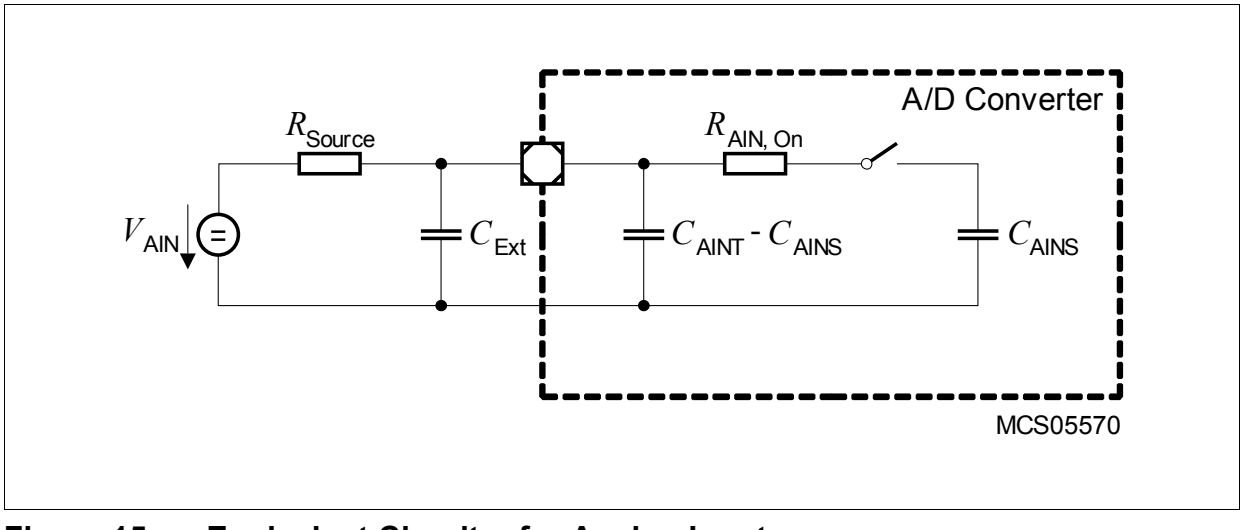

Figure 15 Equivalent Circuitry for Analog Inputs

4.5 Flash Memory Parameters

The XE164 is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE164's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 23 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Programming time per 128-byte page	t_{PR}	–	3[1)]	3.5	ms	ms
Erase time per sector/page	t_{ER}	–	4[1)]	5	ms	ms
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles
Flash erase endurance for user sectors[2)]	N_{ER}	15,000	–	–	cycles	Data retention time 5 years
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	Data retention time 20 years
Drain disturb limit	N_{DD}	64	–	–	cycles	3)

1) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.
In the XE164 erased areas must be programmed completely (with actual code/data or dummy values) before that area is read.

2) A maximum of 64 Flash sectors can be cycled 15,000 times. For all other sectors the limit is 1,000 cycles.

3) This parameter limits the number of subsequent programming operations within a physical sector. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated.

Access to the XE164 Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

Table 24 Flash Access Waitstates

Required Waitstates	System Frequency Range
4 WS (WSFLASH = 100_B)	$f_{SYS} \leq f_{SYSmax}$
3 WS (WSFLASH = 011_B)	$f_{SYS} \leq 17$ MHz
2 WS (WSFLASH = 010_B)	$f_{SYS} \leq 13$ MHz
1 WS (WSFLASH = 001_B)	$f_{SYS} \leq 8$ MHz
0 WS (WSFLASH = 000_B)	Forbidden! Must not be selected!

Note: The maximum achievable system frequency is limited by the properties of the respective derivative.

4.6.4 External Bus Timing

The following parameters specify the behavior of the XE164 bus interface.

Table 27 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit	Note / Test Condition
			Min.	Max.		
CLKOUT cycle time	t_5	CC	40/25/12.5[1)]		ns	
CLKOUT high time	t_6	CC	3	–	ns	
CLKOUT low time	t_7	CC	3	–	ns	
CLKOUT rise time	t_8	CC	–	3	ns	
CLKOUT fall time	t_9	CC	–	3	ns	

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{SYS} = 25/40/80 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

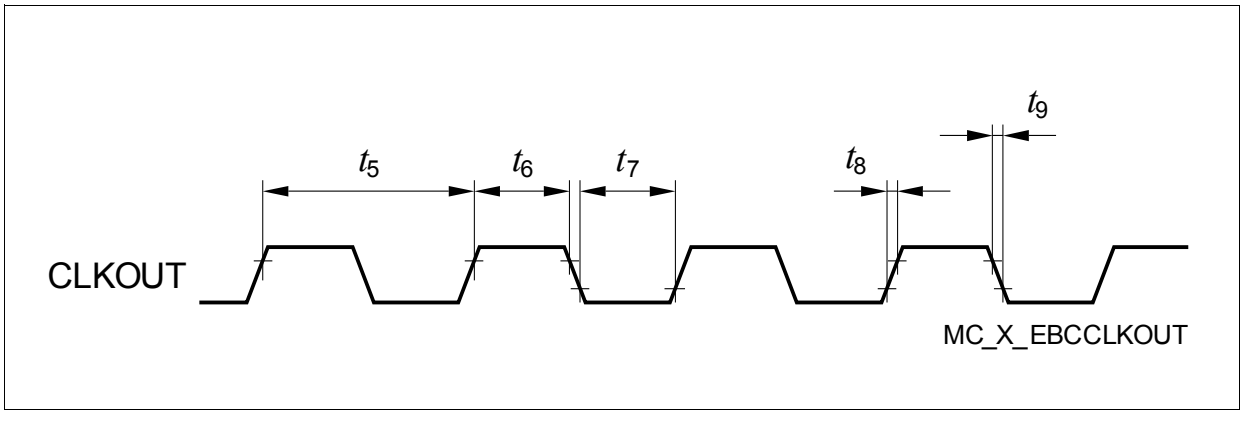

Figure 21 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

Variable Memory Cycles

External bus cycles of the XE164 are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 28 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 … 2 TCS) can be extended by 0 … 3 TCS if the address window is changed	tpAB	1 … 2 (5)	TCS
Command delay phase	tpC	0 … 3	TCS
Write Data setup/MUX Tristate phase	tpD	0 … 1	TCS
Access phase	tpE	1 … 32	TCS
Address/Write Data hold phase	tpF	0 … 3	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Timing values are listed in **Table 29** and **Table 30**. The shaded parameters have been verified by characterization. They are not subject to production test.

Table 29 External Bus Cycle Timing for Upper Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: RD, WR(L/H)	t_{10} CC	–		13	ns	
Output valid delay for: BHE, ALE	t_{11} CC	–		13	ns	
Output valid delay for: A23 … A16, A15 … A0 (on P0/P1)	t_{12} CC	–		14	ns	
Output valid delay for: A15 … A0 (on P2/P10)	t_{13} CC	–		14	ns	
Output valid delay for: CS	t_{14} CC	–		13	ns	
Output valid delay for: D15 … D0 (write data, MUX-mode)	t_{15} CC	–		14	ns	
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	t_{16} CC	–		14	ns	
Output hold time for: RD, WR(L/H)	t_{20} CC	0		8	ns	
Output hold time for: BHE, ALE	t_{21} CC	0		8	ns	
Output hold time for: A23 … A16, A15 … A0 (on P2/P10)	t_{23} CC	0		8	ns	
Output hold time for: CS	t_{24} CC	0		8	ns	
Output hold time for: D15 … D0 (write data)	t_{25} CC	0		8	ns	
Input setup time for: READY, D15 … D0 (read data)	t_{30} SR	18		–	ns	
Input hold time for: READY, D15 … D0 (read data)[1)]	t_{31} SR	-4		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

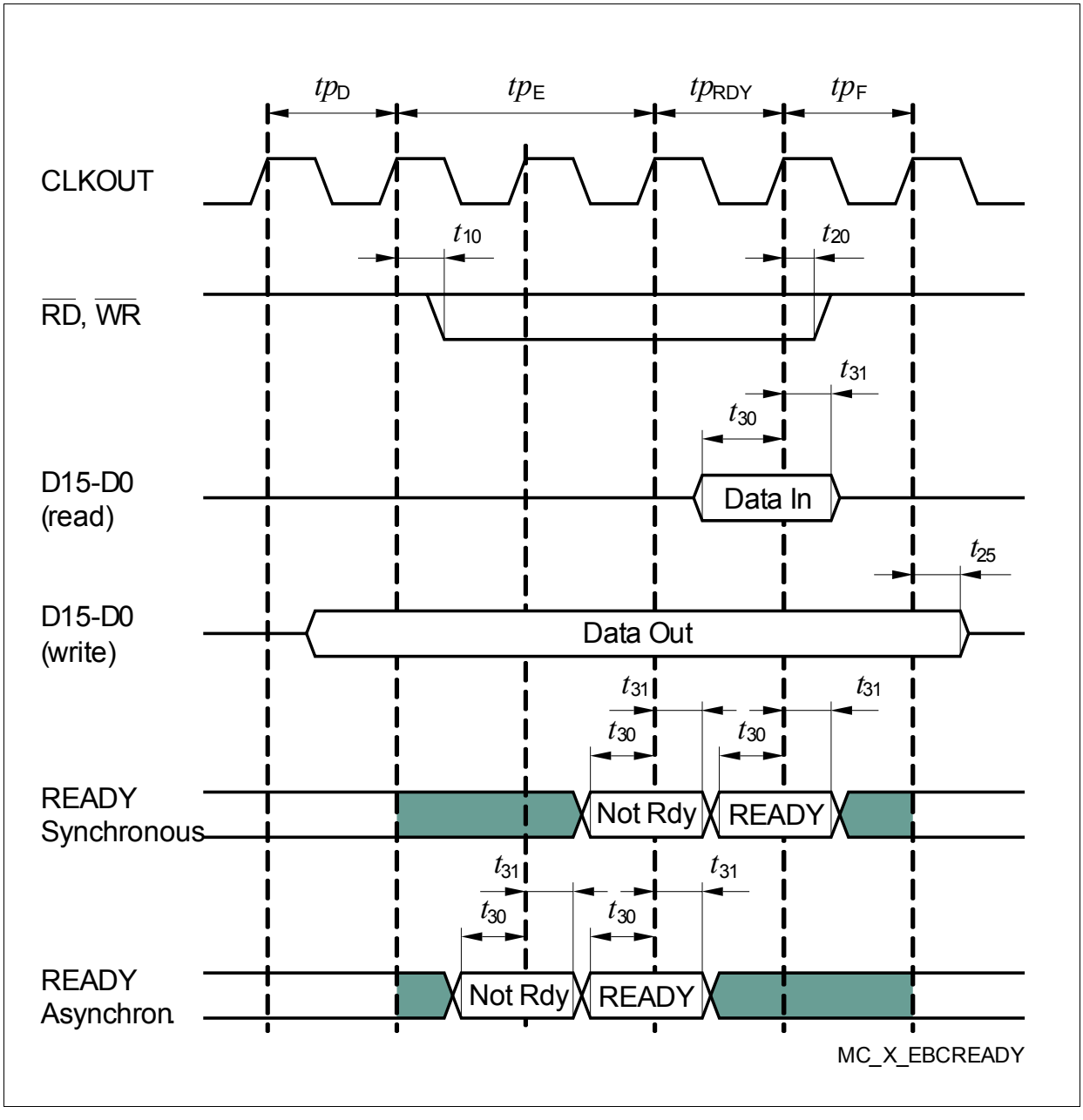

Figure 24 READY Timing

Note: If the READY input is sampled inactive at the indicated sampling point (“Not Rdy”) a READY-controlled waitstate is inserted (tpRDY),
sampling the READY input active at the indicated sampling point (“Ready”) terminates the currently running bus cycle.
Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see tpE) before the READY input value is used.

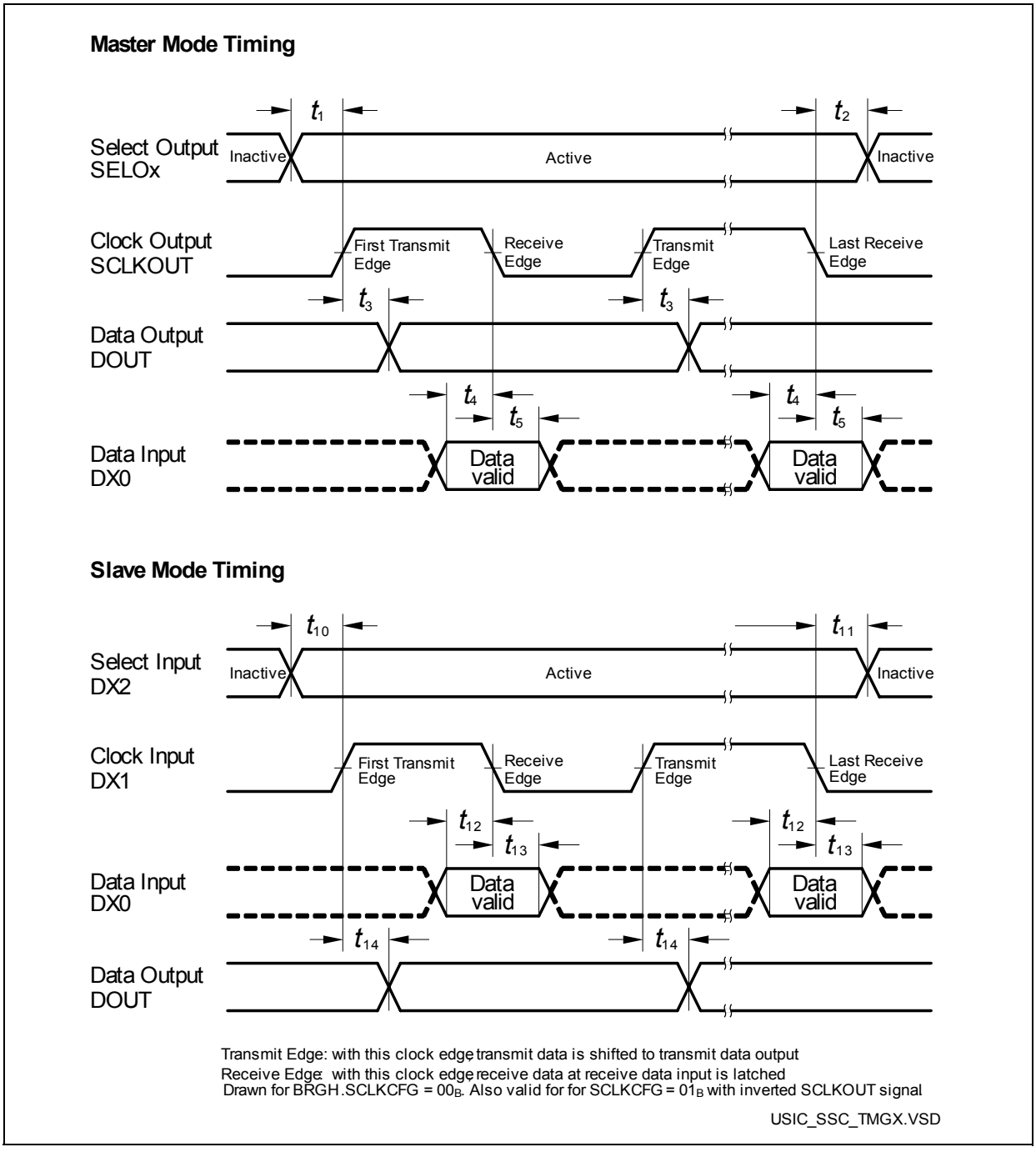

Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

5 Package and Reliability

In addition to the electrical parameters, the following specifcations ensure proper integration of the XE164 into the target system.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 34 Package Parameters (PG-LQFP-100-3)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	6.2 × 6.2	mm	–
Power Dissipation	P_{DISS}	–	1.0	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	49	K/W	No thermal via[1)]
			37	K/W	4-layer, no pad[2)]
			22	K/W	4-layer, pad[3)]

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) or a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

5.2 Thermal Considerations

When operating the XE164 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 125 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (see **Section 4.2.3**).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

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