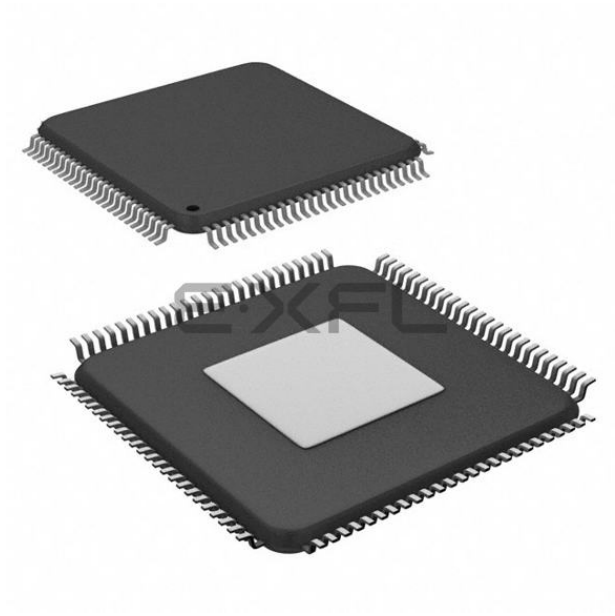
# Infineon Technologies - XE164F72F66LACFXQMA1 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 66MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 75 |
| Program Memory Size | 576KB (576K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 50K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-100-3 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xe164f72f66lacfxqma1 |

The XE164 types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

**Table 2 Flash Memory Allocation**

| Total Flash Size | Flash Area A[1)] | Flash Area B | Flash Area C |
|---|---|---|---|
| 768 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $CB'FFFF_H$ | n.a. |
| 576 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $C8'FFFF_H$ | n.a. |
| 384 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $C5'FFFF_H$ | n.a. |
| 192 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $C1'FFFF_H$ | $C4'0000_H$ … $C4'FFFF_H$ |

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE164 types are offered with different interface options. **Table 3** lists the available channels for each option.

**Table 3 Interface Channel Association**

| Total Number | Available Channels |
|---|---|
| 11 ADC0 channels | CH0, CH2 … CH5, CH8 … CH11, CH13, CH15 |
| 6 ADC0 channels | CH0, CH2, CH3, CH4, CH5, CH8 |
| 5 ADC1 channels | CH0, CH2, CH4, CH5, CH6 |
| 4 CAN nodes | CAN0, CAN1, CAN2, CAN3 |
| 2 CAN nodes | CAN0, CAN1 |
| 6 serial channels | U0C0, U0C1, U1C0, U1C1, U2C0, U2C1 |
| 4 serial channels | U0C0, U0C1, U1C0, U1C1 |

# 2 General Device Information

The XE164 series of real time signal controllers is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

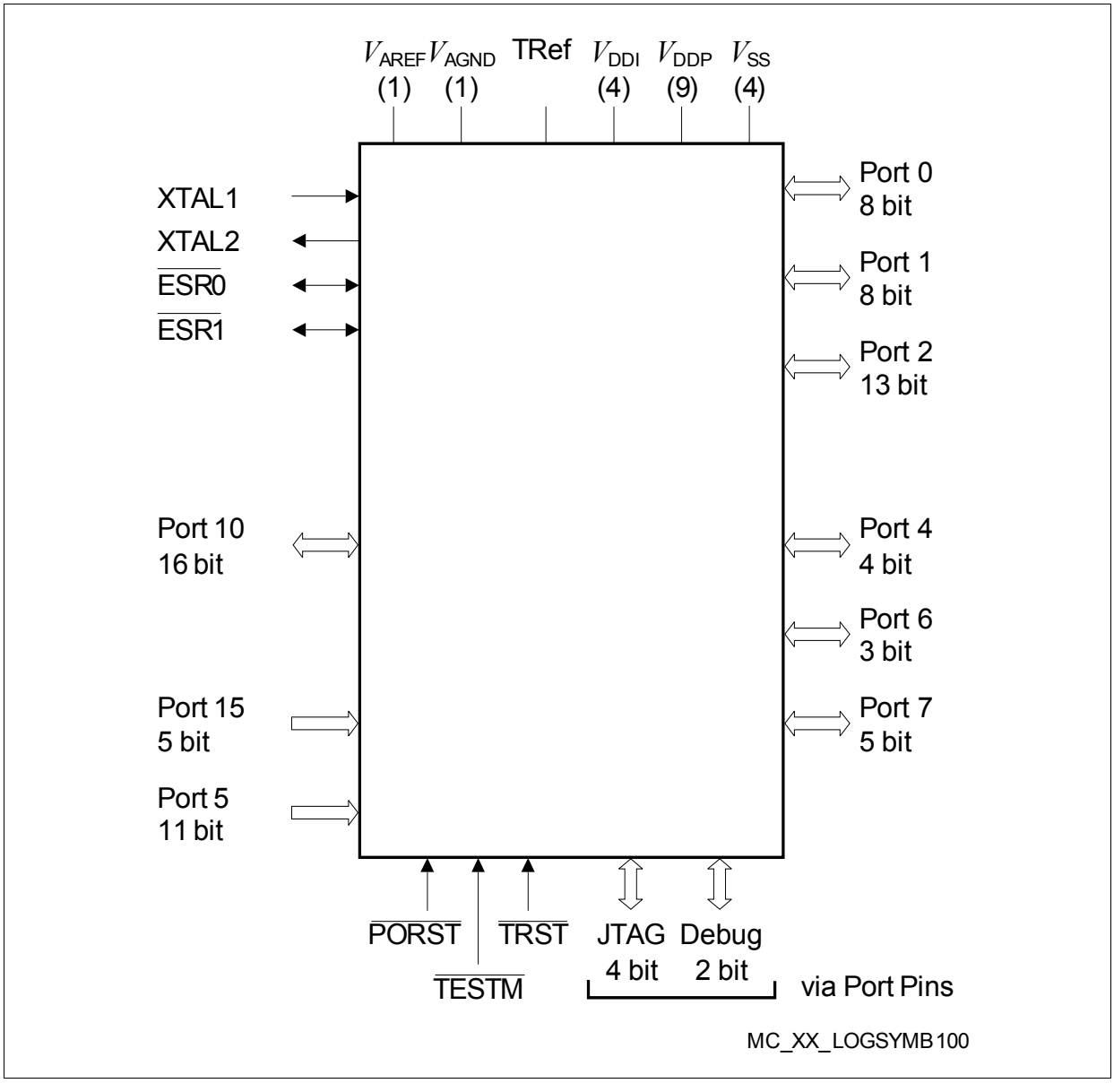


**Figure 1 Logic Symbol**

### Notes to Pin Definitions

1. ***Ctrl.**: The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bitfield PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.*
   *Output signal OH is controlled by hardware.*
2. ***Type**: Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).*

**Table 4 Pin Definitions and Functions**

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 3 | $\overline{\text{TESTM}}$ | I | In/B | **Testmode Enable**<br>Enables factory test modes, must be held HIGH for normal operation (connect to $V_{DDPB}$).<br>An internal pullup device will hold this pin high when nothing is driving it. |
| 4 | P7.2 | O0 / I | St/B | **Bit 2 of Port 7, General Purpose Input/Output** |
| | EMUX0 | O1 | St/B | **External Analog MUX Control Output 0 (ADC1)** |
| | CCU62_ CCPOS0A | I | St/B | **CCU62 Position Input 0** |
| | TDI_C | I | St/B | **JTAG Test Data Input** |
| 5 | $\overline{\text{TRST}}$ | I | In/B | **Test-System Reset Input**<br>For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE164's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.<br>An internal pulldown device will hold this pin low when nothing is driving it. |
| 6 | P7.0 | O0 / I | St/B | **Bit 0 of Port 7, General Purpose Input/Output** |
| | T3OUT | O1 | St/B | **GPT1 Timer T3 Toggle Latch Output** |
| | T6OUT | O2 | St/B | **GPT2 Timer T6 Toggle Latch Output** |
| | TDO_A | OH | St/B | **JTAG Test Data Output** |
| | ESR2_1 | I | St/B | **ESR2 Trigger Input 1** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 12 | P6.1 | O0 / I | St/A | **Bit 1 of Port 6, General Purpose Input/Output** |
| | EMUX1 | O1 | St/A | **External Analog MUX Control Output 1 (ADC0)** |
| | T3OUT | O2 | St/A | **GPT1 Timer T3 Toggle Latch Output** |
| | U1C1_DOUT | O3 | St/A | **USIC1 Channel 1 Shift Data Output** |
| | ADCx_ REQTRyC | I | St/A | **External Request Trigger Input for ADC0/1** |
| 13 | P6.2 | O0 / I | St/A | **Bit 2 of Port 6, General Purpose Input/Output** |
| | EMUX2 | O1 | St/A | **External Analog MUX Control Output 2 (ADC0)** |
| | T6OUT | O2 | St/A | **GPT2 Timer T6 Toggle Latch Output** |
| | U1C1_ SCLKOUT | O3 | St/A | **USIC1 Channel 1 Shift Clock Output** |
| | U1C1_DX1C | I | St/A | **USIC1 Channel 1 Shift Clock Input** |
| 15 | P15.0 | I | In/A | **Bit 0 of Port 15, General Purpose Input** |
| | ADC1_CH0 | I | In/A | **Analog Input Channel 0 for ADC1** |
| 16 | P15.2 | I | In/A | **Bit 2 of Port 15, General Purpose Input** |
| | ADC1_CH2 | I | In/A | **Analog Input Channel 2 for ADC1** |
| | T5IN | I | In/A | **GPT2 Timer T5 Count/Gate Input** |
| 17 | P15.4 | I | In/A | **Bit 4 of Port 15, General Purpose Input** |
| | ADC1_CH4 | I | In/A | **Analog Input Channel 4 for ADC1** |
| | T6IN | I | In/A | **GPT2 Timer T6 Count/Gate Input** |
| 18 | P15.5 | I | In/A | **Bit 5 of Port 15, General Purpose Input** |
| | ADC1_CH5 | I | In/A | **Analog Input Channel 5 for ADC1** |
| | T6EUD | I | In/A | **GPT2 Timer T6 External Up/Down Control Input** |
| 19 | P15.6 | I | In/A | **Bit 6 of Port 15, General Purpose Input** |
| | ADC1_CH6 | I | In/A | **Analog Input Channel 6 for ADC1** |
| 20 | $V_{AREF}$ | - | PS/A | **Reference Voltage for A/D Converters ADC0/1** |
| 21 | $V_{AGND}$ | - | PS/A | **Reference Ground for A/D Converters ADC0/1** |
| 22 | P5.0 | I | In/A | **Bit 0 of Port 5, General Purpose Input** |
| | ADC0_CH0 | I | In/A | **Analog Input Channel 0 for ADC0** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 47 | P4.2 | O0 / I | St/B | **Bit 2 of Port 4, General Purpose Input/Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CC2_26 | O3 / I | St/B | **CAPCOM2 CC26IO Capture Inp./ Compare Out.** |
| | $\overline{CS2}$ | OH | St/B | **External Bus Interface Chip Select 2 Output** |
| | T2IN | I | St/B | **GPT1 Timer T2 Count/Gate Input** |
| 48 | P2.6 | O0 / I | St/B | **Bit 6 of Port 2, General Purpose Input/Output** |
| | U0C0_ SELO0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | U0C1_ SELO1 | O2 | St/B | **USIC0 Channel 1 Select/Control 1 Output** |
| | CC2_19 | O3 / I | St/B | **CAPCOM2 CC19IO Capture Inp./ Compare Out.** |
| | A19 | OH | St/B | **External Bus Interface Address Line 19** |
| | U0C0_DX2D | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | RxDC0D | I | St/B | **CAN Node 0 Receive Data Input** |
| 49 | P4.3 | O0 / I | St/B | **Bit 3 of Port 4, General Purpose Input/Output** |
| | CC2_27 | O3 / I | St/B | **CAPCOM2 CC27IO Capture Inp./ Compare Out.** |
| | $\overline{CS3}$ | OH | St/B | **External Bus Interface Chip Select 3 Output** |
| | RxDC2A | I | St/B | **CAN Node 2 Receive Data Input** |
| | T2EUD | I | St/B | **GPT1 Timer T2 External Up/Down Control Input** |
| 53 | P0.0 | O0 / I | St/B | **Bit 0 of Port 0, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | CCU61_ CC60 | O3 / I | St/B | **CCU61 Channel 0 Input/Output** |
| | A0 | OH | St/B | **External Bus Interface Address Line 0** |
| | U1C0_DX0A | I | St/B | **USIC1 Channel 0 Shift Data Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 79 | P10.8 | O0 / I | St/B | **Bit 8 of Port 10, General Purpose Input/Output** |
| | U0C0_ MCLKOUT | O1 | St/B | **USIC0 Channel 0 Master Clock Output** |
| | U0C1_ SELO0 | O2 | St/B | **USIC0 Channel 1 Select/Control 0 Output** |
| | AD8 | OH / I | St/B | **External Bus Interface Address/Data Line 8** |
| | CCU60_ CCPOS1A | I | St/B | **CCU60 Position Input 1** |
| | U0C0_DX1C | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | $\overline{\text{BRKIN\_B}}$ | I | St/B | **OCDS Break Signal Input** |
| 80 | P10.9 | O0 / I | St/B | **Bit 9 of Port 10, General Purpose Input/Output** |
| | U0C0_ SELO4 | O1 | St/B | **USIC0 Channel 0 Select/Control 4 Output** |
| | U0C1_ MCLKOUT | O2 | St/B | **USIC0 Channel 1 Master Clock Output** |
| | AD9 | OH / I | St/B | **External Bus Interface Address/Data Line 9** |
| | CCU60_ CCPOS2A | I | St/B | **CCU60 Position Input 2** |
| | TCK_B | I | St/B | **JTAG Clock Input** |
| 81 | P1.1 | O0 / I | St/B | **Bit 1 of Port 1, General Purpose Input/Output** |
| | CCU62_ COUT62 | O1 | St/B | **CCU62 Channel 2 Output** |
| | U1C0_ SELO5 | O2 | St/B | **USIC1 Channel 0 Select/Control 5 Output** |
| | U2C1_DOUT | O3 | St/B | **USIC2 Channel 1 Shift Data Output** |
| | A9 | OH | St/B | **External Bus Interface Address Line 9** |
| | ESR2_3 | I | St/B | **ESR2 Trigger Input 3** |
| | EX1BINA | I | St/B | **External Interrupt Trigger Input** |
| | U2C1_DX0C | I | St/B | **USIC2 Channel 1 Shift Data Input** |

## 3.1 Memory Subsystem and Organization

The memory space of the XE164 is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

**Table 5 XE164 Memory Map**

| Address Area | Start Loc. | End Loc. | Area Size[1)] | Notes |
|---|---|---|---|---|
| IMB register space | FF'FF00$_H$ | FF'FFFF$_H$ | 256 Bytes | – |
| Reserved (Access trap) | F0'0000$_H$ | FF'FEFF$_H$ | <1 Mbyte | Minus IMB registers |
| Reserved for EPSRAM | E9'0000$_H$ | EF'FFFF$_H$ | 448 Kbytes | Mirrors EPSRAM |
| Emulated PSRAM | E8'0000$_H$ | E8'FFFF$_H$ | 64 Kbytes | Flash timing |
| Reserved for PSRAM | E1'0000$_H$ | E7'FFFF$_H$ | 448 Kbytes | Mirrors PSRAM |
| Program SRAM | E0'0000$_H$ | E0'FFFF$_H$ | 64 Kbytes | Maximum speed |
| Reserved for pr. mem. | CC'0000$_H$ | DF'FFFF$_H$ | <1.25 Mbytes | – |
| Program Flash 2 | C8'0000$_H$ | CB'FFFF$_H$ | 256 Kbytes | – |
| Program Flash 1 | C4'0000$_H$ | C7'FFFF$_H$ | 256 Kbytes | – |
| Program Flash 0 | C0'0000$_H$ | C3'FFFF$_H$ | 256 Kbytes | 2) |
| External memory area | 40'0000$_H$ | BF'FFFF$_H$ | 8 Mbytes | – |
| Available Ext. IO area[3)] | 20'5800$_H$ | 3F'FFFF$_H$ | < 2 Mbytes | Minus USIC/CAN |
| USIC registers | 20'4000$_H$ | 20'57FF$_H$ | 6 Kbytes | Accessed via EBC |
| MultiCAN registers | 20'0000$_H$ | 20'3FFF$_H$ | 16 Kbytes | Accessed via EBC |
| External memory area | 01'0000$_H$ | 1F'FFFF$_H$ | < 2 Mbytes | Minus segment 0 |
| SFR area | 00'FE00$_H$ | 00'FFFF$_H$ | 0.5 Kbyte | – |
| Dual-Port RAM | 00'F600$_H$ | 00'FDFF$_H$ | 2 Kbytes | – |
| Reserved for DPRAM | 00'F200$_H$ | 00'F5FF$_H$ | 1 Kbyte | – |
| ESFR area | 00'F000$_H$ | 00'F1FF$_H$ | 0.5 Kbyte | – |
| XSFR area | 00'E000$_H$ | 00'EFFF$_H$ | 4 Kbytes | – |
| Data SRAM | 00'A000$_H$ | 00'DFFF$_H$ | 16 Kbytes | – |
| Reserved for DSRAM | 00'8000$_H$ | 00'9FFF$_H$ | 8 Kbytes | – |
| External memory area | 00'0000$_H$ | 00'7FFF$_H$ | 32 Kbytes | – |

1) The areas marked with "<" are slightly smaller than indicated. See column "Notes".

2) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000$_H$ to C0'FFFF$_H$).

3) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

## 3.4 Interrupt System

With a minimum interrupt response time of 7/11[1)] CPU clocks (in the case of internal program execution), the XE164 can react quickly to the occurrence of non-deterministic events.

The architecture of the XE164 supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164 has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

Each of the possible interrupt nodes has a separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield. Each node can be programmed by its related register to one of sixteen interrupt priority levels. Once accepted by the CPU, an interrupt service can only be interrupted by a higher-priority service request. For standard interrupt processing, each possible interrupt node has a dedicated vector location.

Fast external interrupt inputs can service external interrupts with high-precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

**Table 6** shows all of the possible XE164 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

*Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes) may be used to generate software-controlled interrupt requests by setting the respective interrupt request bit (xIR).*

1) Depending if the jump cache is used or not.

**Table 6 XE164 Interrupt Nodes**

| Source of Interrupt or PEC Service Request | Control Register | Vector Location[1)] | Trap Number |
|---|---|---|---|
| CAPCOM Register 16, or ERU Request 0 | CC2_CC16IC | xx'0040$_H$ | 10$_H$ / 16$_D$ |
| CAPCOM Register 17, or ERU Request 1 | CC2_CC17IC | xx'0044$_H$ | 11$_H$ / 17$_D$ |
| CAPCOM Register 18, or ERU Request 2 | CC2_CC18IC | xx'0048$_H$ | 12$_H$ / 18$_D$ |
| CAPCOM Register 19, or ERU Request 3 | CC2_CC19IC | xx'004C$_H$ | 13$_H$ / 19$_D$ |
| CAPCOM Register 20, or USIC0 Request 6 | CC2_CC20IC | xx'0050$_H$ | 14$_H$ / 20$_D$ |
| CAPCOM Register 21, or USIC0 Request 7 | CC2_CC21IC | xx'0054$_H$ | 15$_H$ / 21$_D$ |
| CAPCOM Register 22, or USIC1 Request 6 | CC2_CC22IC | xx'0058$_H$ | 16$_H$ / 22$_D$ |
| CAPCOM Register 23, or USIC1 Request 7 | CC2_CC23IC | xx'005C$_H$ | 17$_H$ / 23$_D$ |
| CAPCOM Register 24, or ERU Request 0 | CC2_CC24IC | xx'0060$_H$ | 18$_H$ / 24$_D$ |
| CAPCOM Register 25, or ERU Request 1 | CC2_CC25IC | xx'0064$_H$ | 19$_H$ / 25$_D$ |
| CAPCOM Register 26, or ERU Request 2 | CC2_CC26IC | xx'0068$_H$ | 1A$_H$ / 26$_D$ |
| CAPCOM Register 27, or ERU Request 3 | CC2_CC27IC | xx'006C$_H$ | 1B$_H$ / 27$_D$ |
| CAPCOM Register 28, or USIC2 Request 6 | CC2_CC28IC | xx'0070$_H$ | 1C$_H$ / 28$_D$ |
| CAPCOM Register 29, or USIC2 Request 7 | CC2_CC29IC | xx'0074$_H$ | 1D$_H$ / 29$_D$ |
| CAPCOM Register 30 | CC2_CC30IC | xx'0078$_H$ | 1E$_H$ / 30$_D$ |
| CAPCOM Register 31 | CC2_CC31IC | xx'007C$_H$ | 1F$_H$ / 31$_D$ |
| GPT1 Timer 2 | GPT12E_T2IC | xx'0080$_H$ | 20$_H$ / 32$_D$ |
| GPT1 Timer 3 | GPT12E_T3IC | xx'0084$_H$ | 21$_H$ / 33$_D$ |
| GPT1 Timer 4 | GPT12E_T4IC | xx'0088$_H$ | 22$_H$ / 34$_D$ |

**Table 6 XE164 Interrupt Nodes** (cont'd)

| Source of Interrupt or PEC Service Request | Control Register | Vector Location[1)] | Trap Number |
|---|---|---|---|
| GPT2 Timer 5 | GPT12E_T5IC | xx'008C$_H$ | 23$_H$ / 35$_D$ |
| GPT2 Timer 6 | GPT12E_T6IC | xx'0090$_H$ | 24$_H$ / 36$_D$ |
| GPT2 CAPREL Register | GPT12E_CRIC | xx'0094$_H$ | 25$_H$ / 37$_D$ |
| CAPCOM Timer 7 | CC2_T7IC | xx'0098$_H$ | 26$_H$ / 38$_D$ |
| CAPCOM Timer 8 | CC2_T8IC | xx'009C$_H$ | 27$_H$ / 39$_D$ |
| A/D Converter Request 0 | ADC_0IC | xx'00A0$_H$ | 28$_H$ / 40$_D$ |
| A/D Converter Request 1 | ADC_1IC | xx'00A4$_H$ | 29$_H$ / 41$_D$ |
| A/D Converter Request 2 | ADC_2IC | xx'00A8$_H$ | 2A$_H$ / 42$_D$ |
| A/D Converter Request 3 | ADC_3IC | xx'00AC$_H$ | 2B$_H$ / 43$_D$ |
| A/D Converter Request 4 | ADC_4IC | xx'00B0$_H$ | 2C$_H$ / 44$_D$ |
| A/D Converter Request 5 | ADC_5IC | xx'00B4$_H$ | 2D$_H$ / 45$_D$ |
| A/D Converter Request 6 | ADC_6IC | xx'00B8$_H$ | 2E$_H$ / 46$_D$ |
| A/D Converter Request 7 | ADC_7IC | xx'00BC$_H$ | 2F$_H$ / 47$_D$ |
| CCU60 Request 0 | CCU60_0IC | xx'00C0$_H$ | 30$_H$ / 48$_D$ |
| CCU60 Request 1 | CCU60_1IC | xx'00C4$_H$ | 31$_H$ / 49$_D$ |
| CCU60 Request 2 | CCU60_2IC | xx'00C8$_H$ | 32$_H$ / 50$_D$ |
| CCU60 Request 3 | CCU60_3IC | xx'00CC$_H$ | 33$_H$ / 51$_D$ |
| CCU61 Request 0 | CCU61_0IC | xx'00D0$_H$ | 34$_H$ / 52$_D$ |
| CCU61 Request 1 | CCU61_1IC | xx'00D4$_H$ | 35$_H$ / 53$_D$ |
| CCU61 Request 2 | CCU61_2IC | xx'00D8$_H$ | 36$_H$ / 54$_D$ |
| CCU61 Request 3 | CCU61_3IC | xx'00DC$_H$ | 37$_H$ / 55$_D$ |
| CCU62 Request 0 | CCU62_0IC | xx'00E0$_H$ | 38$_H$ / 56$_D$ |
| CCU62 Request 1 | CCU62_1IC | xx'00E4$_H$ | 39$_H$ / 57$_D$ |
| CCU62 Request 2 | CCU62_2IC | xx'00E8$_H$ | 3A$_H$ / 58$_D$ |
| CCU62 Request 3 | CCU62_3IC | xx'00EC$_H$ | 3B$_H$ / 59$_D$ |
| Unassigned node | – | xx'00F0$_H$ | 3C$_H$ / 60$_D$ |
| Unassigned node | – | xx'00F4$_H$ | 3D$_H$ / 61$_D$ |
| Unassigned node | – | xx'00F8$_H$ | 3E$_H$ / 62$_D$ |
| Unassigned node | – | xx'00FC$_H$ | 3F$_H$ / 63$_D$ |
| CAN Request 0 | CAN_0IC | xx'0100$_H$ | 40$_H$ / 64$_D$ |

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD[1)]). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE164 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

1) Exception: T5EUD is not connected to a pin.

## 3.10 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 11 + 5 multiplexed input channels and a sample and hold circuit have been integrated on-chip. They use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically.

For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XE164 support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features, such as limit checking or result accumulation, reduce the number of required CPU access operations allowing the precise evaluation of analoginputs (high conversion rate) even at a low CPU speed.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately with registers P5_DIDIS and P15_DIDIS (Port x Digital Input Disable).

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

### MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to four independent CAN nodes
- 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

## 3.16 Instruction Set Summary

Table 10 lists the instructions of the XE164.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

**Table 10 Instruction Set Summary**

| Mnemonic | Description | Bytes |
|---|---|---|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16- × 16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| OR(B) | Bitwise OR, (word/byte operands) | 2 / 4 |
| XOR(B) | Bitwise exclusive OR, (word/byte operands) | 2 / 4 |
| BCLR/BSET | Clear/Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND/BOR/BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH/BFLDL | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL/SHR | Shift left/right direct word GPR | 2 |

4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature ($T_J$ = junction temperature [°C]):
$I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = $V_{DDP}$ - $V_{PIN}$ [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

## 4.3 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

**Table 18 A/D Converter Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Analog reference supply | $V_{AREF}$ | SR | $V_{AGND}$ + 1.0 | $V_{DDPA}$ + 0.05 | V | 1) |
| Analog reference ground | $V_{AGND}$ | SR | $V_{SS}$ - 0.05 | $V_{AREF}$ - 1.0 | V | – |
| Analog input voltage range | $V_{AIN}$ | SR | $V_{AGND}$ | $V_{AREF}$ | V | 2) |
| Analog clock frequency | $f_{ADCI}$ | | 0.5 | 20 | MHz | 3) |
| Conversion time for 10-bit result[4)] | $t_{C10}$ | CC | (13 + STC) × $t_{ADCI}$ + 2 × $t_{SYS}$ | | – | – |
| Conversion time for 8-bit result[4)] | $t_{C8}$ | CC | (11 + STC) × $t_{ADCI}$ + 2 × $t_{SYS}$ | | – | – |
| Wakeup time from analog powerdown, fast mode | $t_{WAF}$ | CC | – | 1 | µs | – |
| Wakeup time from analog powerdown, slow mode | $t_{WAS}$ | CC | – | 10 | µs | – |
| Total unadjusted error[5)] | TUE | CC | – | ±2 | LSB | $V_{AREF}$ = 5.0 V[1)] |
| DNL error | $EA_{DNL}$ | CC | – | ±1 | LSB | |
| INL error | $EA_{INL}$ | CC | – | ±1.2 | LSB | |
| Gain error | $EA_{GAIN}$ | CC | – | ±0.8 | LSB | |
| Offset error | $EA_{OFF}$ | CC | – | ±0.8 | LSB | |
| Total capacitance of an analog input | $C_{AINT}$ | CC | – | 10 | pF | 6)7) |
| Switched capacitance of an analog input | $C_{AINS}$ | CC | – | 4 | pF | 6)7) |
| Resistance of the analog input path | $R_{AIN}$ | CC | – | 1.5 | kΩ | 6)7) |
| Total capacitance of the reference input | $C_{AREFT}$ | CC | – | 15 | pF | 6)7) |

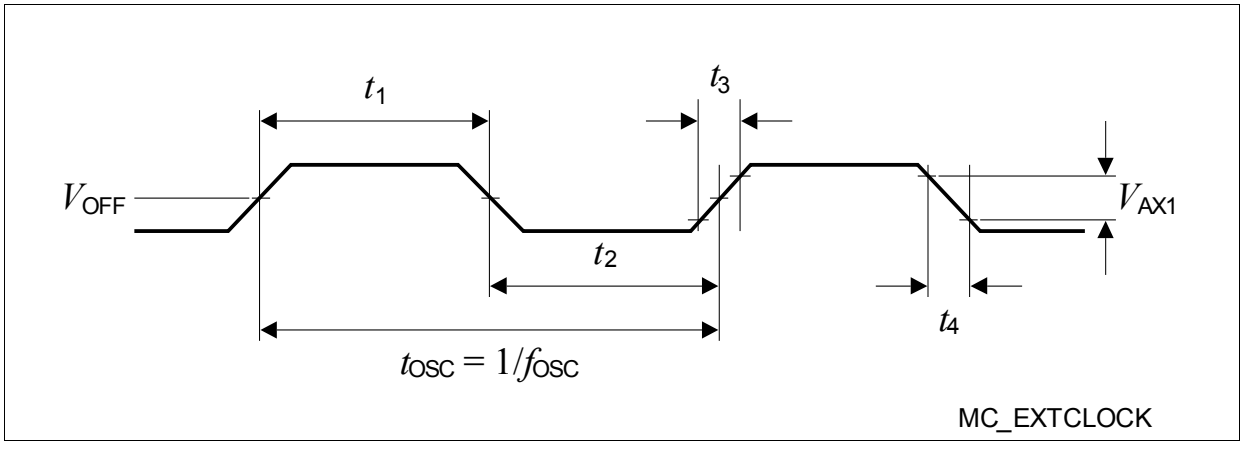


**Figure 20 External Clock Drive XTAL1**

*Note: For crystal/resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.*
*Please refer to the limits specified by the crystal/resonator supplier.*

### 4.6.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 33 JTAG Interface Timing Parameters (Operating Conditions apply)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK clock period | $t_1$ SR | 60 | 50 | – | ns | – |
| TCK high time | $t_2$ SR | 16 | – | – | ns | – |
| TCK low time | $t_3$ SR | 16 | – | – | ns | – |
| TCK clock rise time | $t_4$ SR | – | – | 8 | ns | – |
| TCK clock fall time | $t_5$ SR | – | – | 8 | ns | – |
| TDI/TMS setup to TCK rising edge | $t_6$ SR | 6 | – | – | ns | – |
| TDI/TMS hold after TCK rising edge | $t_7$ SR | 6 | – | – | ns | – |
| TDO valid after TCK falling edge[1] | $t_8$ CC | – | – | 30 | ns | $C_L$ = 50 pF |
| | $t_8$ CC | 10 | – | – | ns | $C_L$ = 20 pF |
| TDO high imped. to valid from TCK falling edge[1)2)] | $t_9$ CC | – | – | 30 | ns | $C_L$ = 50 pF |
| TDO valid to high imped. from TCK falling edge[1)] | $t_{10}$ CC | – | – | 30 | ns | $C_L$ = 50 pF |

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

## Package Outlines

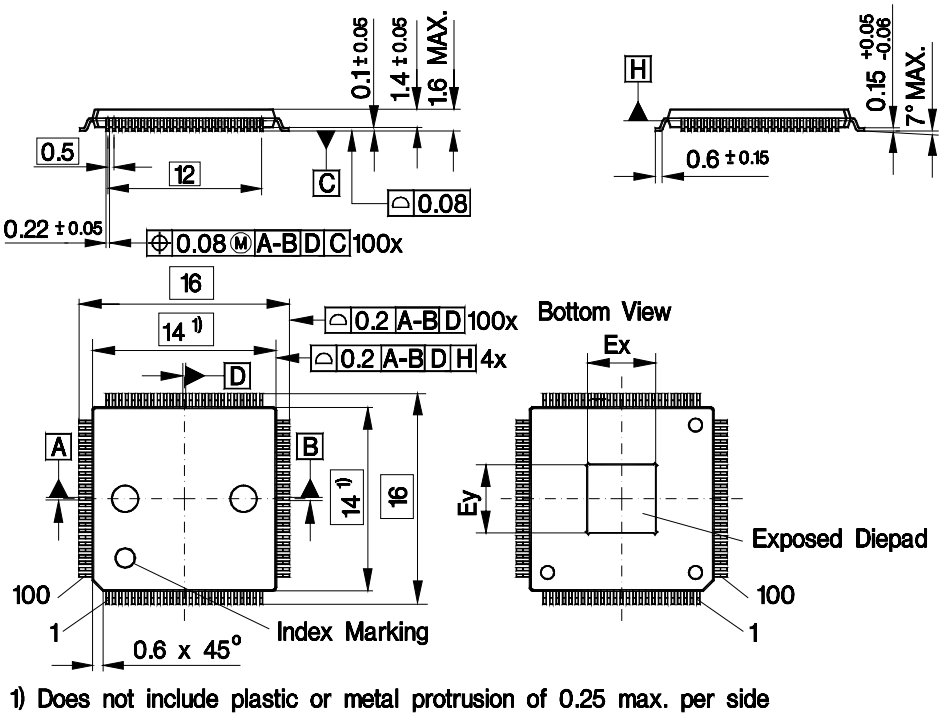


**Figure 28 PG-LQFP-100-3** (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

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