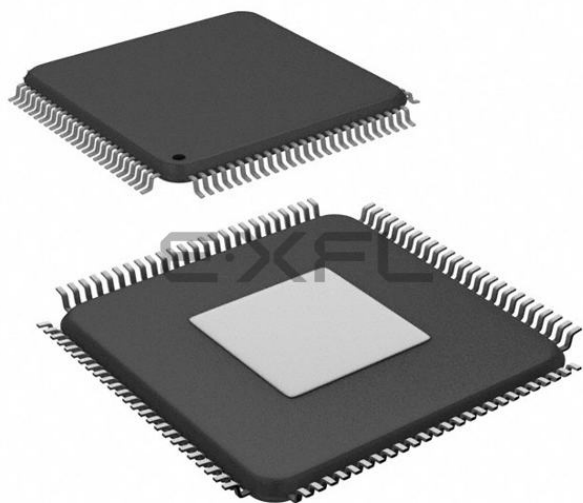




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Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164f96f66lacfxqma1

XE164

Revision History: V2.1, 2008-08

Previous Version(s):

V2.0, 2008-03, Preliminary

V0.1, 2007-09, Preliminary

Page	Subjects (major changes since last revision)
several	Maximum frequency changed to 80 MHz
8	Specification of 6 ADC0 channels corrected
14f	Missing ADC0 channels added
28	Voltage domain for XTAL1/XTAL2 corrected to M
68	Coupling factors corrected
73, 75	Improved leakage parameters
74, 76	Pin leakage formula corrected
81	Improved ADC error values
94f	Improved definition of external clock parameters
107	JTAG clock speed corrected

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Summary of Features

- 2) Specific information about the on-chip Flash memory in [Table 2](#).
- 3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM (12 Kbytes for devices with 192 Kbytes of Flash).
- 4) Specific information about the available channels in [Table 3](#).
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Notes to Pin Definitions

1. **Ctrl.:** The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bitfield PC to 1x00_B, output O1 is selected by 1x01_B, etc.
Output signal OH is controlled by hardware.
2. **Type:** Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	CCU62_ CCPOS0A	I	St/B	CCU62 Position Input 0
	TDI_C	I	St/B	JTAG Test Data Input
5	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE164's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT1 Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT2 Timer T6 Toggle Latch Output
	TDO_A	OH	St/B	JTAG Test Data Output
	ESR2_1	I	St/B	ESR2 Trigger Input 1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
70	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLKOUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COUT62	O2	St/B	CCU60 Channel 2 Output
	AD5	OH / I	St/B	External Bus Interface Address/Data Line 5
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
71	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CCU61_COUT63	O3	St/B	CCU61 Channel 3 Output
	A6	OH	St/B	External Bus Interface Address Line 6
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTRAPA	I	St/B	CCU61 Emergency Trap Input
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input
72	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	U1C0_SELO0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	AD6	OH / I	St/B	External Bus Interface Address/Data Line 6
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTRAPA	I	St/B	CCU60 Emergency Trap Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
82	P10.10	O0 / I	St/B	Bit 10 of Port 10, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	AD10	OH / I	St/B	External Bus Interface Address/Data Line 10
	U0C0_DX2C	I	St/B	USIC0 Channel 0 Shift Control Input
	TDI_B	I	St/B	JTAG Test Data Input
	U0C1_DX1A	I	St/B	USIC0 Channel 1 Shift Clock Input
83	P10.11	O0 / I	St/B	Bit 11 of Port 10, General Purpose Input/Output
	U1C0_SCLKOUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	BRKOUT	O2	St/B	OCDS Break Signal Output
	AD11	OH / I	St/B	External Bus Interface Address/Data Line 11
	U1C0_DX1D	I	St/B	USIC1 Channel 0 Shift Clock Input
	RxDC2B	I	St/B	CAN Node 2 Receive Data Input
	TMS_B	I	St/B	JTAG Test Mode Selection Input
84	P1.2	O0 / I	St/B	Bit 2 of Port 1, General Purpose Input/Output
	CCU62_CC62	O1 / I	St/B	CCU62 Channel 2 Input/Output
	U1C0_SELO6	O2	St/B	USIC1 Channel 0 Select/Control 6 Output
	U2C1_SCLKOUT	O3	St/B	USIC2 Channel 1 Shift Clock Output
	A10	OH	St/B	External Bus Interface Address Line 10
	ESR1_4	I	St/B	ESR1 Trigger Input 4
	CCU61_T12HRB	I	St/B	External Run Control Input for T12 of CCU61
	EX2AINA	I	St/B	External Interrupt Trigger Input
	U2C1_DX0D	I	St/B	USIC2 Channel 1 Shift Data Input
	U2C1_DX1C	I	St/B	USIC2 Channel 1 Shift Clock Input

Functional Description

The XE164 includes an excellent mechanism to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 7 shows all possible exceptions or error conditions that can arise during runtime:

Table 7 Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location ¹⁾	Trap Number	Trap Priority
Reset Functions	–	RESET	xx'0000 _H	00 _H	III
Class A Hardware Traps:					
• System Request 0	SR0	SR0TRAP	xx'0008 _H	02 _H	II
• Stack Overflow	STKOF	STOTRAP	xx'0010 _H	04 _H	II
• Stack Underflow	STKUF	STUTRAP	xx'0018 _H	06 _H	II
• Software Break	SOFTBRK	SBRKTRAP	xx'0020 _H	08 _H	II
Class B Hardware Traps:					
• System Request 1	SR1	BTRAP	xx'0028 _H	0A _H	I
• Undefined Opcode	UNDOPC	BTRAP	xx'0028 _H	0A _H	I
• Memory Access Error	ACER	BTRAP	xx'0028 _H	0A _H	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx'0028 _H	0A _H	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx'0028 _H	0A _H	I
Reserved	–	–	[2C _H - 3C _H]	[0B _H - 0F _H]	–
Software Traps:	–	–	Any	Any	Current
• TRAP Instruction			[xx'0000 _H - xx'01FC _H] in steps of 4 _H	[00 _H - 7F _H]	CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

3.6 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to a number of prescaled values of the internal system clock. It may also be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range for the timer period and resolution while allowing precise adjustments for application-specific requirements. An external count input for CAPCOM2 timer T7 allows event scheduling for the capture/compare registers with respect to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers. Each may be individually allocated to either CAPCOM2 timer T7 or T8 and programmed for a capture or compare function.

12 registers of the CAPCOM2 module have one port pin associated with it. This serves as an input pin to trigger the capture function or as an output pin to indicate the occurrence of a compare event.

Table 8 Compare Modes (CAPCOM2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

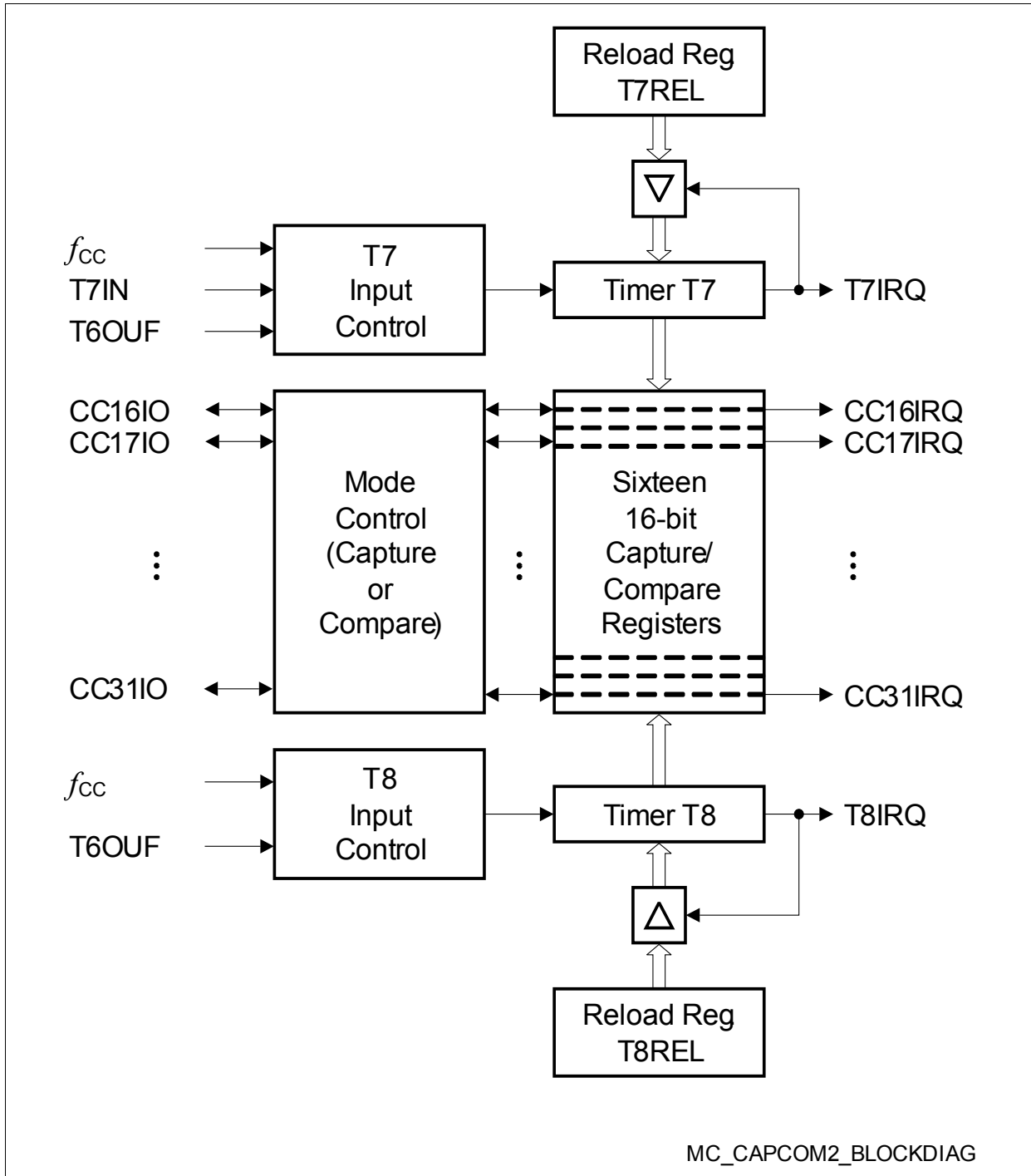


Figure 5 CAPCOM2 Unit Block Diagram

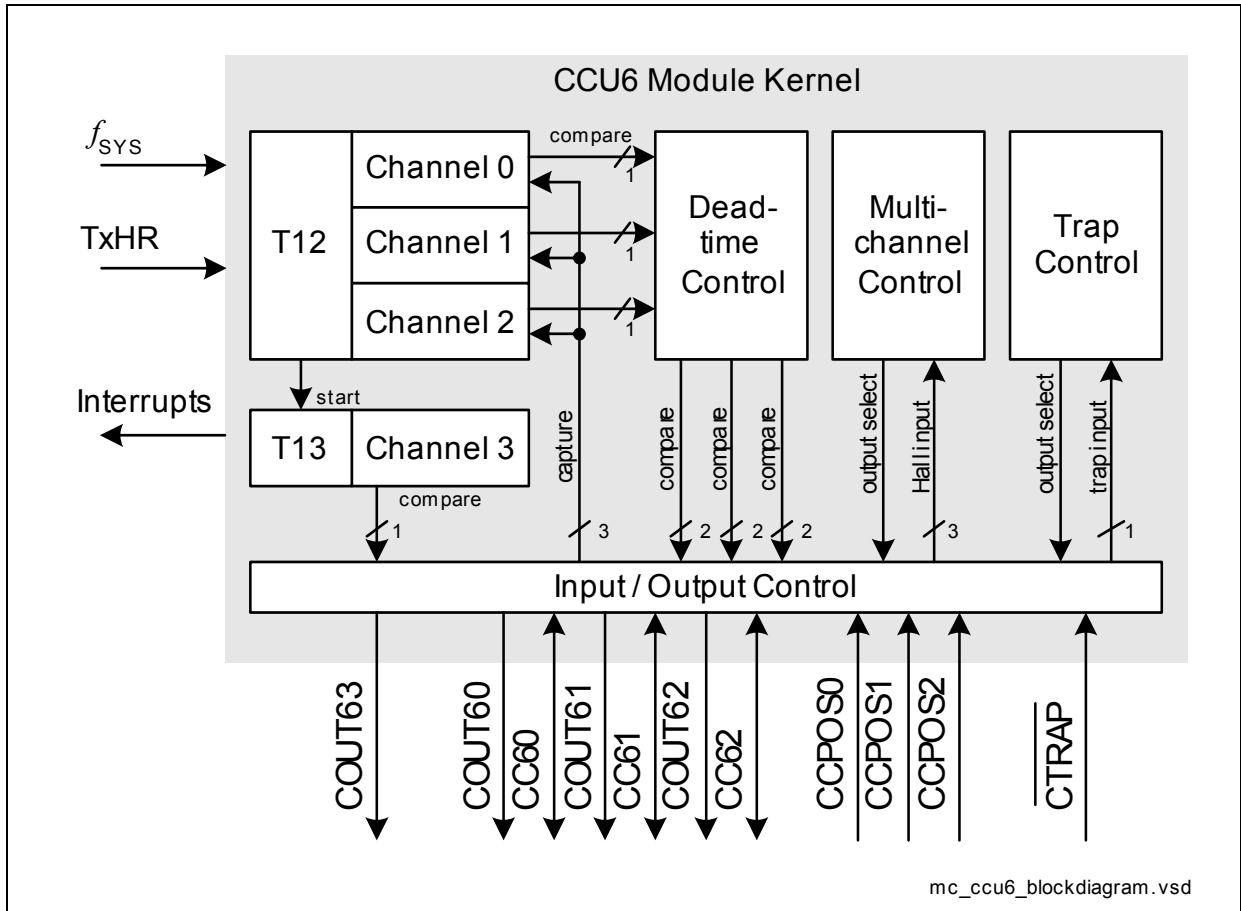


Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

Functional Description

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
 - maximum baud rate: $f_{\text{SYS}} / 4$
 - data frame length programmable from 1 to 63 bits
 - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
 - maximum baud rate: $f_{\text{SYS}} / 16$
 - checksum generation under software control
 - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
 - maximum baud rate in slave mode: f_{SYS}
 - maximum baud rate in master mode: $f_{\text{SYS}} / 2$, limited by loop delay
 - number of data bits programmable from 1 to 63, more with explicit stop condition
 - MSB or LSB first
 - optional control of slave select signals
- **IIC** (Inter-IC Bus)
 - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
 - maximum baud rate: $f_{\text{SYS}} / 2$ for transmitter, f_{SYS} for receiver

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 12 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital core supply voltage	V_{DDI}	1.4	–	1.6	V	
Core Supply Voltage Difference	ΔV_{DDI}	-10	–	+10	mV	$V_{DDIM} - V_{DDI1}$ 1)
Digital supply voltage for IO pads and voltage regulators, upper voltage range	V_{DDPA}, V_{DDPB}	4.5	–	5.5	V	2)
Digital supply voltage for IO pads and voltage regulators, lower voltage range	V_{DDPA}, V_{DDPB}	3.0	–	4.5	V	2)
Digital ground voltage	V_{SS}	0	–	0	V	Reference voltage
Overload current	I_{OV}	-5	–	5	mA	Per IO pin ³⁾⁴⁾
		-2	–	5	mA	Per analog input pin ³⁾⁴⁾
Overload positive current coupling factor for analog inputs ⁵⁾	K_{OVA}	–	1.0×10^{-6}	1.0×10^{-4}	–	$I_{OV} > 0$
Overload negative current coupling factor for analog inputs ⁵⁾	K_{OVA}	–	2.5×10^{-4}	1.5×10^{-3}	–	$I_{OV} < 0$
Overload positive current coupling factor for digital I/O pins ⁵⁾	K_{OVD}	–	1.0×10^{-4}	5.0×10^{-3}	–	$I_{OV} > 0$
Overload negative current coupling factor for digital I/O pins ⁵⁾	K_{OVD}	–	1.0×10^{-2}	3.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma IOV $	–	–	50	mA	4)

Parameter Interpretation

The parameters listed in the following include both the characteristics of the XE164 and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column "Symbol":

CC (Controller Characteristics):

The logic of the XE164 provides signals with the specified characteristics.

SR (System Requirement):

The external system must provide signals with the specified characteristics to the XE164.

Table 16 Switching Power Consumption XE164
(Operating Conditions apply)

Parameter	Sym- bol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT}	–	10 + $0.6 \times f_{\text{SYS}}$	10 + $1.0 \times f_{\text{SYS}}$	mA	Active mode ¹⁾²⁾ f_{SYS} in [MHz]
Power supply current in stopover mode, EVVRs on	I_{SSO}	–	1.0	2.0	mA	Stopover Mode ²⁾

1) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers' input stages are switched.

2) The pad supply voltage has only a minor influence on this parameter.

Table 18 A/D Converter Characteristics (cont'd)
(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Switched capacitance of the reference input	C_{AREFS}	CC	–	7	pF	6)7)
Resistance of the reference input path	R_{AREF}	CC	–	2	kΩ	6)7)

- 1) TUE is tested at $V_{AREFX} = V_{DDPA}$, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.
- 2) V_{AIN} may exceed V_{AGND} or V_{AREFX} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.
- 3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
- 4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{ADCI} depend on programming and are found in [Table 19](#).
- 5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.
- 6) Not subject to production test - verified by design/characterization.
- 7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
 $C_{AINTtyp} = 12$ pF, $C_{AINStyp} = 5$ pF, $R_{AINTtyp} = 1.0$ kΩ, $C_{AREFTtyp} = 15$ pF, $C_{AREFStyp} = 10$ pF, $R_{AREFTyp} = 1.0$ kΩ.

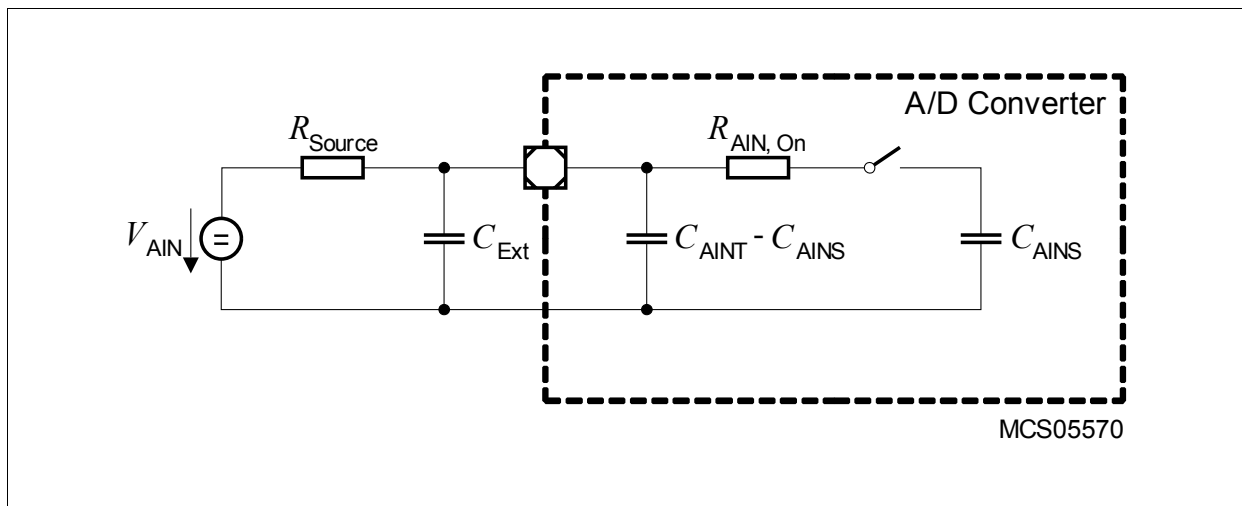


Figure 15 Equivalent Circuitry for Analog Inputs

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH} . In connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters ($t_1 \dots t_4$) are only valid for an external clock input signal.

Table 26 External Clock Input Characteristics
(Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range limits for signal on XTAL1	V_{IX1} SR	$-1.7 + V_{DDI}$	–	1.7	V	1)
Input voltage (amplitude) on XTAL1	V_{AX1} SR	$0.3 \times V_{DDI}$	–	–	V	Peak-to-peak voltage ²⁾
XTAL1 input current	I_{IL} CC	–	–	± 20	μA	$0 V < V_{IN} < V_{DDI}$
Oscillator frequency	f_{OSC} CC	4	–	40	MHz	Clock signal
		4	–	16	MHz	Crystal or Resonator
High time	t_1 SR	6	–	–	ns	
Low time	t_2 SR	6	–	–	ns	
Rise time	t_3 SR	–	8	8	ns	
Fall time	t_4 SR	–	8	8	ns	

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .

Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

Table 32 SSC Master/Slave Mode Timing for Lower Voltage Range
(Operating Conditions apply), $C_L = 50 \text{ pF}$

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	—	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$0.5 \times t_{\text{BIT}}$	—	3)	ns	2)
Transmit data output valid time	t_3 CC	-13	—	16	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	48	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-11	—	—	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	12	—	—	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	8	—	—	ns	4)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	12	—	—	ns	4)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	8	—	—	ns	4)
Data output DOUT valid time	t_{14} CC	11	—	44	ns	4)

- 1) The maximum value further depends on the settings for the slave select output leading delay.
- 2) $t_{\text{SYS}} = 1/f_{\text{SYS}} (= 12.5 \text{ ns @ } 80 \text{ MHz})$
- 3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.
- 4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Package Outlines

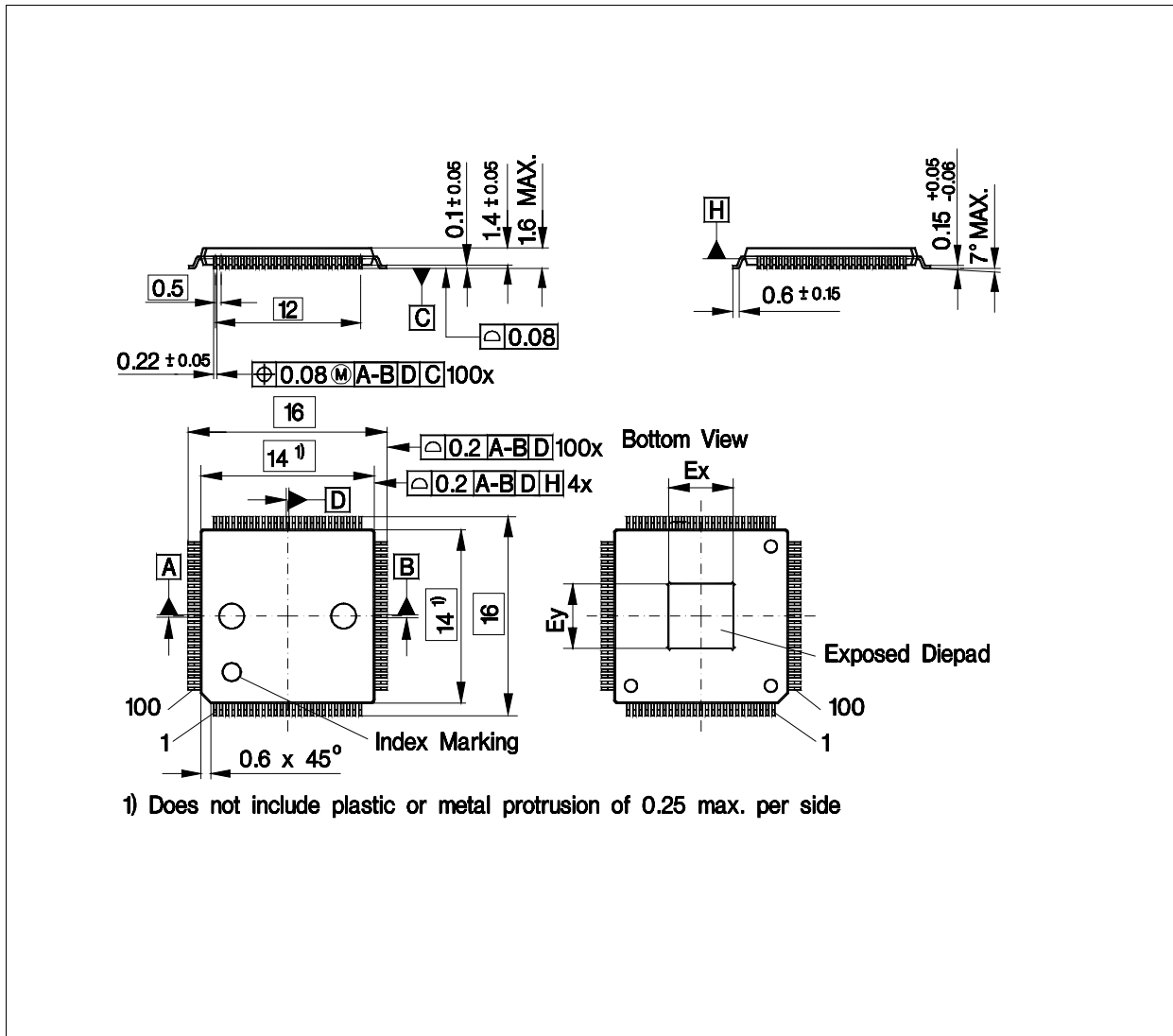


Figure 28 PG-LQFP-100-3 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": <http://www.infineon.com/packages>