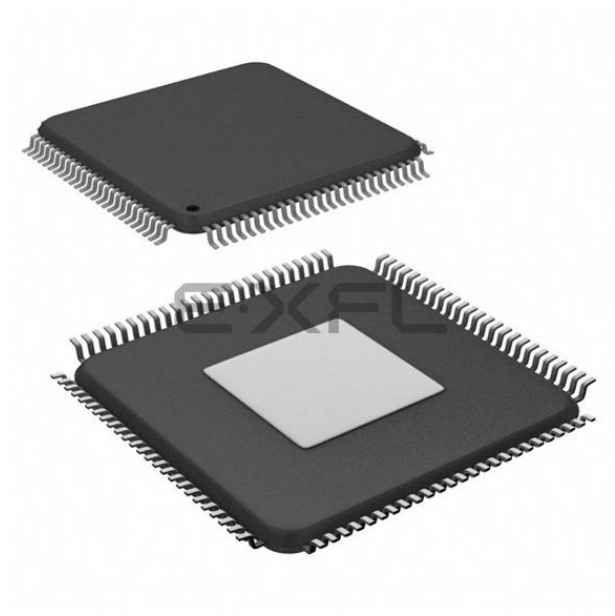
Infineon Technologies - XE164F96F66LACFXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164f96f66lacfxuma1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_ CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	I	St/B	**JTAG Test Mode Selection Input**
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
8	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	CCU62_ CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**
9	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_ SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU62_ CCPOS2A	I	St/B	**CCU62 Position Input 2**
	TCK_C	I	St/B	**JTAG Clock Input**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**
11	P6.0	O0 / I	St/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	St/A	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	St/A	**OCDS Break Signal Output**
	ADCx_ REQGTyC	I	St/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	St/A	**USIC1 Channel 1 Shift Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
70	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_ SCLKOUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_ COUT62	O2	St/B	**CCU60 Channel 2 Output**
	AD5	OH / I	St/B	**External Bus Interface Address/Data Line 5**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
71	P0.6	O0 / I	St/B	**Bit 6 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CCU61_ COUT63	O3	St/B	**CCU61 Channel 3 Output**
	A6	OH	St/B	**External Bus Interface Address Line 6**
	U1C1_DX0A	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_ CTRAPA	I	St/B	**CCU61 Emergency Trap Input**
	U1C1_DX1B	I	St/B	**USIC1 Channel 1 Shift Clock Input**
72	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U1C0_ SELO0	O3	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	AD6	OH / I	St/B	**External Bus Interface Address/Data Line 6**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX2D	I	St/B	**USIC1 Channel 0 Shift Control Input**
	CCU60_ CTRAPA	I	St/B	**CCU60 Emergency Trap Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
98	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
	EX0AINB	I	St/B	**External Interrupt Trigger Input**
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** *Note: After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.*
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see **Table 12** for details.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see **Table 12** for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6, and P15 are fed from supply voltage V_{DDPA}.*

3.4 Interrupt System

With a minimum interrupt response time of 7/11[1)] CPU clocks (in the case of internal program execution), the XE164 can react quickly to the occurrence of non-deterministic events.

The architecture of the XE164 supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164 has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

Each of the possible interrupt nodes has a separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield. Each node can be programmed by its related register to one of sixteen interrupt priority levels. Once accepted by the CPU, an interrupt service can only be interrupted by a higher-priority service request. For standard interrupt processing, each possible interrupt node has a dedicated vector location.

Fast external interrupt inputs can service external interrupts with high-precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 6 shows all of the possible XE164 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes) may be used to generate software-controlled interrupt requests by setting the respective interrupt request bit (xIR).

1) Depending if the jump cache is used or not.

Table 6 XE164 Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 16, or ERU Request 0	CC2_CC16IC	xx'0040$_H$	10$_H$ / 16$_D$
CAPCOM Register 17, or ERU Request 1	CC2_CC17IC	xx'0044$_H$	11$_H$ / 17$_D$
CAPCOM Register 18, or ERU Request 2	CC2_CC18IC	xx'0048$_H$	12$_H$ / 18$_D$
CAPCOM Register 19, or ERU Request 3	CC2_CC19IC	xx'004C$_H$	13$_H$ / 19$_D$
CAPCOM Register 20, or USIC0 Request 6	CC2_CC20IC	xx'0050$_H$	14$_H$ / 20$_D$
CAPCOM Register 21, or USIC0 Request 7	CC2_CC21IC	xx'0054$_H$	15$_H$ / 21$_D$
CAPCOM Register 22, or USIC1 Request 6	CC2_CC22IC	xx'0058$_H$	16$_H$ / 22$_D$
CAPCOM Register 23, or USIC1 Request 7	CC2_CC23IC	xx'005C$_H$	17$_H$ / 23$_D$
CAPCOM Register 24, or ERU Request 0	CC2_CC24IC	xx'0060$_H$	18$_H$ / 24$_D$
CAPCOM Register 25, or ERU Request 1	CC2_CC25IC	xx'0064$_H$	19$_H$ / 25$_D$
CAPCOM Register 26, or ERU Request 2	CC2_CC26IC	xx'0068$_H$	1A$_H$ / 26$_D$
CAPCOM Register 27, or ERU Request 3	CC2_CC27IC	xx'006C$_H$	1B$_H$ / 27$_D$
CAPCOM Register 28, or USIC2 Request 6	CC2_CC28IC	xx'0070$_H$	1C$_H$ / 28$_D$
CAPCOM Register 29, or USIC2 Request 7	CC2_CC29IC	xx'0074$_H$	1D$_H$ / 29$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0078$_H$	1E$_H$ / 30$_D$
CAPCOM Register 31	CC2_CC31IC	xx'007C$_H$	1F$_H$ / 31$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0080$_H$	20$_H$ / 32$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'0084$_H$	21$_H$ / 33$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0088$_H$	22$_H$ / 34$_D$

Table 6 XE164 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
GPT2 Timer 5	GPT12E_T5IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'0094$_H$	25$_H$ / 37$_D$
CAPCOM Timer 7	CC2_T7IC	xx'0098$_H$	26$_H$ / 38$_D$
CAPCOM Timer 8	CC2_T8IC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Converter Request 0	ADC_0IC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Converter Request 1	ADC_1IC	xx'00A4$_H$	29$_H$ / 41$_D$
A/D Converter Request 2	ADC_2IC	xx'00A8$_H$	2A$_H$ / 42$_D$
A/D Converter Request 3	ADC_3IC	xx'00AC$_H$	2B$_H$ / 43$_D$
A/D Converter Request 4	ADC_4IC	xx'00B0$_H$	2C$_H$ / 44$_D$
A/D Converter Request 5	ADC_5IC	xx'00B4$_H$	2D$_H$ / 45$_D$
A/D Converter Request 6	ADC_6IC	xx'00B8$_H$	2E$_H$ / 46$_D$
A/D Converter Request 7	ADC_7IC	xx'00BC$_H$	2F$_H$ / 47$_D$
CCU60 Request 0	CCU60_0IC	xx'00C0$_H$	30$_H$ / 48$_D$
CCU60 Request 1	CCU60_1IC	xx'00C4$_H$	31$_H$ / 49$_D$
CCU60 Request 2	CCU60_2IC	xx'00C8$_H$	32$_H$ / 50$_D$
CCU60 Request 3	CCU60_3IC	xx'00CC$_H$	33$_H$ / 51$_D$
CCU61 Request 0	CCU61_0IC	xx'00D0$_H$	34$_H$ / 52$_D$
CCU61 Request 1	CCU61_1IC	xx'00D4$_H$	35$_H$ / 53$_D$
CCU61 Request 2	CCU61_2IC	xx'00D8$_H$	36$_H$ / 54$_D$
CCU61 Request 3	CCU61_3IC	xx'00DC$_H$	37$_H$ / 55$_D$
CCU62 Request 0	CCU62_0IC	xx'00E0$_H$	38$_H$ / 56$_D$
CCU62 Request 1	CCU62_1IC	xx'00E4$_H$	39$_H$ / 57$_D$
CCU62 Request 2	CCU62_2IC	xx'00E8$_H$	3A$_H$ / 58$_D$
CCU62 Request 3	CCU62_3IC	xx'00EC$_H$	3B$_H$ / 59$_D$
Unassigned node	–	xx'00F0$_H$	3C$_H$ / 60$_D$
Unassigned node	–	xx'00F4$_H$	3D$_H$ / 61$_D$
Unassigned node	–	xx'00F8$_H$	3E$_H$ / 62$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
CAN Request 0	CAN_0IC	xx'0100$_H$	40$_H$ / 64$_D$

Table 6 XE164 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAN Request 1	CAN_1IC	xx'0104$_H$	41$_H$ / 65$_D$
CAN Request 2	CAN_2IC	xx'0108$_H$	42$_H$ / 66$_D$
CAN Request 3	CAN_3IC	xx'010C$_H$	43$_H$ / 67$_D$
CAN Request 4	CAN_4IC	xx'0110$_H$	44$_H$ / 68$_D$
CAN Request 5	CAN_5IC	xx'0114$_H$	45$_H$ / 69$_D$
CAN Request 6	CAN_6IC	xx'0118$_H$	46$_H$ / 70$_D$
CAN Request 7	CAN_7IC	xx'011C$_H$	47$_H$ / 71$_D$
CAN Request 8	CAN_8IC	xx'0120$_H$	48$_H$ / 72$_D$
CAN Request 9	CAN_9IC	xx'0124$_H$	49$_H$ / 73$_D$
CAN Request 10	CAN_10IC	xx'0128$_H$	4A$_H$ / 74$_D$
CAN Request 11	CAN_11IC	xx'012C$_H$	4B$_H$ / 75$_D$
CAN Request 12	CAN_12IC	xx'0130$_H$	4C$_H$ / 76$_D$
CAN Request 13	CAN_13IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAN Request 14	CAN_14IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAN Request 15	CAN_15IC	xx'013C$_H$	4F$_H$ / 79$_D$
USIC0 Cannel 0, Request 0	U0C0_0IC	xx'0140$_H$	50$_H$ / 80$_D$
USIC0 Cannel 0, Request 1	U0C0_1IC	xx'0144$_H$	51$_H$ / 81$_D$
USIC0 Cannel 0, Request 2	U0C0_2IC	xx'0148$_H$	52$_H$ / 82$_D$
USIC0 Cannel 1, Request 0	U0C1_0IC	xx'014C$_H$	53$_H$ / 83$_D$
USIC0 Cannel 1, Request 1	U0C1_1IC	xx'0150$_H$	54$_H$ / 84$_D$
USIC0 Cannel 1, Request 2	U0C1_2IC	xx'0154$_H$	55$_H$ / 85$_D$
USIC1 Cannel 0, Request 0	U1C0_0IC	xx'0158$_H$	56$_H$ / 86$_D$
USIC1 Cannel 0, Request 1	U1C0_1IC	xx'015C$_H$	57$_H$ / 87$_D$
USIC1 Cannel 0, Request 2	U1C0_2IC	xx'0160$_H$	58$_H$ / 88$_D$
USIC1 Cannel 1, Request 0	U1C1_0IC	xx'0164$_H$	59$_H$ / 89$_D$
USIC1 Cannel 1, Request 1	U1C1_1IC	xx'0168$_H$	5A$_H$ / 90$_D$
USIC1 Cannel 1, Request 2	U1C1_2IC	xx'016C$_H$	5B$_H$ / 91$_D$
USIC2 Cannel 0, Request 0	U2C0_0IC	xx'0170$_H$	5C$_H$ / 92$_D$
USIC2 Cannel 0, Request 1	U2C0_1IC	xx'0174$_H$	5D$_H$ / 93$_D$
USIC2 Cannel 0, Request 2	U2C0_2IC	xx'0178$_H$	5E$_H$ / 94$_D$

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

3.12 MultiCAN Module

The MultiCAN module contains up to four independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of 128 message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

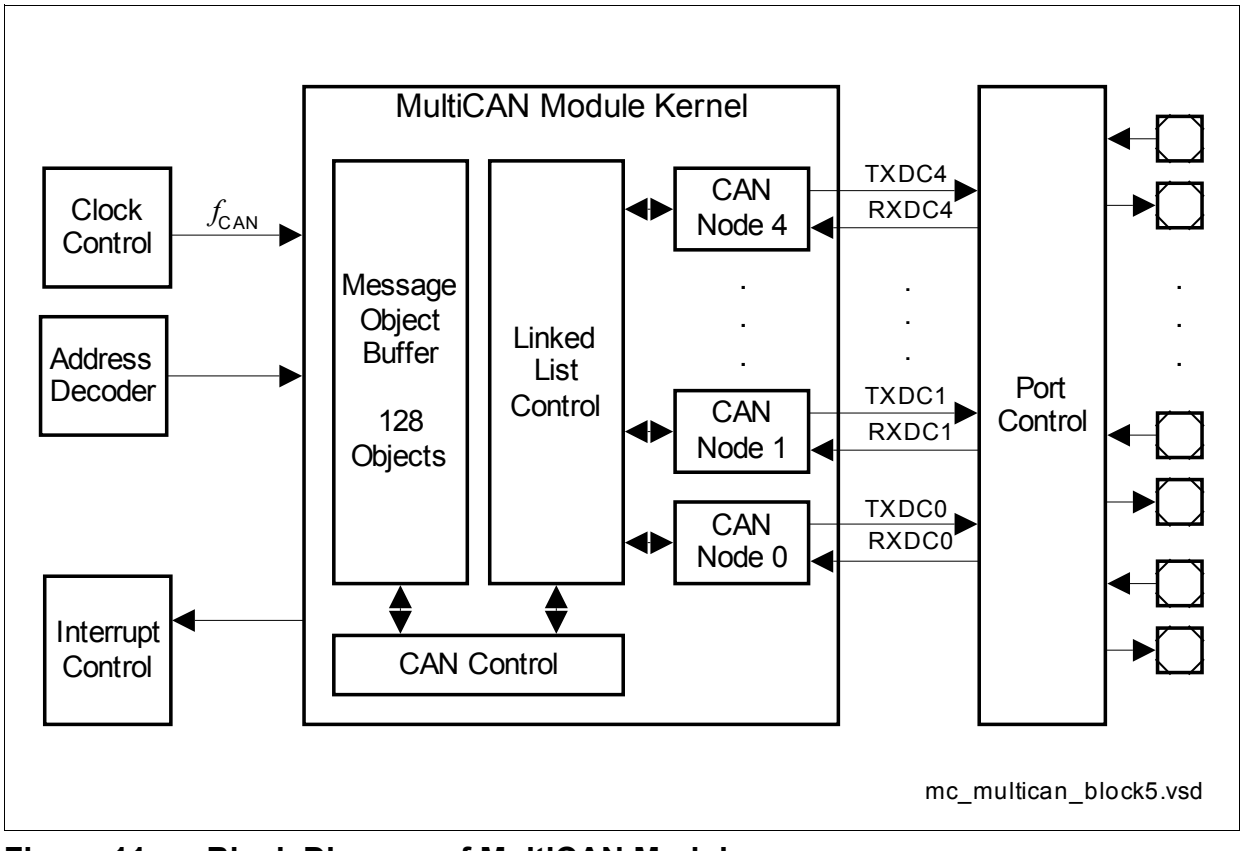

Figure 11 Block Diagram of MultiCAN Module

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE164, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

4 Electrical Parameters

The operating range for the XE164 is defined by its electrical parameters. For proper operation the specified limits must be respected during system design.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature	T_{ST}	-65	–	150	°C	–
Junction temperature	T_J	-40	–	125	°C	under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDIM}, V_{DDI1}	-0.5	–	1.65	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDPA}, V_{DDPB}	-0.5	–	6.0	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} < V_{DDPmax}$
Input current on any pin during overload condition	–	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	–	–	–	|100|	mA	–
Output current on any pin	I_{OH}, I_{OL}	–	–	|30|	mA	–

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 12 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital core supply voltage	V_{DDI}	1.4	–	1.6	V	
Core Supply Voltage Difference	ΔVDDI	-10	–	+10	mV	V_{DDIM} - V_{DDI1} 1)
Digital supply voltage for IO pads and voltage regulators, upper voltage range	V_{DDPA}, V_{DDPB}	4.5	–	5.5	V	2)
Digital supply voltage for IO pads and voltage regulators, lower voltage range	V_{DDPA}, V_{DDPB}	3.0	–	4.5	V	2)
Digital ground voltage	V_{SS}	0	–	0	V	Reference voltage
Overload current	I_{OV}	-5	–	5	mA	Per IO pin 3)4)
		-2	–	5	mA	Per analog input pin 3)4)
Overload positive current coupling factor for analog inputs 5)	K_{OVA}	–	1.0×10^{-6}	1.0×10^{-4}	–	$I_{OV} > 0$
Overload negative current coupling factor for analog inputs 5)	K_{OVA}	–	2.5×10^{-4}	1.5×10^{-3}	–	$I_{OV} < 0$
Overload positive current coupling factor for digital I/O pins 5)	K_{OVD}	–	1.0×10^{-4}	5.0×10^{-3}	–	$I_{OV} > 0$
Overload negative current coupling factor for digital I/O pins 5)	K_{OVD}	–	1.0×10^{-2}	3.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	Σ|IOV|	–	–	50	mA	4)

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE164 can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE164 are designed to operate in various driver modes. The DC parameter specifications refer to the current limits in **Table 13**.

Table 13 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]		Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)	
	$V_{DDP} \geq$ 4.5 V	$V_{DDP} <$ 4.5 V	$V_{DDP} \geq$ 4.5 V	$V_{DDP} <$ 4.5 V
Strong driver	10 mA	10 mA	2.5 mA	2.5 mA
Medium driver	4.0 mA	2.5 mA	1.0 mA	1.0 mA
Weak driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

4.2.2 DC Parameters for Lower Voltage Area

These parameters apply to the lower IO voltage range, 3.0 V ≤ V_{DDP} ≤ 4.5 V.

Table 15 DC Characteristics for Lower Voltage Range (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input Hysteresis[2)]	HYS CC	0.07 × V_{DDP}	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \ge I_{OHmax}$[3)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5, Port 15)[6)]	I_{OZ1} CC	–	±10	±200	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±2.5	µA	$T_J \le$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Pull level keep current	I_{PLK}	–	–	±10	µA	$V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn)
Pull level force current	I_{PLF}	±150	–	–	µA	$V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn)
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

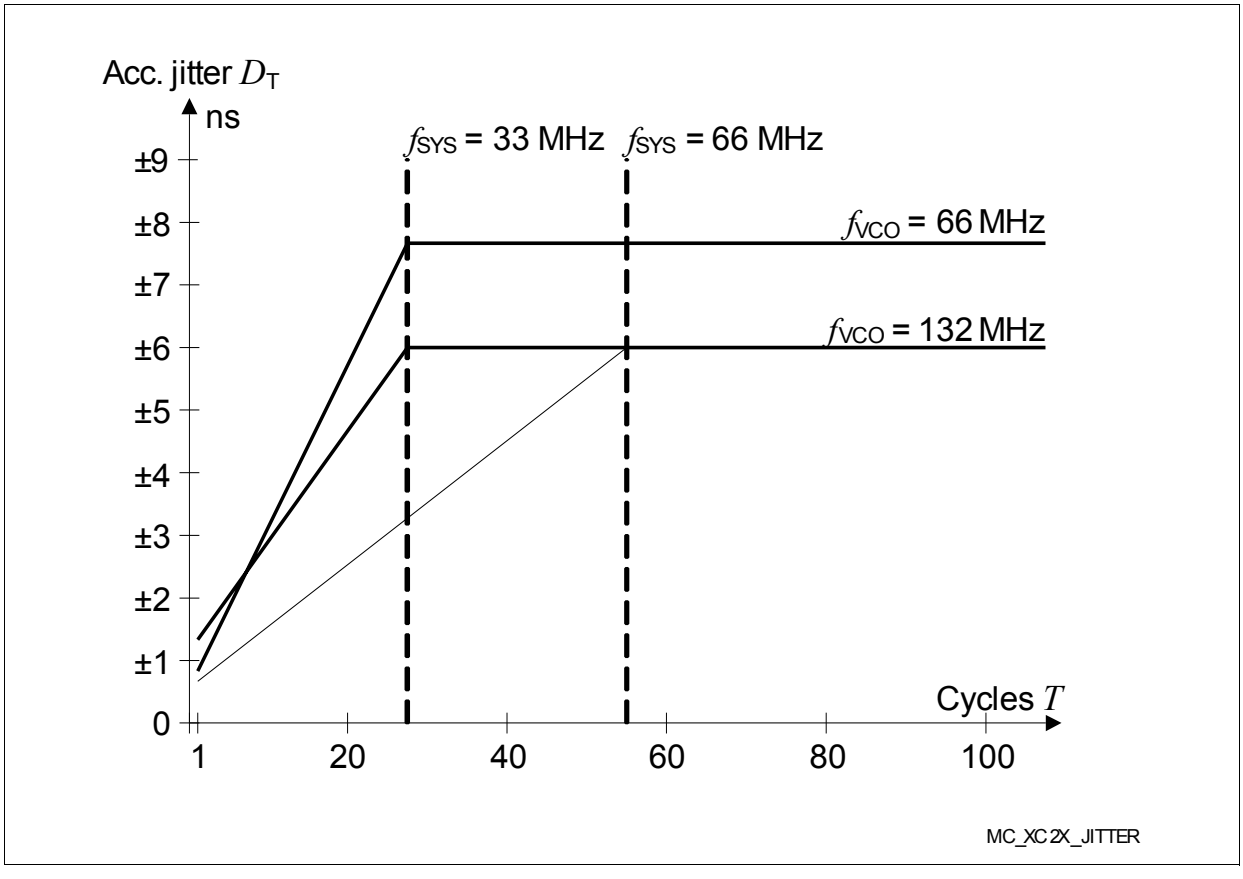

Figure 19 Approximated Accumulated PLL Jitter

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF (see **Table 12**).*
The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100/144 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 25 VCO Bands for PLL Operation[1)]

PLLCON0.VCOSEL	VCO Frequency Range	Base Frequency Range
00	50 … 110 MHz	10 … 40 MHz
01	100 … 160 MHz	20 … 80 MHz
1X	Reserved	

1) Not subject to production test - verified by design/characterization.

Table 29 External Bus Cycle Timing for Upper Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: RD, WR(L/H)	t_{10} CC	–		13	ns	
Output valid delay for: BHE, ALE	t_{11} CC	–		13	ns	
Output valid delay for: A23 … A16, A15 … A0 (on P0/P1)	t_{12} CC	–		14	ns	
Output valid delay for: A15 … A0 (on P2/P10)	t_{13} CC	–		14	ns	
Output valid delay for: CS	t_{14} CC	–		13	ns	
Output valid delay for: D15 … D0 (write data, MUX-mode)	t_{15} CC	–		14	ns	
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	t_{16} CC	–		14	ns	
Output hold time for: RD, WR(L/H)	t_{20} CC	0		8	ns	
Output hold time for: BHE, ALE	t_{21} CC	0		8	ns	
Output hold time for: A23 … A16, A15 … A0 (on P2/P10)	t_{23} CC	0		8	ns	
Output hold time for: CS	t_{24} CC	0		8	ns	
Output hold time for: D15 … D0 (write data)	t_{25} CC	0		8	ns	
Input setup time for: READY, D15 … D0 (read data)	t_{30} SR	18		–	ns	
Input hold time for: READY, D15 … D0 (read data)[1)]	t_{31} SR	-4		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

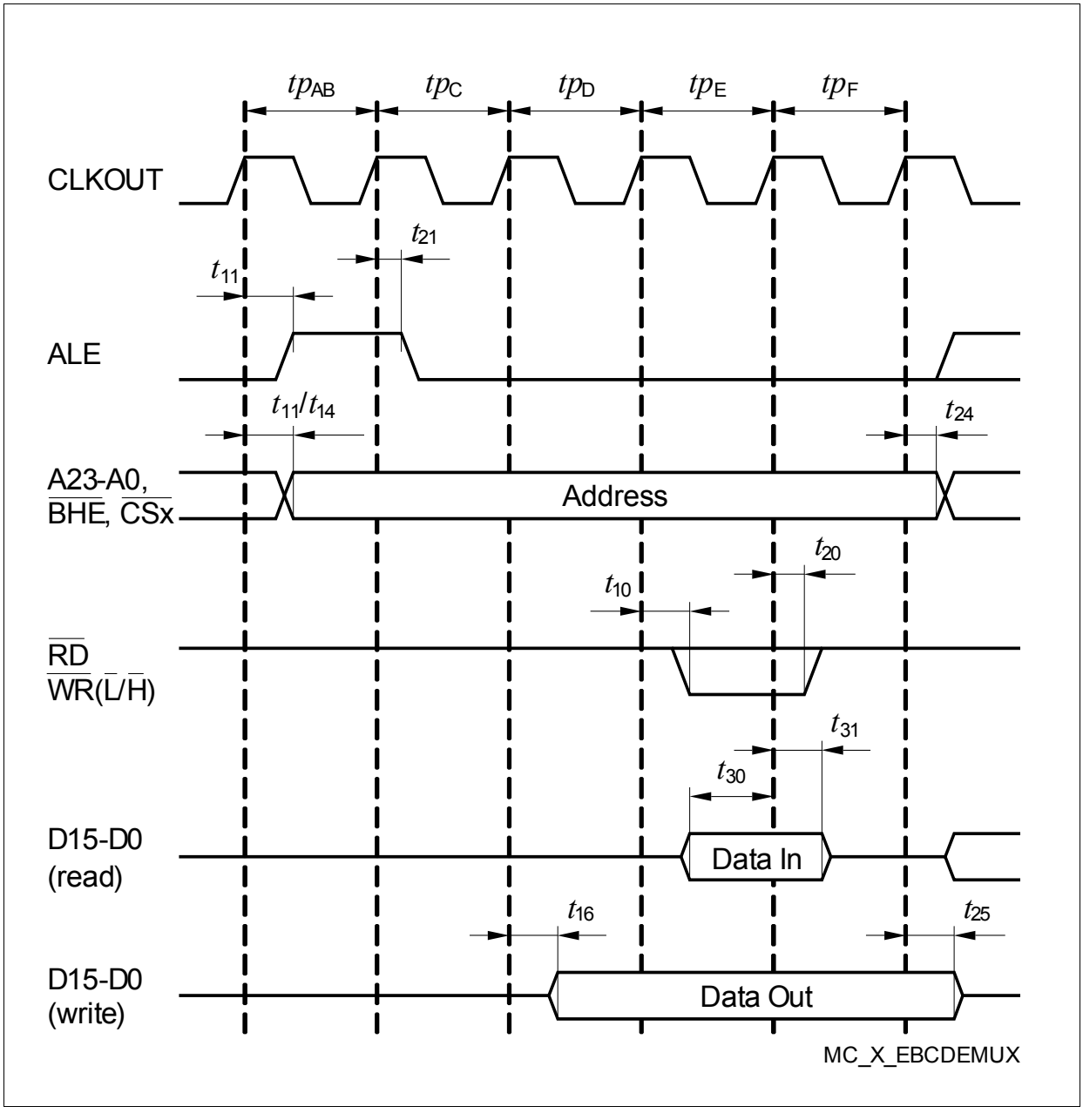

Figure 23 Demultiplexed Bus Cycle

Package Outlines

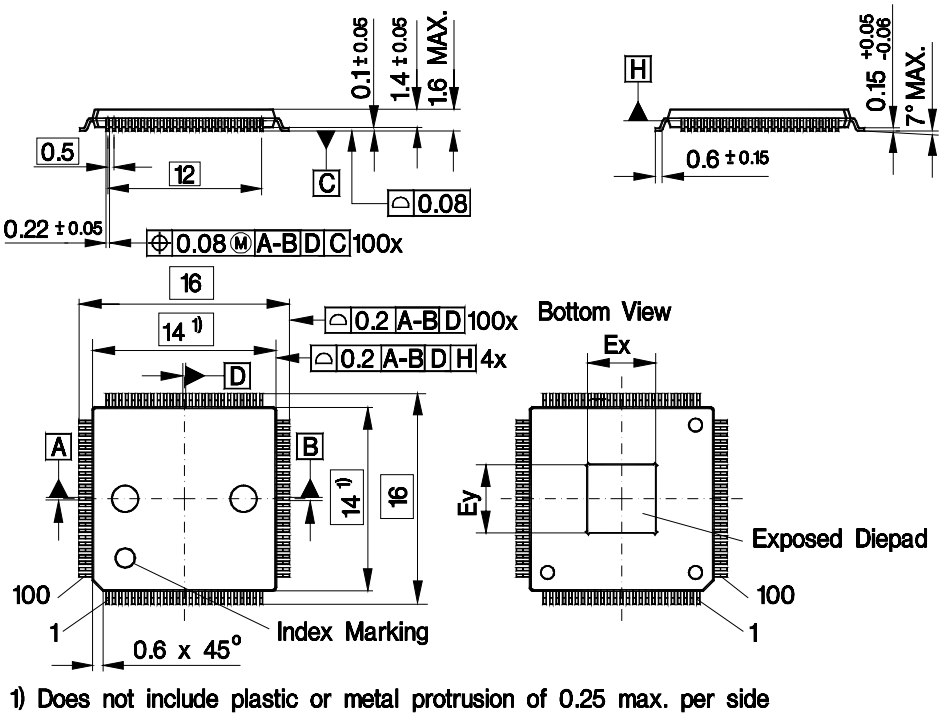

Figure 28 PG-LQFP-100-3 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

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