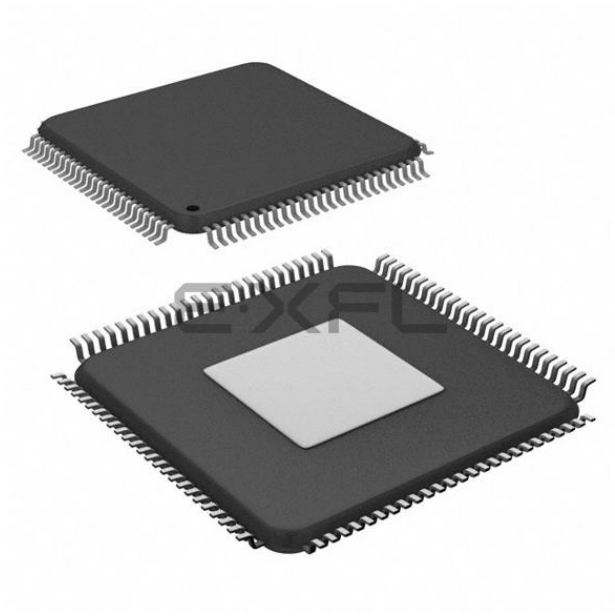
# Infineon Technologies - XE164F96F80LACFXQMA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 75 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 82K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-100-3 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xe164f96f80lacfxqma1 |

# XE164

## 16-Bit Single-Chip Real Time Signal Controller

Microcontrollers

Never stop thinking

2) Specific inormation about the on-chip Flash memory in **Table 2**.
3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM (12 Kbytes for devices with 192 Kbytes of Flash).
4) Specific information about the available channels in **Table 3**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

The XE164 types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

**Table 2 Flash Memory Allocation**

| Total Flash Size | Flash Area A[1)] | Flash Area B | Flash Area C |
|---|---|---|---|
| 768 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $CB'FFFF_H$ | n.a. |
| 576 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $C8'FFFF_H$ | n.a. |
| 384 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $C5'FFFF_H$ | n.a. |
| 192 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $C1'FFFF_H$ | $C4'0000_H$ … $C4'FFFF_H$ |

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE164 types are offered with different interface options. **Table 3** lists the available channels for each option.

**Table 3 Interface Channel Association**

| Total Number | Available Channels |
|---|---|
| 11 ADC0 channels | CH0, CH2 … CH5, CH8 … CH11, CH13, CH15 |
| 6 ADC0 channels | CH0, CH2, CH3, CH4, CH5, CH8 |
| 5 ADC1 channels | CH0, CH2, CH4, CH5, CH6 |
| 4 CAN nodes | CAN0, CAN1, CAN2, CAN3 |
| 2 CAN nodes | CAN0, CAN1 |
| 6 serial channels | U0C0, U0C1, U1C0, U1C1, U2C0, U2C1 |
| 4 serial channels | U0C0, U0C1, U1C0, U1C1 |

## 2.1 Pin Configuration and Definition

The pins of the XE164 are described in detail in **Table 4**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. **Figure 2** summarizes all pins, showing their locations on the four sides of the package.

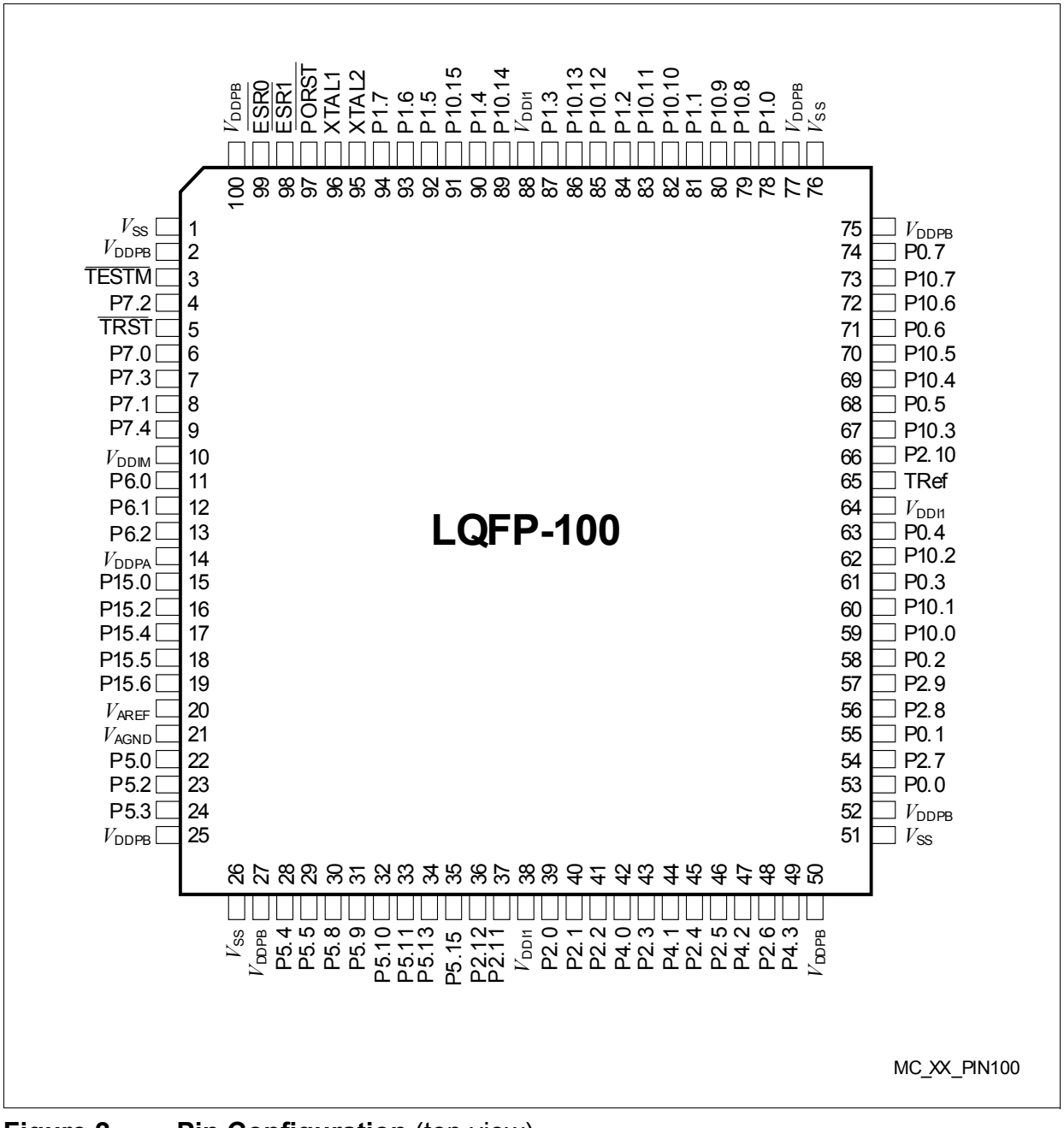


**Figure 2 Pin Configuration** (top view)

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 7 | P7.3 | O0 / I | St/B | **Bit 3 of Port 7, General Purpose Input/Output** |
| | EMUX1 | O1 | St/B | **External Analog MUX Control Output 1 (ADC1)** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_DOUT | O3 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU62_ CCPOS1A | I | St/B | **CCU62 Position Input 1** |
| | TMS_C | I | St/B | **JTAG Test Mode Selection Input** |
| | U0C1_DX0F | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| 8 | P7.1 | O0 / I | St/B | **Bit 1 of Port 7, General Purpose Input/Output** |
| | EXTCLK | O1 | St/B | **Programmable Clock Signal Output** |
| | CCU62_ CTRAPA | I | St/B | **CCU62 Emergency Trap Input** |
| | $\overline{\text{BRKIN\_C}}$ | I | St/B | **OCDS Break Signal Input** |
| 9 | P7.4 | O0 / I | St/B | **Bit 4 of Port 7, General Purpose Input/Output** |
| | EMUX2 | O1 | St/B | **External Analog MUX Control Output 2 (ADC1)** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C1_ SCLKOUT | O3 | St/B | **USIC0 Channel 1 Shift Clock Output** |
| | CCU62_ CCPOS2A | I | St/B | **CCU62 Position Input 2** |
| | TCK_C | I | St/B | **JTAG Clock Input** |
| | U0C0_DX0D | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX1E | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| 11 | P6.0 | O0 / I | St/A | **Bit 0 of Port 6, General Purpose Input/Output** |
| | EMUX0 | O1 | St/A | **External Analog MUX Control Output 0 (ADC0)** |
| | $\overline{\text{BRKOUT}}$ | O3 | St/A | **OCDS Break Signal Output** |
| | ADCx_ REQGTyC | I | St/A | **External Request Gate Input for ADC0/1** |
| | U1C1_DX0E | I | St/A | **USIC1 Channel 1 Shift Data Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 61 | P0.3 | O0 / I | St/B | **Bit 3 of Port 0, General Purpose Input/Output** |
| | U1C0_ SELO0 | O1 | St/B | **USIC1 Channel 0 Select/Control 0 Output** |
| | U1C1_ SELO1 | O2 | St/B | **USIC1 Channel 1 Select/Control 1 Output** |
| | CCU61_ COUT60 | O3 | St/B | **CCU61 Channel 0 Output** |
| | A3 | OH | St/B | **External Bus Interface Address Line 3** |
| | U1C0_DX2A | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | RxDC0B | I | St/B | **CAN Node 0 Receive Data Input** |
| 62 | P10.2 | O0 / I | St/B | **Bit 2 of Port 10, General Purpose Input/Output** |
| | U0C0_ SCLKOUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | CCU60_ CC62 | O2 / I | St/B | **CCU60 Channel 2 Input/Output** |
| | AD2 | OH / I | St/B | **External Bus Interface Address/Data Line 2** |
| | U0C0_DX1B | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| 63 | P0.4 | O0 / I | St/B | **Bit 4 of Port 0, General Purpose Input/Output** |
| | U1C1_ SELO0 | O1 | St/B | **USIC1 Channel 1 Select/Control 0 Output** |
| | U1C0_ SELO1 | O2 | St/B | **USIC1 Channel 0 Select/Control 1 Output** |
| | CCU61_ COUT61 | O3 | St/B | **CCU61 Channel 1 Output** |
| | A4 | OH | St/B | **External Bus Interface Address Line 4** |
| | U1C1_DX2A | I | St/B | **USIC1 Channel 1 Shift Control Input** |
| | RxDC1B | I | St/B | **CAN Node 1 Receive Data Input** |
| 65 | TRef | IO | Sp/1 | **Control Pin for Core Voltage Generation** 2) |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 2, 25, 27, 50, 52, 75, 77, 100 | $V_{DDPB}$ | - | PS/B | **Digital Pad Supply Voltage for Domain B**<br>Connect decoupling capacitors to adjacent $V_{DDP}/V_{SS}$ pin pairs as close as possible to the pins.<br>*Note: The on-chip voltage regulators and all ports except P5, P6, and P15 are fed from supply voltage $V_{DDPB}$.* |
| 1, 26, 51, 76 | $V_{SS}$ | - | PS/-- | **Digital Ground**<br>All $V_{SS}$ pins must be connected to the ground-line or ground-plane.<br>*Note: Also the exposed pad is connected to $V_{SS}$. The respective board area must be connected to ground (if soldered) or left free.* |

1) To generate the reference clock output for bus timing measurement, $f_{SYS}$ must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

2) Pin TRef was used to control the core voltage generation in step AA. For that step, pin TRef must be connected to $V_{DDPB}$.
This connection is no more required from step AB on. For the current step, pin TRef is logically not connected. Future derivatives will feature an additional general purpose IO pin at this position.

# 3 Functional Description

The architecture of the XE164 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE164.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE164.

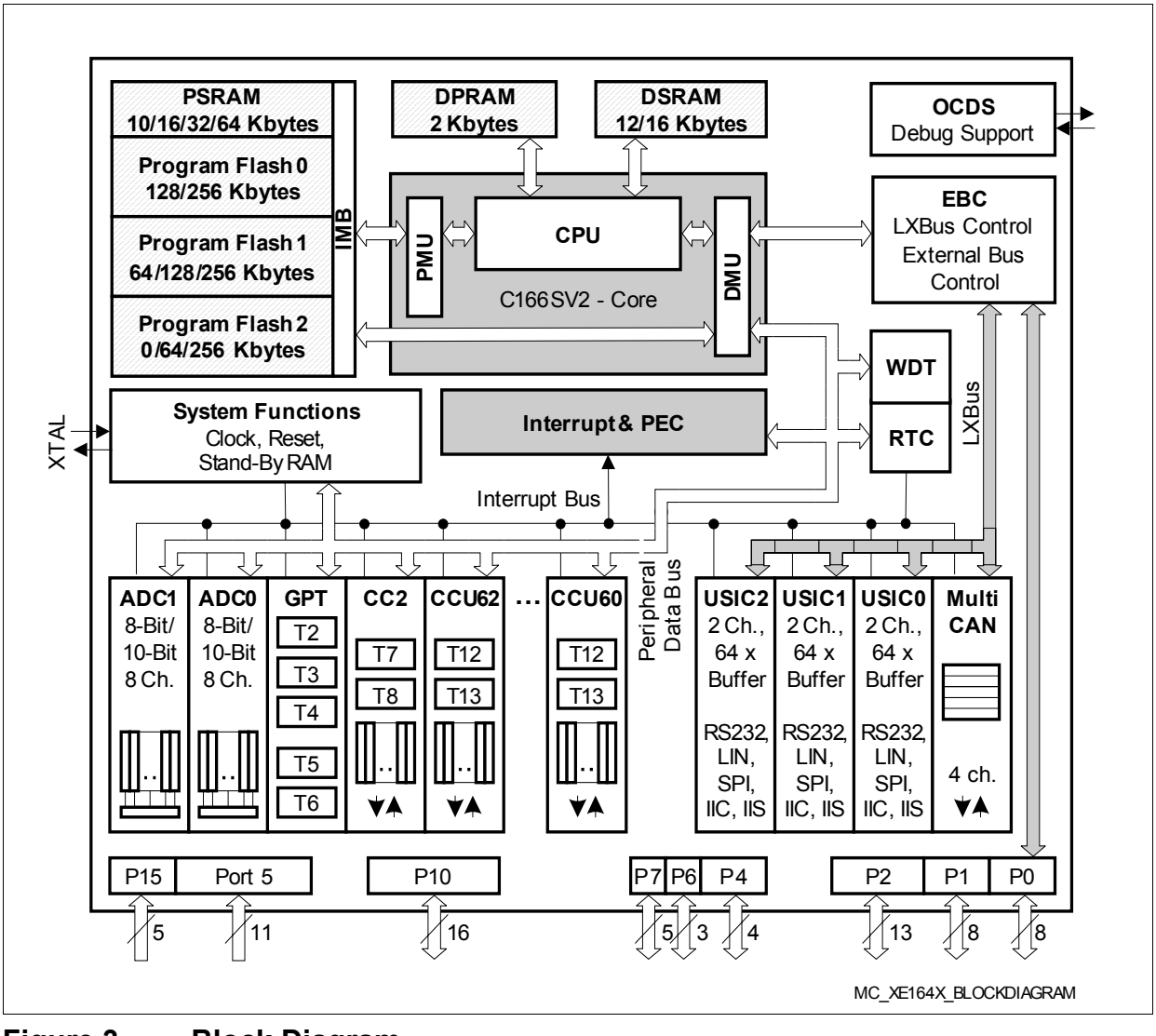


**Figure 3 Block Diagram**

## 3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to four external $\overline{CS}$ signals (three windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

## 3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

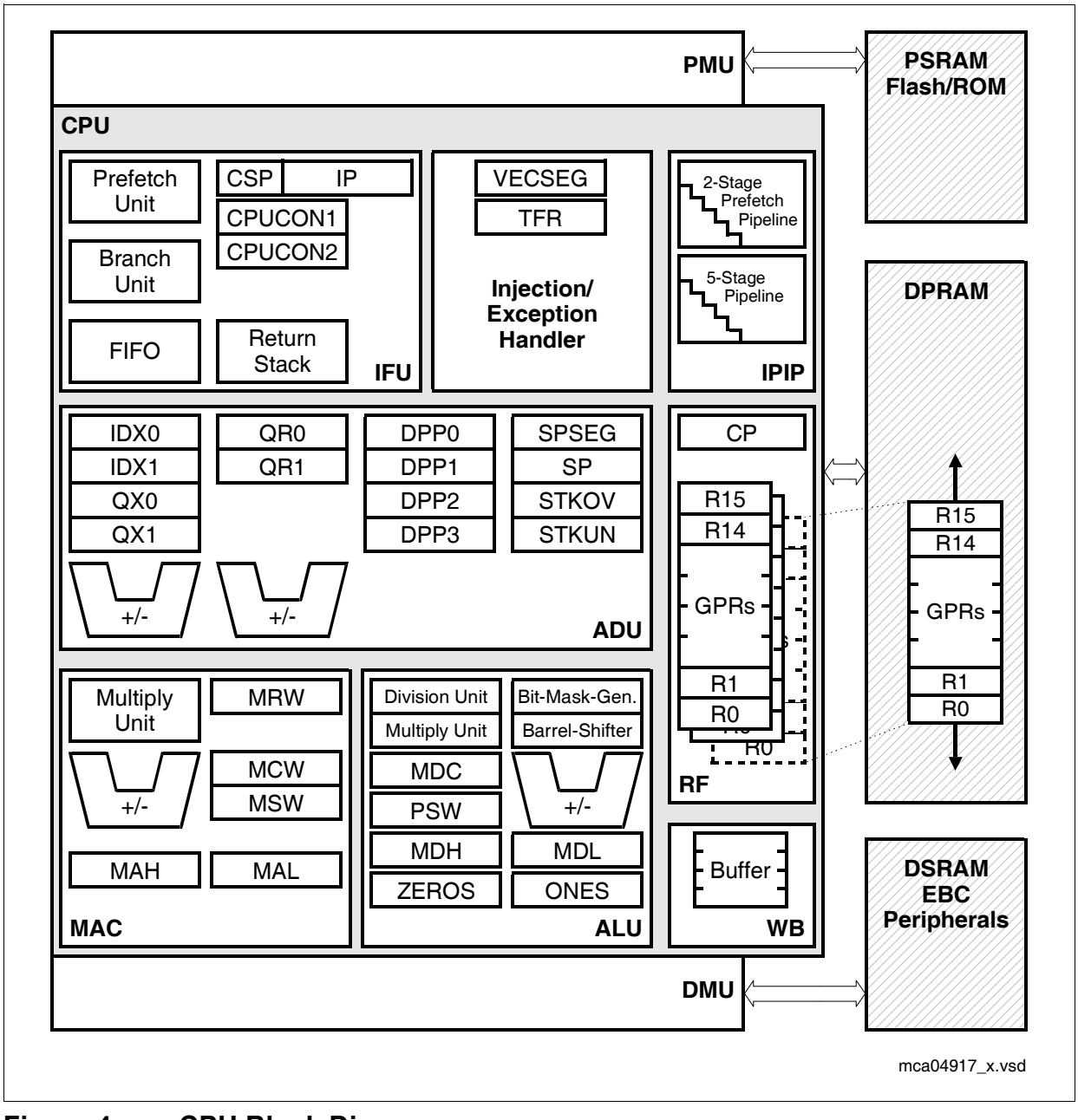


**Figure 4 CPU Block Diagram**

## 3.7 Capture/Compare Units CCU6x

The XE164 features up to three CCU6 units (CCU60, CCU61, CCU62).

The CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

### Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

### Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

### Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

## 3.9 Real Time Clock

The Real Time Clock (RTC) module of the XE164 can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

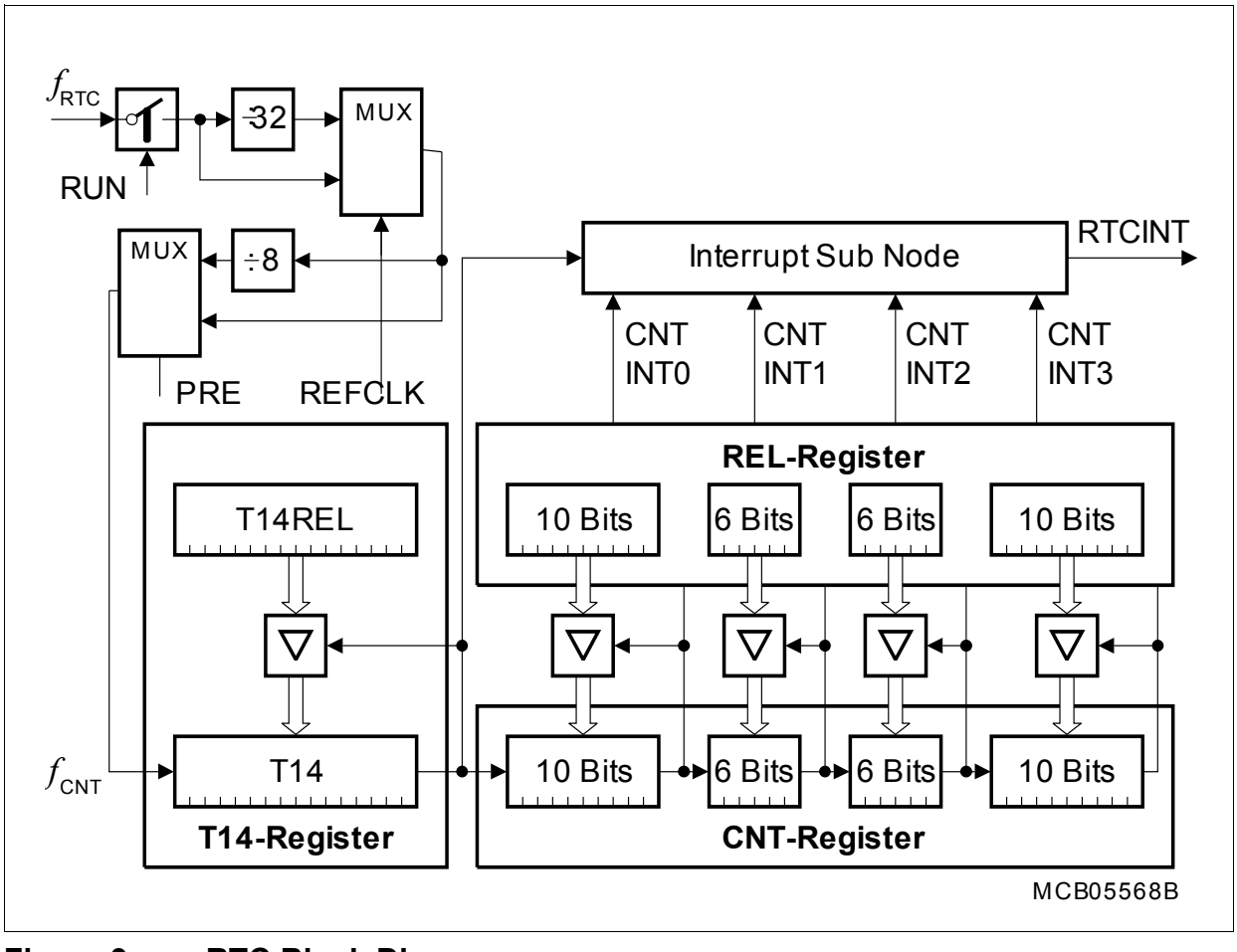


**Figure 9 RTC Block Diagram**

*Note: The registers associated with the RTC are only affected by a power reset.*

**Table 9 Summary of the XE164's Parallel Ports** (cont'd)

| Port | Width | Alternate Functions |
|---|---|---|
| Port 6 | 4 | ADC control lines,<br>Serial interface lines of USIC1,<br>Timer control signals,<br>OCDS control |
| Port 7 | 5 | ADC control lines,<br>Serial interface lines of USIC0,<br>Input/Output lines for CCU62,<br>Timer control signals,<br>JTAG, OCDS control,system clock output |
| Port 10 | 16 | Address and/or data lines, bus control,<br>Serial interface lines of USIC0, USIC1, CAN2 and CAN3,<br>Input/Output lines for CCU60,<br>JTAG, OCDS control |
| Port 15 | 8 | Analog input channels to ADC1,<br>Timer control signals |

## Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

**Table 12 Operating Condition Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital core supply voltage | $V_{DDI}$ | 1.4 | – | 1.6 | V | |
| Core Supply Voltage Difference | ΔVDDI | -10 | – | +10 | mV | $V_{DDIM}$ - $V_{DDI1}$ 1) |
| Digital supply voltage for IO pads and voltage regulators, upper voltage range | $V_{DDPA}$, $V_{DDPB}$ | 4.5 | – | 5.5 | V | 2) |
| Digital supply voltage for IO pads and voltage regulators, lower voltage range | $V_{DDPA}$, $V_{DDPB}$ | 3.0 | – | 4.5 | V | 2) |
| Digital ground voltage | $V_{SS}$ | 0 | – | 0 | V | Reference voltage |
| Overload current | $I_{OV}$ | -5 | – | 5 | mA | Per IO pin 3)4) |
| | | -2 | – | 5 | mA | Per analog input pin 3)4) |
| Overload positive current coupling factor for analog inputs 5) | $K_{OVA}$ | – | $1.0 \times 10^{-6}$ | $1.0 \times 10^{-4}$ | – | $I_{OV} > 0$ |
| Overload negative current coupling factor for analog inputs 5) | $K_{OVA}$ | – | $2.5 \times 10^{-4}$ | $1.5 \times 10^{-3}$ | – | $I_{OV} < 0$ |
| Overload positive current coupling factor for digital I/O pins 5) | $K_{OVD}$ | – | $1.0 \times 10^{-4}$ | $5.0 \times 10^{-3}$ | – | $I_{OV} > 0$ |
| Overload negative current coupling factor for digital I/O pins 5) | $K_{OVD}$ | – | $1.0 \times 10^{-2}$ | $3.0 \times 10^{-2}$ | – | $I_{OV} < 0$ |
| Absolute sum of overload currents | Σ\|IOV\| | – | – | 50 | mA | 4) |

## 4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE164 can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE164 are designed to operate in various driver modes. The DC parameter specifications refer to the current limits in **Table 13**.

**Table 13 Current Limits for Port Output Drivers**

| Port Output Driver Mode | Maximum Output Current ($I_{OLmax}$, $-I_{OHmax}$)[1] | | Nominal Output Current ($I_{OLnom}$, $-I_{OHnom}$) | |
|---|---|---|---|---|
| | $V_{DDP} \geq$ 4.5 V | $V_{DDP} <$ 4.5 V | $V_{DDP} \geq$ 4.5 V | $V_{DDP} <$ 4.5 V |
| **Strong driver** | 10 mA | 10 mA | 2.5 mA | 2.5 mA |
| **Medium driver** | 4.0 mA | 2.5 mA | 1.0 mA | 1.0 mA |
| **Weak driver** | 0.5 mA | 0.5 mA | 0.1 mA | 0.1 mA |

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring output pins, the total output current in each direction ($\Sigma I_{OL}$ and $\Sigma -I_{OH}$) must remain below 50 mA.

**Table 18 A/D Converter Characteristics** (cont'd)
**(Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Switched capacitance of the reference input | $C_{AREFS}$ | CC | – | 7 | pF | 6)7) |
| Resistance of the reference input path | $R_{AREF}$ | CC | – | 2 | kΩ | 6)7) |

1) TUE is tested at $V_{AREFx}$ = $V_{DDPA}$, $V_{AGND}$ = 0 V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see $I_{OV}$ specification) does not exceed 10 mA, and if $V_{AREF}$ and $V_{AGND}$ remain stable during the measurement time.
2) $V_{AIN}$ may exceed $V_{AGND}$ or $V_{AREFx}$ up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
3) The limit values for $f_{ADCI}$ must not be exceeded when selecting the peripheral frequency and the prescaler setting.
4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock $t_{ADCI}$ depend on programming and are found in **Table 19**.
5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.
6) Not subject to production test - verified by design/characterization.
7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, $R_{AINtyp}$ = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

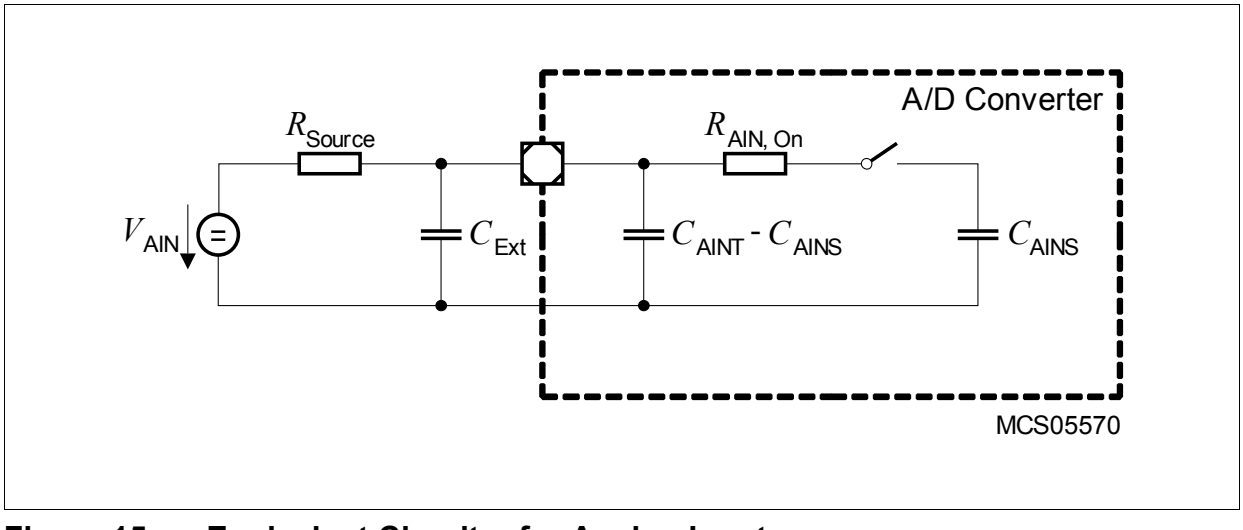


**Figure 15 Equivalent Circuitry for Analog Inputs**

**Table 24 Flash Access Waitstates**

| Required Waitstates | System Frequency Range |
|---|---|
| 4 WS (WSFLASH = $100_B$) | $f_{SYS} \leq f_{SYSmax}$ |
| 3 WS (WSFLASH = $011_B$) | $f_{SYS} \leq 17$ MHz |
| 2 WS (WSFLASH = $010_B$) | $f_{SYS} \leq 13$ MHz |
| 1 WS (WSFLASH = $001_B$) | $f_{SYS} \leq 8$ MHz |
| 0 WS (WSFLASH = $000_B$) | Forbidden! Must not be selected! |

*Note: The maximum achievable system frequency is limited by the properties of the respective derivative.*

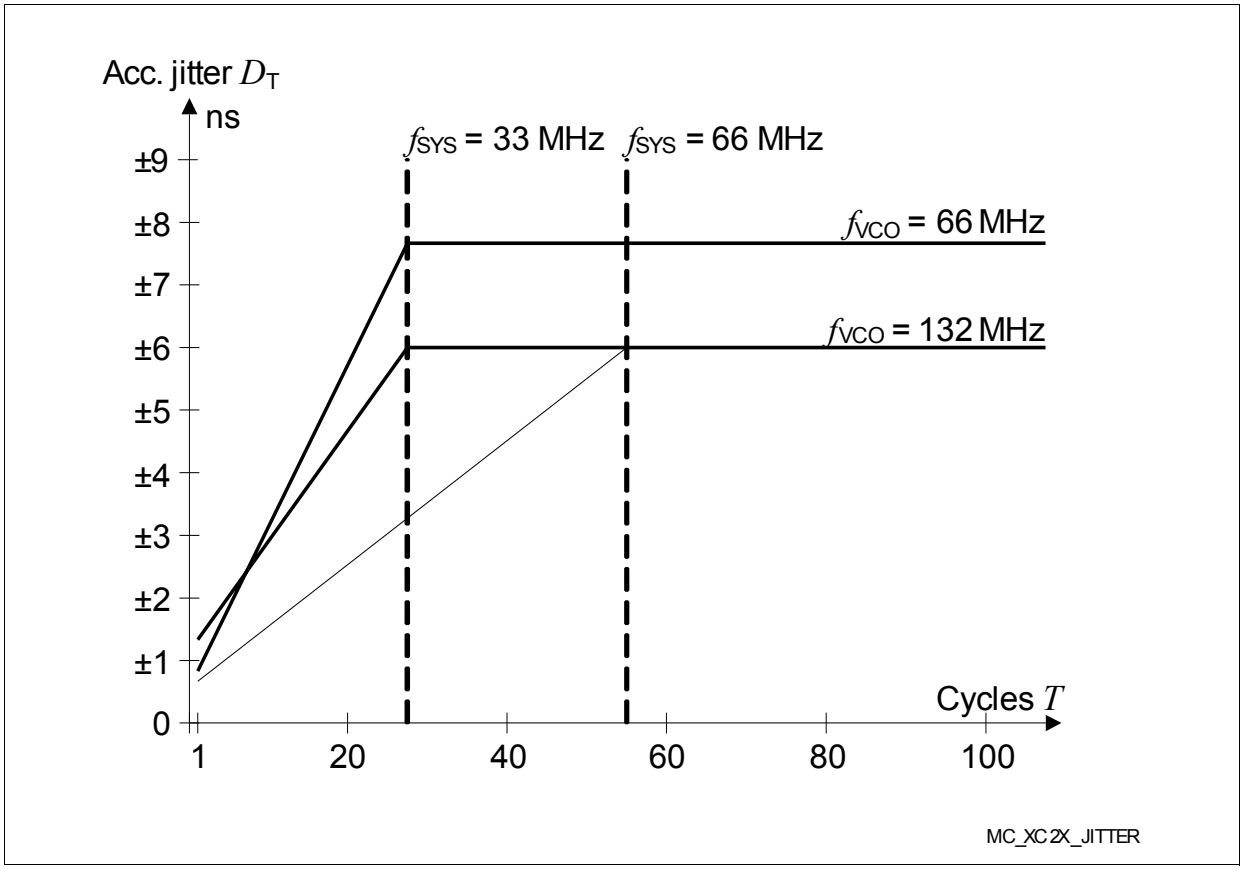


**Figure 19 Approximated Accumulated PLL Jitter**

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L$ = 20 pF (see **Table 12**).*
*The maximum peak-to-peak noise on the pad supply voltage (measured between $V_{DDPB}$ pin 100/144 and $V_{SS}$ pin 1) is limited to a peak-to-peak voltage of $V_{PP}$ = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.*

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

**Table 25 VCO Bands for PLL Operation[1)]**

| PLLCON0.VCOSEL | VCO Frequency Range | Base Frequency Range |
|---|---|---|
| 00 | 50 … 110 MHz | 10 … 40 MHz |
| 01 | 100 … 160 MHz | 20 … 80 MHz |
| 1X | Reserved | |

1) Not subject to production test - verified by design/characterization.

### 4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels $V_{IL}$ and $V_{IH}$. In connected to XTAL1, a minimum amplitude $V_{AX1}$ (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

*Note: The given clock timing parameters ($t_1$ … $t_4$) are only valid for an external clock input signal.*

**Table 26 External Clock Input Characteristics (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input voltage range limits for signal on XTAL1 | $V_{IX1}$ SR | -1.7 + $V_{DDI}$ | – | 1.7 | V | 1) |
| Input voltage (amplitude) on XTAL1 | $V_{AX1}$ SR | 0.3 × $V_{DDI}$ | – | – | V | Peak-to-peak voltage2) |
| XTAL1 input current | $I_{IL}$ CC | – | – | ±20 | µA | 0 V < $V_{IN}$ < $V_{DDI}$ |
| Oscillator frequency | $f_{OSC}$ CC | 4 | – | 40 | MHz | Clock signal |
| | | 4 | – | 16 | MHz | Crystal or Resonator |
| High time | $t_1$ SR | 6 | – | – | ns | |
| Low time | $t_2$ SR | 6 | – | – | ns | |
| Rise time | $t_3$ SR | – | 8 | 8 | ns | |
| Fall time | $t_4$ SR | – | 8 | 8 | ns | |

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage $V_{AX1}$ refers to the offset voltage $V_{OFF}$. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by $V_{IX1}$.

### 4.6.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 33 JTAG Interface Timing Parameters (Operating Conditions apply)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK clock period | $t_1$ SR | 60 | 50 | – | ns | – |
| TCK high time | $t_2$ SR | 16 | – | – | ns | – |
| TCK low time | $t_3$ SR | 16 | – | – | ns | – |
| TCK clock rise time | $t_4$ SR | – | – | 8 | ns | – |
| TCK clock fall time | $t_5$ SR | – | – | 8 | ns | – |
| TDI/TMS setup to TCK rising edge | $t_6$ SR | 6 | – | – | ns | – |
| TDI/TMS hold after TCK rising edge | $t_7$ SR | 6 | – | – | ns | – |
| TDO valid after TCK falling edge[1] | $t_8$ CC | – | – | 30 | ns | $C_L$ = 50 pF |
| | $t_8$ CC | 10 | – | – | ns | $C_L$ = 20 pF |
| TDO high imped. to valid from TCK falling edge[1)2)] | $t_9$ CC | – | – | 30 | ns | $C_L$ = 50 pF |
| TDO valid to high imped. from TCK falling edge[1)] | $t_{10}$ CC | – | – | 30 | ns | $C_L$ = 50 pF |

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.