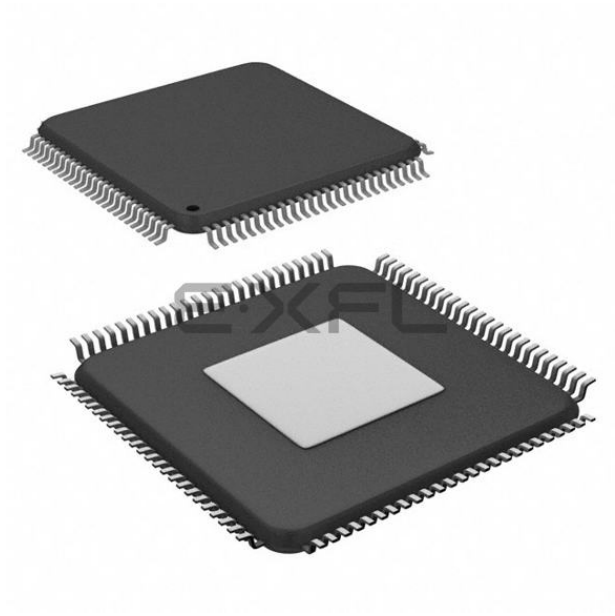
Infineon Technologies - XE164G96F66LACFXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164g96f66lacfxqma1

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1 Summary of Features

For a quick overview and easy reference, the features of the XE164 are summarized here.

- High-performance CPU with five-stage pipeline
  - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
- Interrupt system with 16 priority levels for up to 83 sources
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- On-chip memory modules
  - 1 Kbyte on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 64 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 768 Kbytes on-chip program memory (Flash memory)
- On-Chip Peripheral Modules
  - Two Synchronizable A/D Converters with up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check)
  - 16-channel general purpose capture/compare unit (CAPCOM2)
  - Up to three capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers

  - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 4 CAN nodes and gateway functionality
  - On-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 75 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For ordering codes for the XE164 please contact your sales representative or local distributor.

This document describes several derivatives of the XE164 group. **Table 1** lists these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity the term **XE164** is used for all derivatives throughout this document.

The XE164 types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

Table 2 Flash Memory Allocation

Total Flash Size	Flash Area A[1)]	Flash Area B	Flash Area C
768 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $CB'FFFF_H$	n.a.
576 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C8'FFFF_H$	n.a.
384 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C5'FFFF_H$	n.a.
192 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'FFFF_H$	$C4'0000_H$ … $C4'FFFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE164 types are offered with different interface options. **Table 3** lists the available channels for each option.

Table 3 Interface Channel Association

Total Number	Available Channels
11 ADC0 channels	CH0, CH2 … CH5, CH8 … CH11, CH13, CH15
6 ADC0 channels	CH0, CH2, CH3, CH4, CH5, CH8
5 ADC1 channels	CH0, CH2, CH4, CH5, CH6
4 CAN nodes	CAN0, CAN1, CAN2, CAN3
2 CAN nodes	CAN0, CAN1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1
4 serial channels	U0C0, U0C1, U1C0, U1C1

Notes to Pin Definitions

1. ***Ctrl.**: The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bitfield PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.*
   Output signal OH is controlled by hardware.
2. ***Type**: Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).*

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	**Bit 2 of Port 7, General Purpose Input/Output**
	EMUX0	O1	St/B	**External Analog MUX Control Output 0 (ADC1)**
	CCU62_ CCPOS0A	I	St/B	**CCU62 Position Input 0**
	TDI_C	I	St/B	**JTAG Test Data Input**
5	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE164's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
6	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT1 Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT2 Timer T6 Toggle Latch Output**
	TDO_A	OH	St/B	**JTAG Test Data Output**
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CC2_16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	A16	OH	St/B	**External Bus Interface Address Line 16**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC0A	I	St/B	**CAN Node 0 Receive Data Input**
44	P4.1	O0 / I	St/B	**Bit 1 of Port 4, General Purpose Input/Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_25	O3 / I	St/B	**CAPCOM2 CC25IO Capture Inp./ Compare Out.**
	$\overline{CS1}$	OH	St/B	**External Bus Interface Chip Select 1 Output**
45	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	A17	OH	St/B	**External Bus Interface Address Line 17**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
46	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_ SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	A18	OH	St/B	**External Bus Interface Address Line 18**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
98	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
	EX0AINB	I	St/B	**External Interrupt Trigger Input**
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** *Note: After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.*
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see **Table 12** for details.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see **Table 12** for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6, and P15 are fed from supply voltage V_{DDPA}.*

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 25, 27, 50, 52, 75, 77, 100	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6, and P15 are fed from supply voltage V_{DDPB}.*
1, 26, 51, 76	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected to V_{SS}. The respective board area must be connected to ground (if soldered) or left free.*

1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

2) Pin TRef was used to control the core voltage generation in step AA. For that step, pin TRef must be connected to V_{DDPB}.
This connection is no more required from step AB on. For the current step, pin TRef is logically not connected. Future derivatives will feature an additional general purpose IO pin at this position.

3.6 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to a number of prescaled values of the internal system clock. It may also be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range for the timer period and resolution while allowing precise adjustments for application-specific requirements. An external count input for CAPCOM2 timer T7 allows event scheduling for the capture/compare registers with respect to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers. Each may be individually allocated to either CAPCOM2 timer T7 or T8 and programmed for a capture or compare function.
12 registers of the CAPCOM2 module have one port pin associated with it. This serves as an input pin to trigger the capture function or as an output pin to indicate the occurrence of a compare event.

Table 8 Compare Modes (CAPCOM2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

3.11 Universal Serial Interface Channel Modules (USIC)

The XE164 includes up to three USIC modules (USIC0, USIC1, USIC2), each providing two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

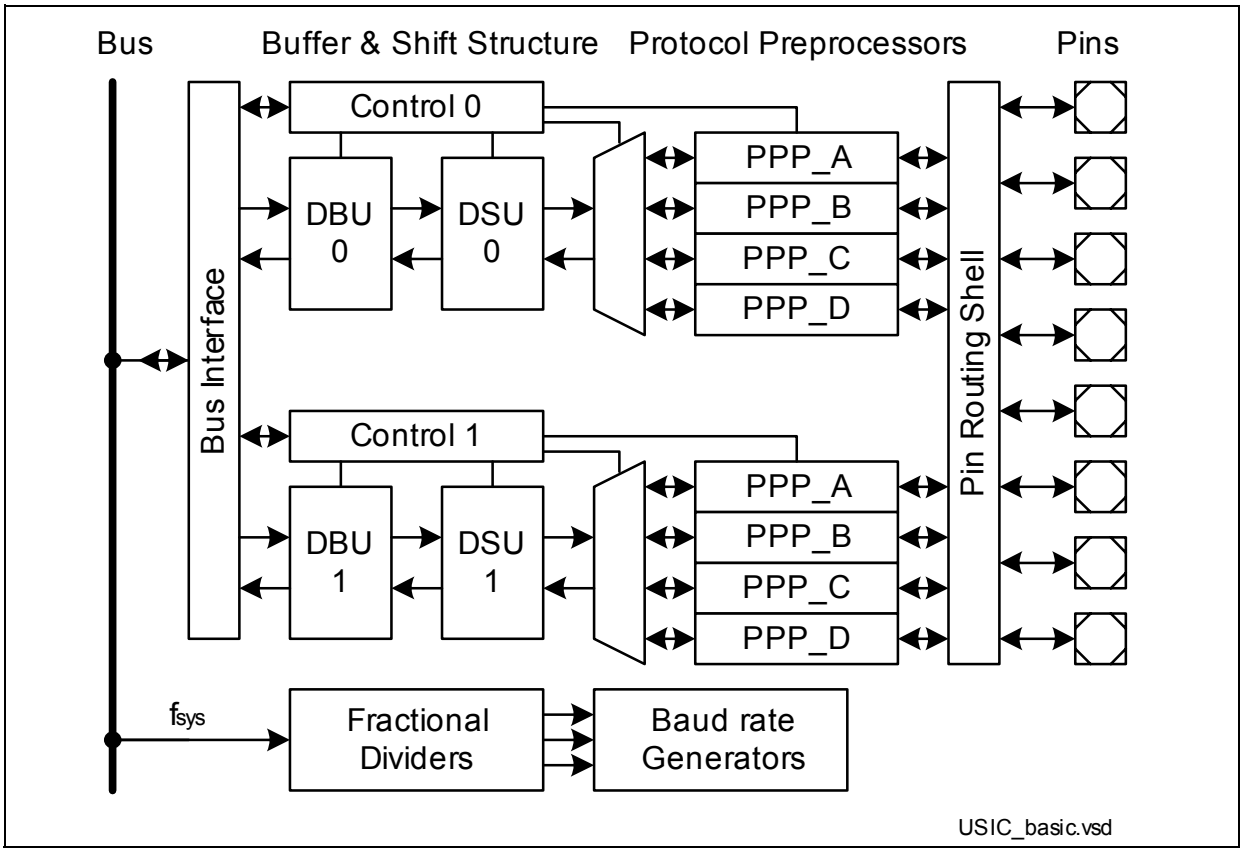

Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - maximum baud rate: f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - maximum baud rate: f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
  - maximum baud rate in slave mode: f_{SYS}
  - maximum baud rate in master mode: f_{SYS} / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - maximum baud rate: f_{SYS} / 2 for transmitter, f_{SYS} for receiver

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to four independent CAN nodes
- 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE164, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

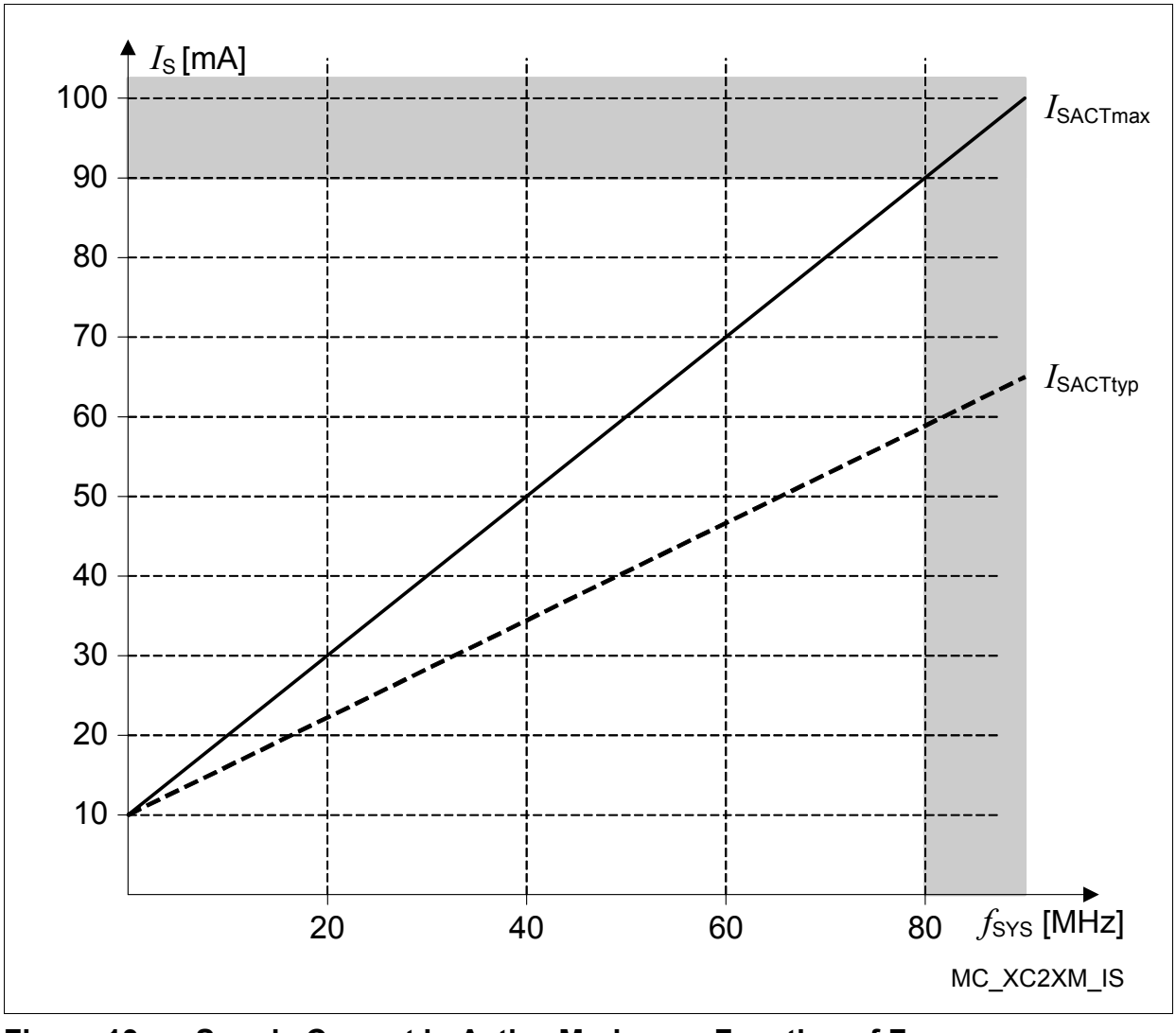

Figure 13 Supply Current in Active Mode as a Function of Frequency

Table 17 Leakage Power Consumption XE164 (Operating Conditions apply)

Parameter	Sym-bol	Values			Unit	Note / Test Condition[1]
		Min.	Typ.	Max.		
Leakage supply current[2] Formula[3]: 600,000 × $e^{-\alpha}$; α = 5000 / (273 + B×T_J); Typ.: B = 1.0, Max.: B = 1.3	I_{LK1}	–	0.03	0.05	mA	T_J = 25°C
		–	0.5	1.3	mA	T_J = 85°C
		–	2.1	6.2	mA	T_J = 125°C

1) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

2) The supply current caused by leakage depends mainly on the junction temperature (see **Figure 14**) and the supply voltage. The temperature difference between the junction temperature T_J and the ambient temperature T_A must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.

3) This formula is valid for temperatures above 0°C. For temperatures below 0°C a value of below 10 µA can be assumed.

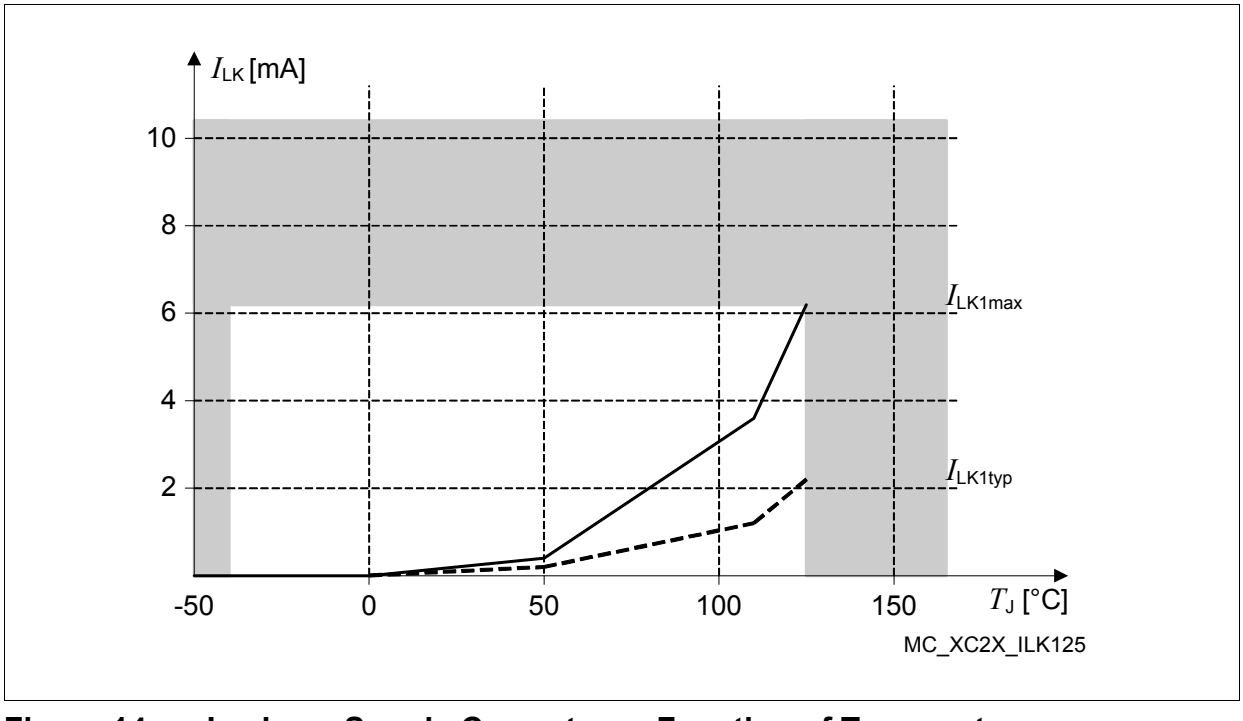

Figure 14 Leakage Supply Current as a Function of Temperature

Table 21 Coding of Bitfields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	2.9 V	
0001_B	3.0 V	LEV1V: reset request
0010_B	3.1 V	
0011_B	3.2 V	
0100_B	3.3 V	
0101_B	3.4 V	
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B	4.6 V	
1011_B	4.7 V	
1100_B	4.8 V	
1101_B	4.9 V	
1110_B	5.0 V	
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B	0.9 V	
001_B	1.0 V	
010_B	1.1 V	
011_B	1.2 V	
100_B	1.3 V	LEV1V: reset request
101_B	1.4 V	LEV2V: interrupt request
110_B	1.5 V	
111_B	1.6 V	

1) The indicated default levels are selected automatically after a power reset.

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. In connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Table 26 External Clock Input Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDI}	–	1.7	V	1)
Input voltage (amplitude) on XTAL1	V_{AX1} SR	0.3 × V_{DDI}	–	–	V	Peak-to-peak voltage2)
XTAL1 input current	I_{IL} CC	–	–	±20	µA	0 V < V_{IN} < V_{DDI}
Oscillator frequency	f_{OSC} CC	4	–	40	MHz	Clock signal
		4	–	16	MHz	Crystal or Resonator
High time	t_1 SR	6	–	–	ns	
Low time	t_2 SR	6	–	–	ns	
Rise time	t_3 SR	–	8	8	ns	
Fall time	t_4 SR	–	8	8	ns	

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

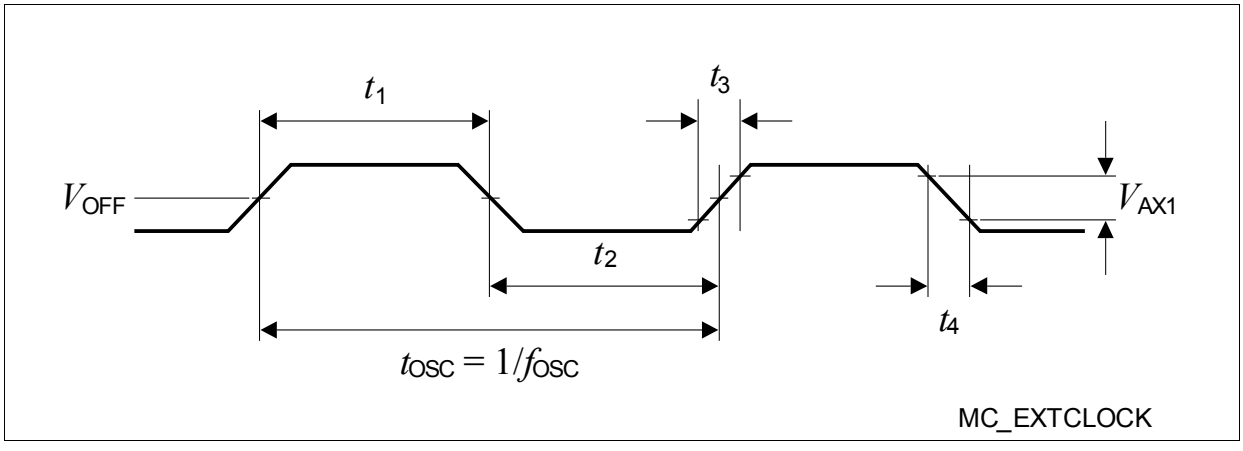

Figure 20 External Clock Drive XTAL1

Note: For crystal/resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.
Please refer to the limits specified by the crystal/resonator supplier.

4.6.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 33 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	60	50	–	ns	–
TCK high time	t_2 SR	16	–	–	ns	–
TCK low time	t_3 SR	16	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	8	ns	–
TCK clock fall time	t_5 SR	–	–	8	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1]	t_8 CC	–	–	30	ns	C_L = 50 pF
	t_8 CC	10	–	–	ns	C_L = 20 pF
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	30	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1)]	t_{10} CC	–	–	30	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.