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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164h96f66lacfxqma1

XE164

16-Bit Single-Chip

Real Time Signal Controller

Microcontrollers



Never stop thinking

XE164

Revision History: V2.1, 2008-08

Previous Version(s):

V2.0, 2008-03, Preliminary

V0.1, 2007-09, Preliminary

Page	Subjects (major changes since last revision)
several	Maximum frequency changed to 80 MHz
8	Specification of 6 ADC0 channels corrected
14f	Missing ADC0 channels added
28	Voltage domain for XTAL1/XTAL2 corrected to M
68	Coupling factors corrected
73, 75	Improved leakage parameters
74, 76	Pin leakage formula corrected
81	Improved ADC error values
94f	Improved definition of external clock parameters
107	JTAG clock speed corrected

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?

Your feedback will help us to continuously improve the quality of this document.

Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



Summary of Features

- Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
- On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 4 CAN nodes and gateway functionality
- On-chip real time clock
- Up to 12 Mbytes external address space for code and data
 - Programmable external bus characteristics for different address ranges
 - Multiplexed or demultiplexed external address/data buses
 - Selectable address bus width
 - 16-bit or 8-bit data bus width
 - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 75 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For ordering codes for the XE164 please contact your sales representative or local distributor.

This document describes several derivatives of the XE164 group. **Table 1** lists these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity the term **XE164** is used for all derivatives throughout this document.

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
54	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
55	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC61	O3 / I	St/B	CCU61 Channel 1 Input/Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input
56	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output 1)
	CC2_21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input
57	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input
	TCK_A	I	St/B	JTAG Clock Input

3 Functional Description

The architecture of the XE164 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see [Figure 3](#)). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE164.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE164.

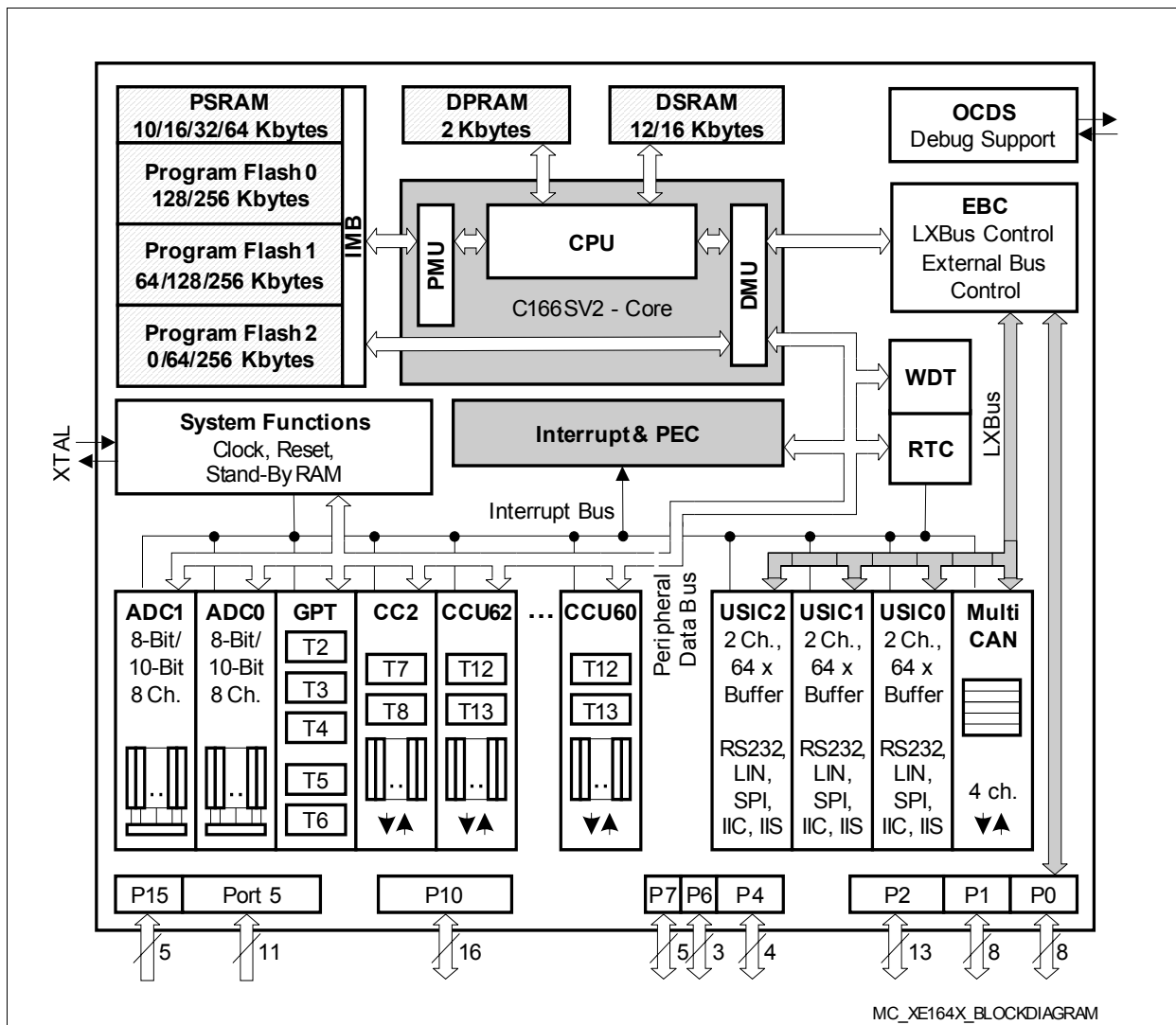


Figure 3 Block Diagram

Functional Description

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

Functional Description

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD¹⁾). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE164 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

1) Exception: T5EUD is not connected to a pin.

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
 - maximum baud rate: $f_{\text{SYS}} / 4$
 - data frame length programmable from 1 to 63 bits
 - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
 - maximum baud rate: $f_{\text{SYS}} / 16$
 - checksum generation under software control
 - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
 - maximum baud rate in slave mode: f_{SYS}
 - maximum baud rate in master mode: $f_{\text{SYS}} / 2$, limited by loop delay
 - number of data bits programmable from 1 to 63, more with explicit stop condition
 - MSB or LSB first
 - optional control of slave select signals
- **IIC** (Inter-IC Bus)
 - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
 - maximum baud rate: $f_{\text{SYS}} / 2$ for transmitter, f_{SYS} for receiver

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to four independent CAN nodes
- 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
 - Can be assigned to one of the CAN nodes
 - Configurable as transmit or receive objects, or as message buffer FIFO
 - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
 - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

Table 9 **Summary of the XE164's Parallel Ports (cont'd)**

Port	Width	Alternate Functions
Port 6	4	ADC control lines, Serial interface lines of USIC1, Timer control signals, OCDS control
Port 7	5	ADC control lines, Serial interface lines of USIC0, Input/Output lines for CCU62, Timer control signals, JTAG, OCDS control, system clock output
Port 10	16	Address and/or data lines, bus control, Serial interface lines of USIC0, USIC1, CAN2 and CAN3, Input/Output lines for CCU60, JTAG, OCDS control
Port 15	8	Analog input channels to ADC1, Timer control signals

3.16 Instruction Set Summary

Table 10 lists the instructions of the XE164.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Table 10 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Pullup/Pulldown Device Behavior

Most pins of the XE164 feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 12** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

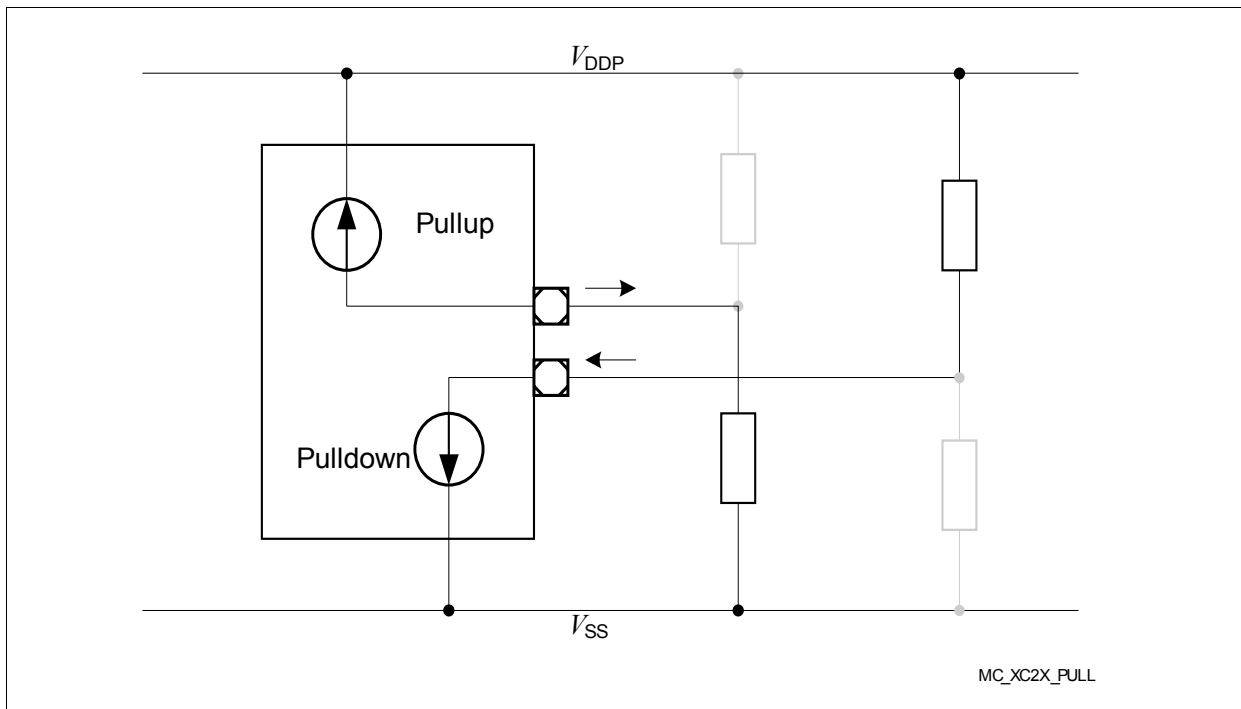


Figure 12 Pullup/Pulldown Current Definition

Table 17 Leakage Power Consumption XE164
(Operating Conditions apply)

Parameter	Sym- bol	Values			Unit	Note / Test Condition ¹⁾
		Min.	Typ.	Max.		
Leakage supply current ²⁾ Formula ³⁾ : $600,000 \times e^{-\alpha}$; $\alpha = 5000 / (273 + B \times T_J)$; Typ.: $B = 1.0$, Max.: $B = 1.3$	I_{LK1}	–	0.03	0.05	mA	$T_J = 25^\circ\text{C}$
		–	0.5	1.3	mA	$T_J = 85^\circ\text{C}$
		–	2.1	6.2	mA	$T_J = 125^\circ\text{C}$

- 1) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at $V_{DDP} - 0.1$ V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.
- 2) The supply current caused by leakage depends mainly on the junction temperature (see [Figure 14](#)) and the supply voltage. The temperature difference between the junction temperature T_J and the ambient temperature T_A must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.
- 3) This formula is valid for temperatures above 0°C . For temperatures below 0°C a value of below 10 μA can be assumed.

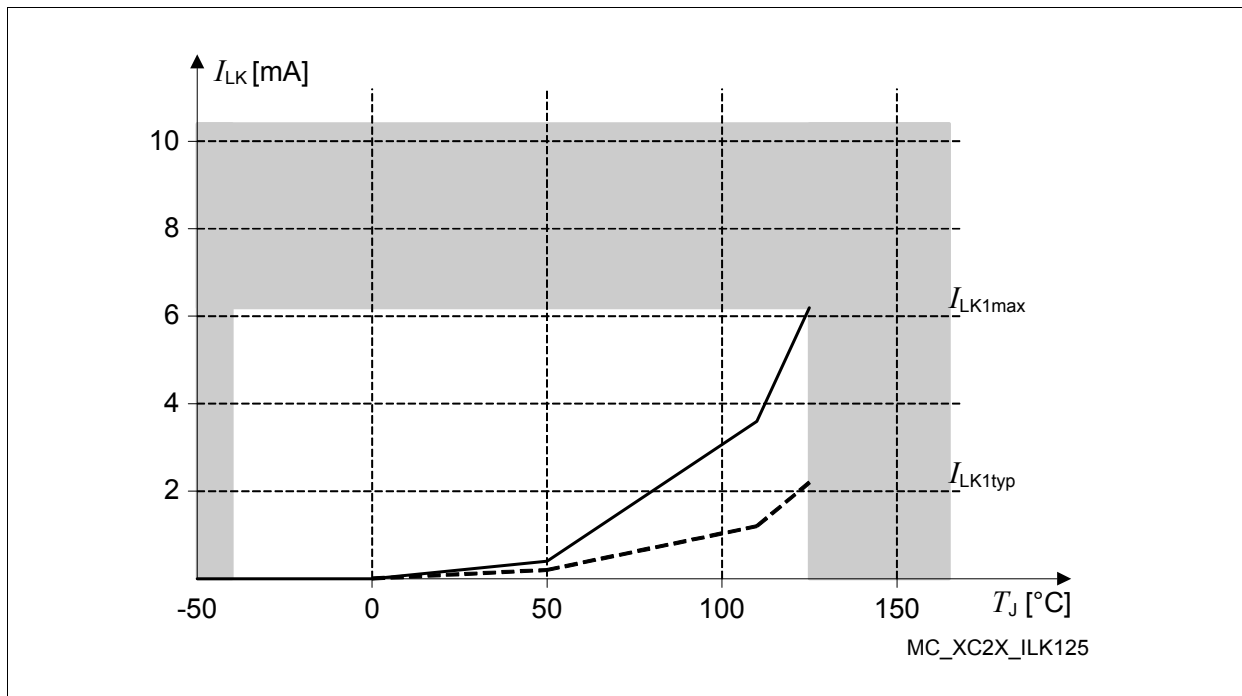


Figure 14 Leakage Supply Current as a Function of Temperature

Table 18 A/D Converter Characteristics (cont'd)
(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Switched capacitance of the reference input	C_{AREFS}	CC	–	7	pF	6)7)
Resistance of the reference input path	R_{AREF}	CC	–	2	k Ω	6)7)

- 1) TUE is tested at $V_{AREFX} = V_{DDPA}$, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.
- 2) V_{AIN} may exceed V_{AGND} or V_{AREFX} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.
- 3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
- 4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{ADCI} depend on programming and are found in [Table 19](#).
- 5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.
- 6) Not subject to production test - verified by design/characterization.
- 7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
 $C_{AINTtyp} = 12$ pF, $C_{AINStyp} = 5$ pF, $R_{AINTtyp} = 1.0$ k Ω , $C_{AREFTtyp} = 15$ pF, $C_{AREFStyp} = 10$ pF, $R_{AREFTtyp} = 1.0$ k Ω .

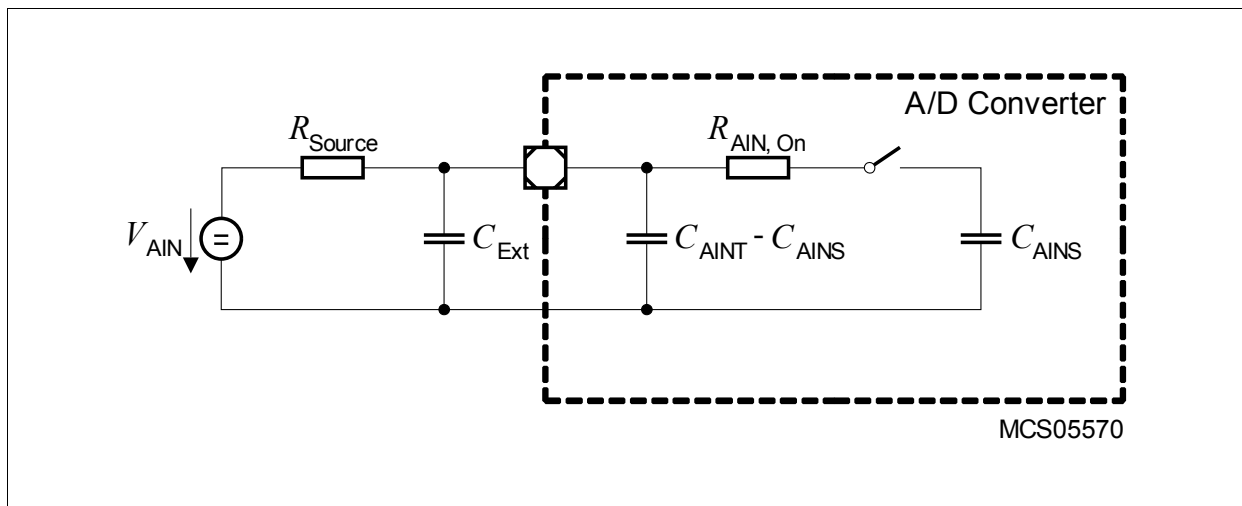


Figure 15 Equivalent Circuitry for Analog Inputs

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$$f_{\text{SYS}} = f_{\text{IN}}$$

The frequency of f_{SYS} is the same as the frequency of f_{IN} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN} .

Selecting Bypass Operation from the XTAL1¹⁾ input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$$f_{\text{SYS}} = f_{\text{OSC}} / K1.$$

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$$f_{\text{SYS}} = f_{\text{OSC}} / 1024.$$

Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{\text{SYS}} = f_{\text{IN}} \times \mathbf{F}$).

F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):

$$(\mathbf{F} = N / (P \times K2)).$$

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN} . The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDI1} .

Wakeup Clock

When wakeup operation is selected ($\text{SYSCON0.CLKSEL} = 00_{\text{B}}$), the system clock is derived from the low-frequency wakeup clock source:

$$f_{\text{SYS}} = f_{\text{WU}}$$

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bitfields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.

Please refer to the Programmer's Guide.

Variable Memory Cycles

External bus cycles of the XE164 are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 28 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 ... 2 TCS) can be extended by 0 ... 3 TCS if the address window is changed	tpAB	1 ... 2 (5)	TCS
Command delay phase	tpC	0 ... 3	TCS
Write Data setup/MUX Tristate phase	tpD	0 ... 1	TCS
Access phase	tpE	1 ... 32	TCS
Address/Write Data hold phase	tpF	0 ... 3	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Timing values are listed in [Table 29](#) and [Table 30](#). The shaded parameters have been verified by characterization. They are not subject to production test.

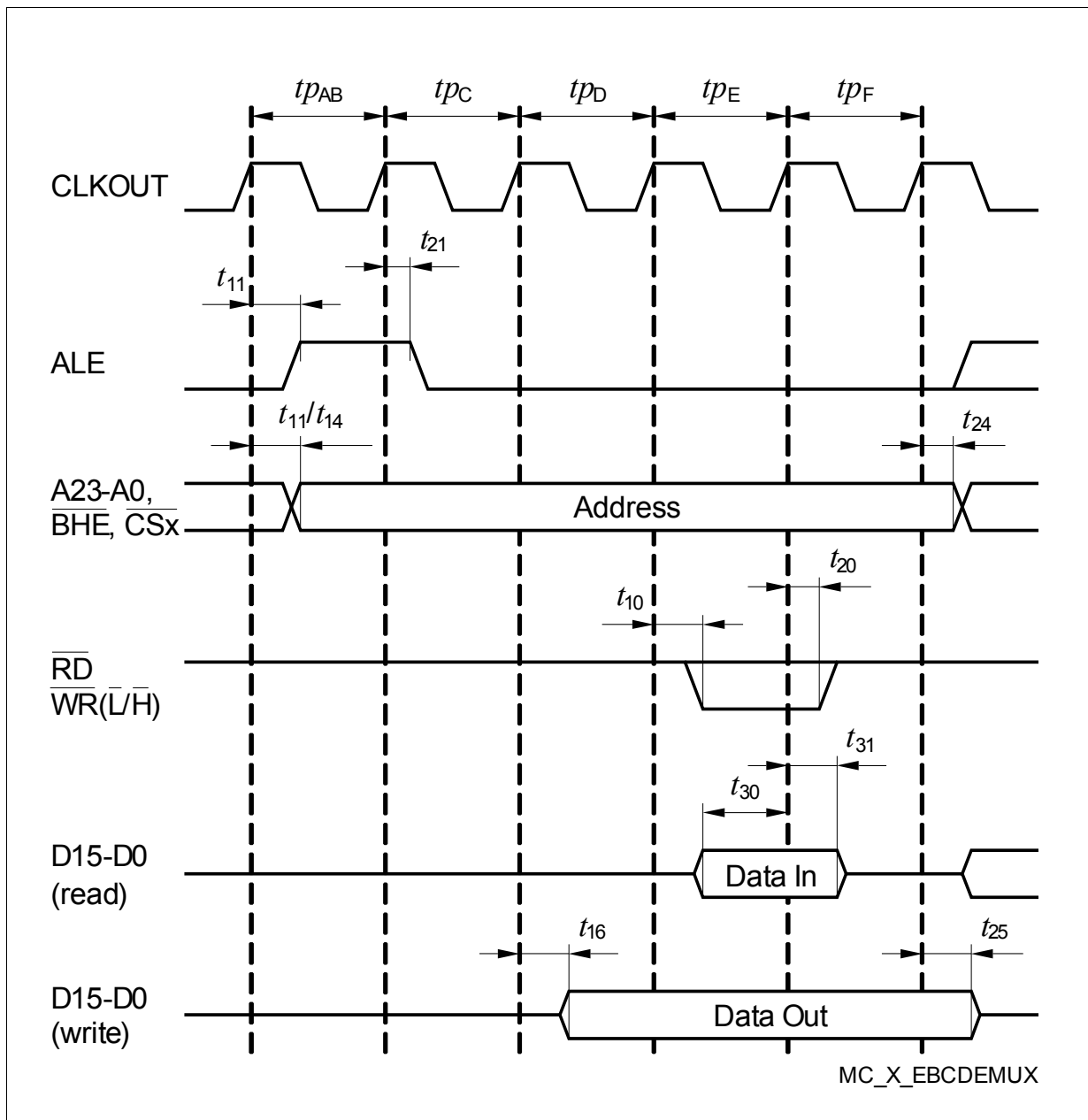


Figure 23 Demultiplexed Bus Cycle

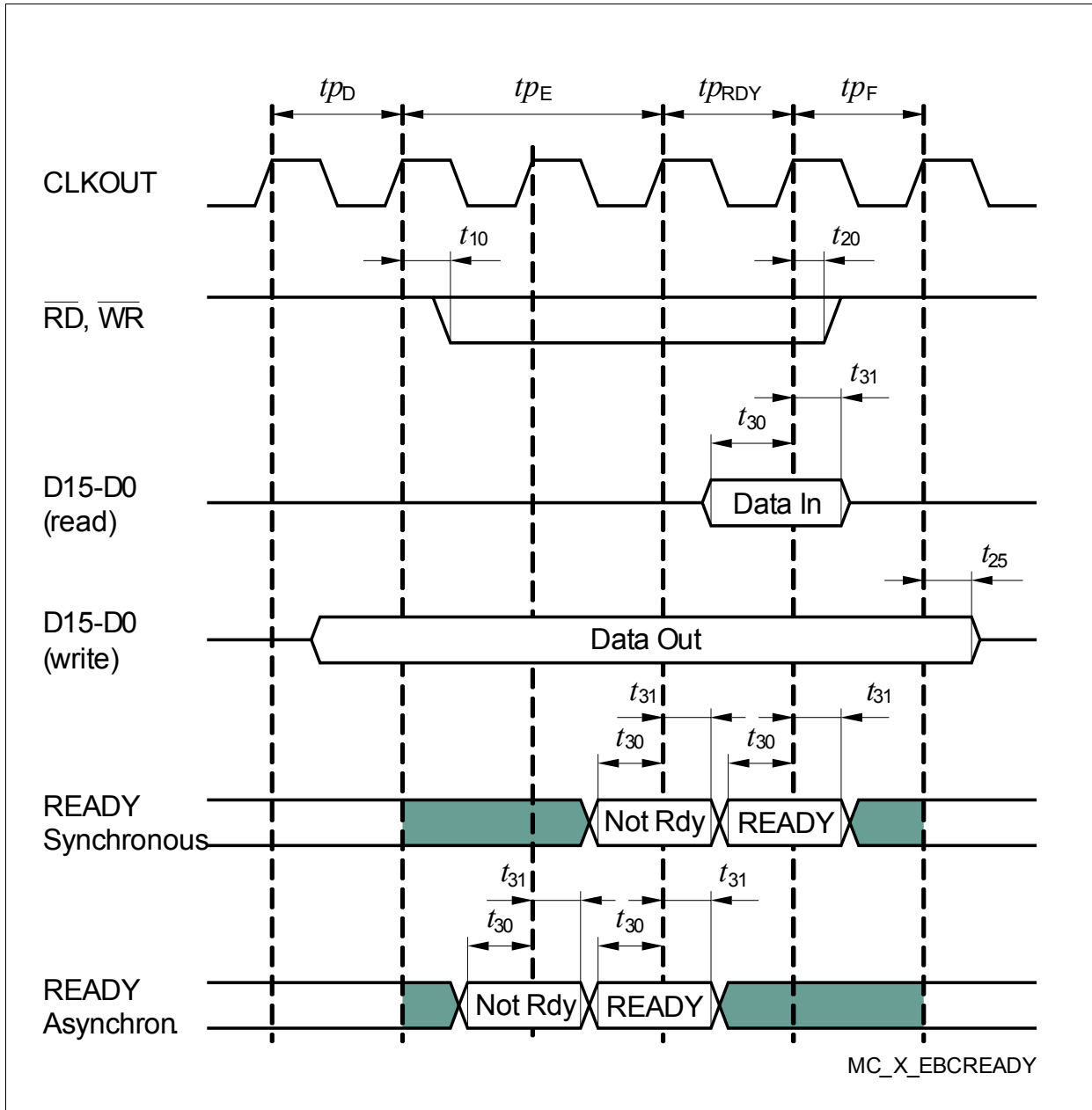


Figure 24 **READY Timing**

Note: If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (t_{pRDY}), sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle.

Note the different sampling points for synchronous and asynchronous READY. This example uses one mandatory waitstate (see t_{pE}) before the READY input value is used.

4.6.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 33 JTAG Interface Timing Parameters
(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	60	50	—	ns	—
TCK high time	t_2 SR	16	—	—	ns	—
TCK low time	t_3 SR	16	—	—	ns	—
TCK clock rise time	t_4 SR	—	—	8	ns	—
TCK clock fall time	t_5 SR	—	—	8	ns	—
TDI/TMS setup to TCK rising edge	t_6 SR	6	—	—	ns	—
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	—
TDO valid after TCK falling edge ¹⁾	t_8 CC	—	—	30	ns	$C_L = 50$ pF
	t_8 CC	10	—	—	ns	$C_L = 20$ pF
TDO high imped. to valid from TCK falling edge ¹⁾²⁾	t_9 CC	—	—	30	ns	$C_L = 50$ pF
TDO valid to high imped. from TCK falling edge ¹⁾	t_{10} CC	—	—	30	ns	$C_L = 50$ pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.