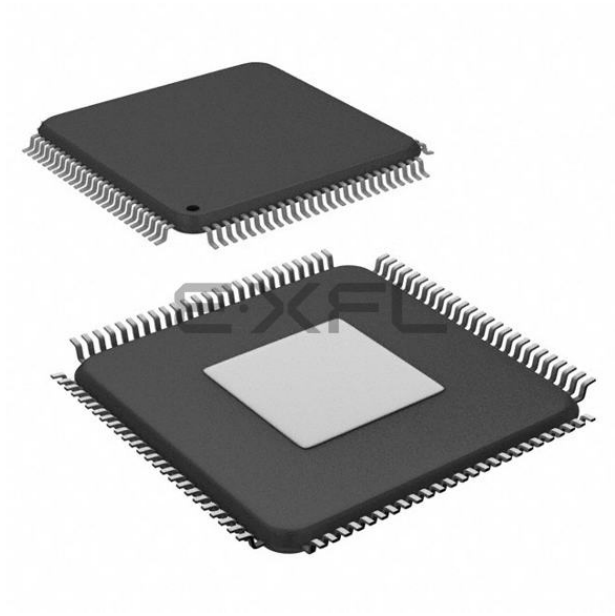
Infineon Technologies - XE164K48F66LACFXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164k48f66lacfxqma1

XE164

16-Bit Single-Chip Real Time Signal Controller

Microcontrollers

Never stop thinking

2 General Device Information

The XE164 series of real time signal controllers is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

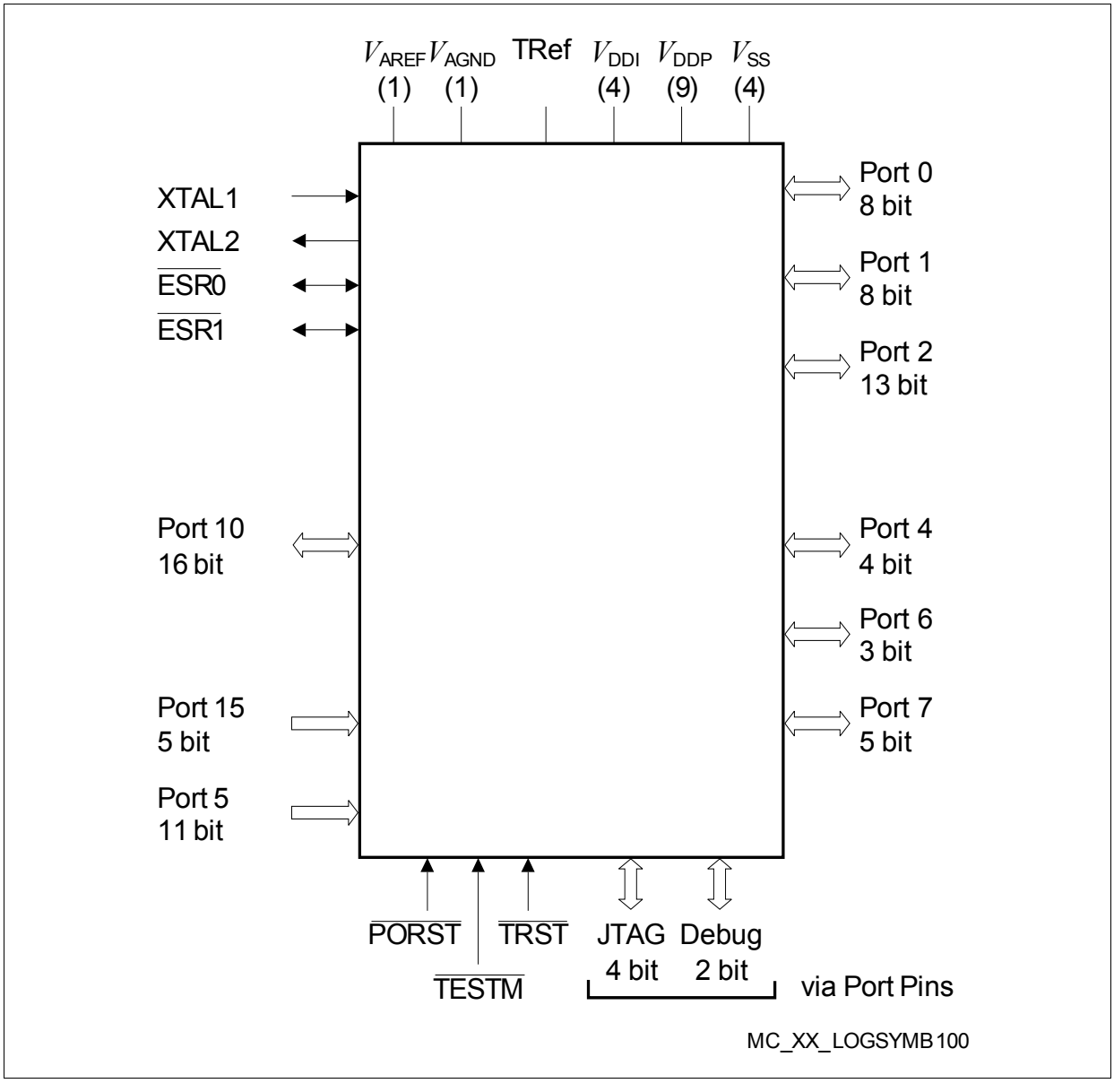

Figure 1 Logic Symbol

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
12	P6.1	O0 / I	St/A	**Bit 1 of Port 6, General Purpose Input/Output**
	EMUX1	O1	St/A	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	St/A	**GPT1 Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	St/A	**USIC1 Channel 1 Shift Data Output**
	ADCx_ REQTRyC	I	St/A	**External Request Trigger Input for ADC0/1**
13	P6.2	O0 / I	St/A	**Bit 2 of Port 6, General Purpose Input/Output**
	EMUX2	O1	St/A	**External Analog MUX Control Output 2 (ADC0)**
	T6OUT	O2	St/A	**GPT2 Timer T6 Toggle Latch Output**
	U1C1_ SCLKOUT	O3	St/A	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1C	I	St/A	**USIC1 Channel 1 Shift Clock Input**
15	P15.0	I	In/A	**Bit 0 of Port 15, General Purpose Input**
	ADC1_CH0	I	In/A	**Analog Input Channel 0 for ADC1**
16	P15.2	I	In/A	**Bit 2 of Port 15, General Purpose Input**
	ADC1_CH2	I	In/A	**Analog Input Channel 2 for ADC1**
	T5IN	I	In/A	**GPT2 Timer T5 Count/Gate Input**
17	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6IN	I	In/A	**GPT2 Timer T6 Count/Gate Input**
18	P15.5	I	In/A	**Bit 5 of Port 15, General Purpose Input**
	ADC1_CH5	I	In/A	**Analog Input Channel 5 for ADC1**
	T6EUD	I	In/A	**GPT2 Timer T6 External Up/Down Control Input**
19	P15.6	I	In/A	**Bit 6 of Port 15, General Purpose Input**
	ADC1_CH6	I	In/A	**Analog Input Channel 6 for ADC1**
20	V_{AREF}	-	PS/A	**Reference Voltage for A/D Converters ADC0/1**
21	V_{AGND}	-	PS/A	**Reference Ground for A/D Converters ADC0/1**
22	P5.0	I	In/A	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/A	**Analog Input Channel 0 for ADC0**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	P4.2	O0 / I	St/B	**Bit 2 of Port 4, General Purpose Input/Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_26	O3 / I	St/B	**CAPCOM2 CC26IO Capture Inp./ Compare Out.**
	$\overline{CS2}$	OH	St/B	**External Bus Interface Chip Select 2 Output**
	T2IN	I	St/B	**GPT1 Timer T2 Count/Gate Input**
48	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_ SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_ SELO1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	A19	OH	St/B	**External Bus Interface Address Line 19**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**
49	P4.3	O0 / I	St/B	**Bit 3 of Port 4, General Purpose Input/Output**
	CC2_27	O3 / I	St/B	**CAPCOM2 CC27IO Capture Inp./ Compare Out.**
	$\overline{CS3}$	OH	St/B	**External Bus Interface Chip Select 3 Output**
	RxDC2A	I	St/B	**CAN Node 2 Receive Data Input**
	T2EUD	I	St/B	**GPT1 Timer T2 External Up/Down Control Input**
53	P0.0	O0 / I	St/B	**Bit 0 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	CCU61_ CC60	O3 / I	St/B	**CCU61 Channel 0 Input/Output**
	A0	OH	St/B	**External Bus Interface Address Line 0**
	U1C0_DX0A	I	St/B	**USIC1 Channel 0 Shift Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_ MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_ SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	AD8	OH / I	St/B	**External Bus Interface Address/Data Line 8**
	CCU60_ CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
80	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_ SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_ MCLKOUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	AD9	OH / I	St/B	**External Bus Interface Address/Data Line 9**
	CCU60_ CCPOS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	I	St/B	**JTAG Clock Input**
81	P1.1	O0 / I	St/B	**Bit 1 of Port 1, General Purpose Input/Output**
	CCU62_ COUT62	O1	St/B	**CCU62 Channel 2 Output**
	U1C0_ SELO5	O2	St/B	**USIC1 Channel 0 Select/Control 5 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	A9	OH	St/B	**External Bus Interface Address Line 9**
	ESR2_3	I	St/B	**ESR2 Trigger Input 3**
	EX1BINA	I	St/B	**External Interrupt Trigger Input**
	U2C1_DX0C	I	St/B	**USIC2 Channel 1 Shift Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
98	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
	EX0AINB	I	St/B	**External Interrupt Trigger Input**
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** *Note: After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.*
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see **Table 12** for details.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see **Table 12** for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6, and P15 are fed from supply voltage V_{DDPA}.*

3.1 Memory Subsystem and Organization

The memory space of the XE164 is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 5 XE164 Memory Map

Address Area	Start Loc.	End Loc.	Area Size[1)]	Notes
IMB register space	FF'FF00$_H$	FF'FFFF$_H$	256 Bytes	–
Reserved (Access trap)	F0'0000$_H$	FF'FEFF$_H$	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E9'0000$_H$	EF'FFFF$_H$	448 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000$_H$	E8'FFFF$_H$	64 Kbytes	Flash timing
Reserved for PSRAM	E1'0000$_H$	E7'FFFF$_H$	448 Kbytes	Mirrors PSRAM
Program SRAM	E0'0000$_H$	E0'FFFF$_H$	64 Kbytes	Maximum speed
Reserved for pr. mem.	CC'0000$_H$	DF'FFFF$_H$	<1.25 Mbytes	–
Program Flash 2	C8'0000$_H$	CB'FFFF$_H$	256 Kbytes	–
Program Flash 1	C4'0000$_H$	C7'FFFF$_H$	256 Kbytes	–
Program Flash 0	C0'0000$_H$	C3'FFFF$_H$	256 Kbytes	2)
External memory area	40'0000$_H$	BF'FFFF$_H$	8 Mbytes	–
Available Ext. IO area[3)]	20'5800$_H$	3F'FFFF$_H$	< 2 Mbytes	Minus USIC/CAN
USIC registers	20'4000$_H$	20'57FF$_H$	6 Kbytes	Accessed via EBC
MultiCAN registers	20'0000$_H$	20'3FFF$_H$	16 Kbytes	Accessed via EBC
External memory area	01'0000$_H$	1F'FFFF$_H$	< 2 Mbytes	Minus segment 0
SFR area	00'FE00$_H$	00'FFFF$_H$	0.5 Kbyte	–
Dual-Port RAM	00'F600$_H$	00'FDFF$_H$	2 Kbytes	–
Reserved for DPRAM	00'F200$_H$	00'F5FF$_H$	1 Kbyte	–
ESFR area	00'F000$_H$	00'F1FF$_H$	0.5 Kbyte	–
XSFR area	00'E000$_H$	00'EFFF$_H$	4 Kbytes	–
Data SRAM	00'A000$_H$	00'DFFF$_H$	16 Kbytes	–
Reserved for DSRAM	00'8000$_H$	00'9FFF$_H$	8 Kbytes	–
External memory area	00'0000$_H$	00'7FFF$_H$	32 Kbytes	–

1) The areas marked with "<" are slightly smaller than indicated. See column "Notes".

2) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000$_H$ to C0'FFFF$_H$).

3) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 64 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

*Note: The actual size of the PSRAM depends on the chosen derivative (see **Table 1**).*

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data (12 Kbytes for devices with 192 Kbytes of Flash). The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1 Kbyte of on-chip Stand-By SRAM (SBRAM) provides storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 5**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Up to 768 Kbytes of on-chip Flash memory store code, constant data, and control data. The on-chip Flash memory consists of up to three modules with a maximum capacity of 256 Kbytes each. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

*Note: The actual size of the Flash memory depends on the chosen derivative (see **Table 1**).*

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.5**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.12 MultiCAN Module

The MultiCAN module contains up to four independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of 128 message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

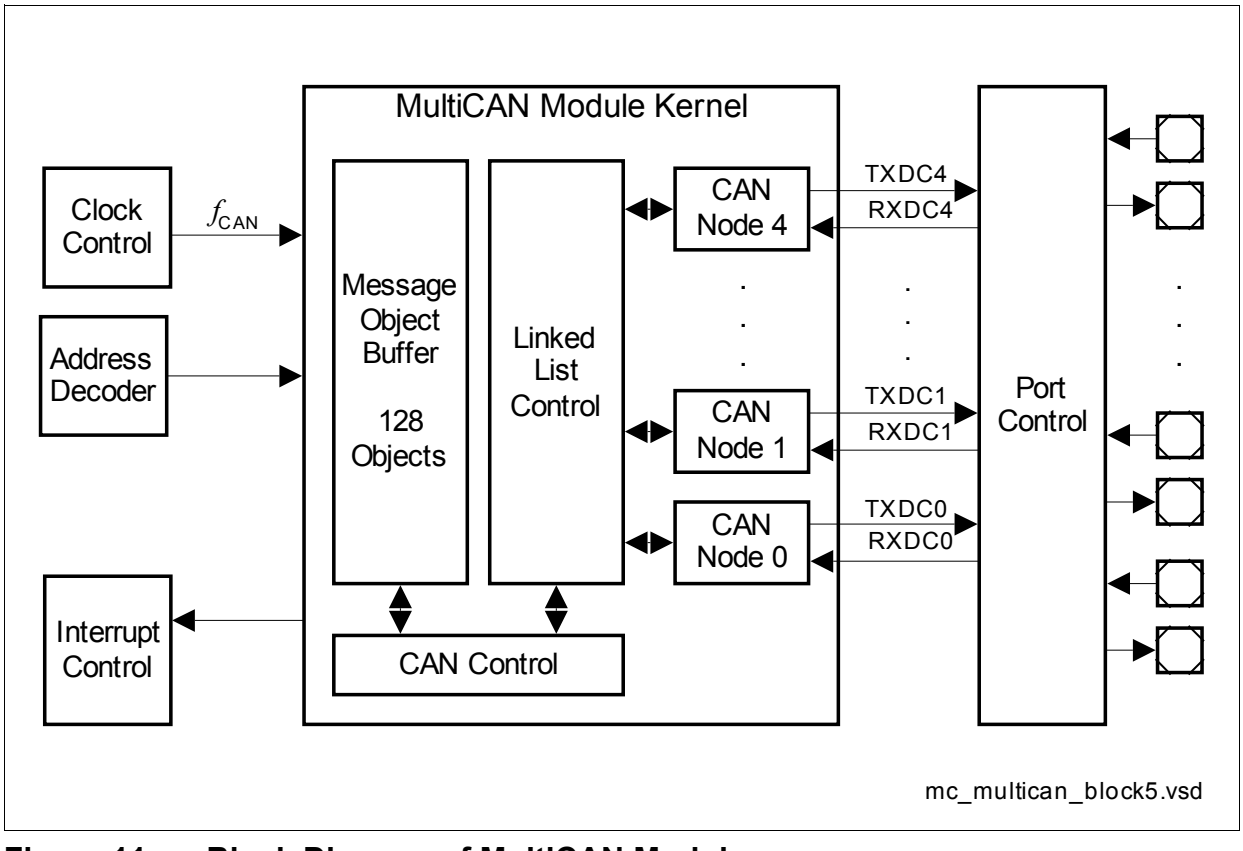

Figure 11 Block Diagram of MultiCAN Module

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to four independent CAN nodes
- 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 Parallel Ports

The XE164 provides up to 75 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 9**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 9 Summary of the XE164's Parallel Ports

Port	Width	Alternate Functions
Port 0	8	Address lines, Serial interface lines of USIC1, CAN0, and CAN1, Input/Output lines for CCU61
Port 1	8	Address lines, Serial interface lines of USIC1 and USIC2, Input/Output lines for CCU62, OCDS control, interrupts
Port 2	13	Address and/or data lines, bus control, Serial interface lines of USIC0, CAN0, and CAN1, Input/Output lines for CCU60 and CAPCOM2, Timer control signals, JTAG, interrupts, system clock output
Port 4	8	Chip select signals, Serial interface lines of CAN2, Input/Output lines for CAPCOM2, Timer control signals
Port 5	16	Analog input channels to ADC0, Input/Output lines for CCU6x, Timer control signals, JTAG, OCDS control, interrupts

Parameter Interpretation

The parameters listed in the following include both the characteristics of the XE164 and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XE164 provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XE164.

4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

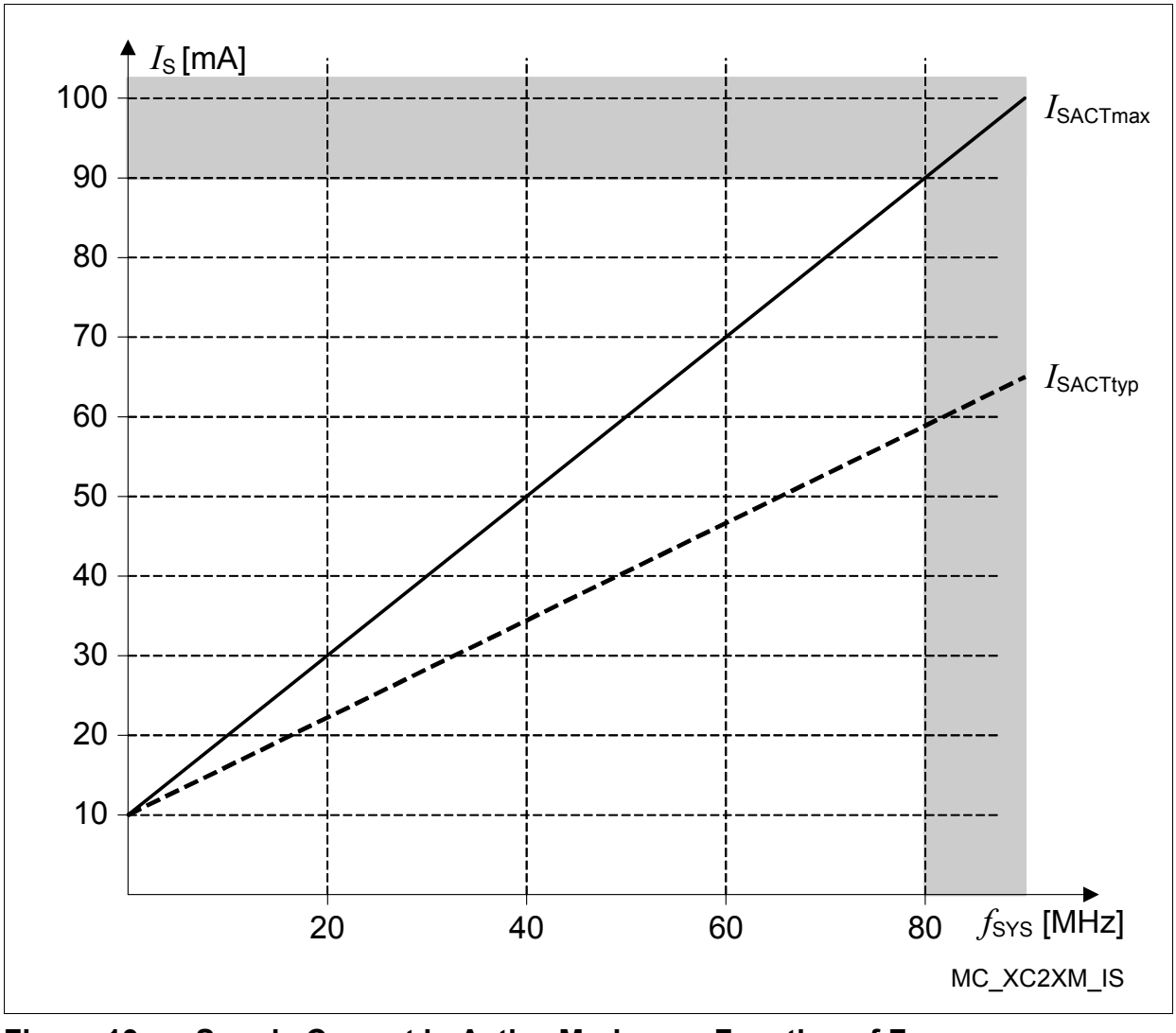

Figure 13 Supply Current in Active Mode as a Function of Frequency

Table 21 Coding of Bitfields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	2.9 V	
0001_B	3.0 V	LEV1V: reset request
0010_B	3.1 V	
0011_B	3.2 V	
0100_B	3.3 V	
0101_B	3.4 V	
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B	4.6 V	
1011_B	4.7 V	
1100_B	4.8 V	
1101_B	4.9 V	
1110_B	5.0 V	
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B	0.9 V	
001_B	1.0 V	
010_B	1.1 V	
011_B	1.2 V	
100_B	1.3 V	LEV1V: reset request
101_B	1.4 V	LEV2V: interrupt request
110_B	1.5 V	
111_B	1.6 V	

1) The indicated default levels are selected automatically after a power reset.

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$f_{SYS} = f_{IN}$.

The frequency of f_{SYS} is the same as the frequency of f_{IN}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN}.

Selecting Bypass Operation from the XTAL1[1)] input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$f_{SYS} = f_{OSC}$ / K1.

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$f_{SYS} = f_{OSC}$ / 1024.

Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times$ **F**).
F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):
(**F** = N / (P $\times$ K2)).

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN}. The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDI1}.

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 19**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

D_{Tmax} [ns] = $\pm(220 / (K2 \times f_{SYS}) + 4.3)$

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

D_T [ns] = $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

$D_{max} = \pm(220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

$D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$
$= 5.97 \times [0.768 \times 2 / 26.39 + 0.232]$
$= 1.7$ ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

$D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

$D_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 2]$
$= 7.63 \times [0.884 \times 2 / 26.39 + 0.116]$
$= 1.4$ ns

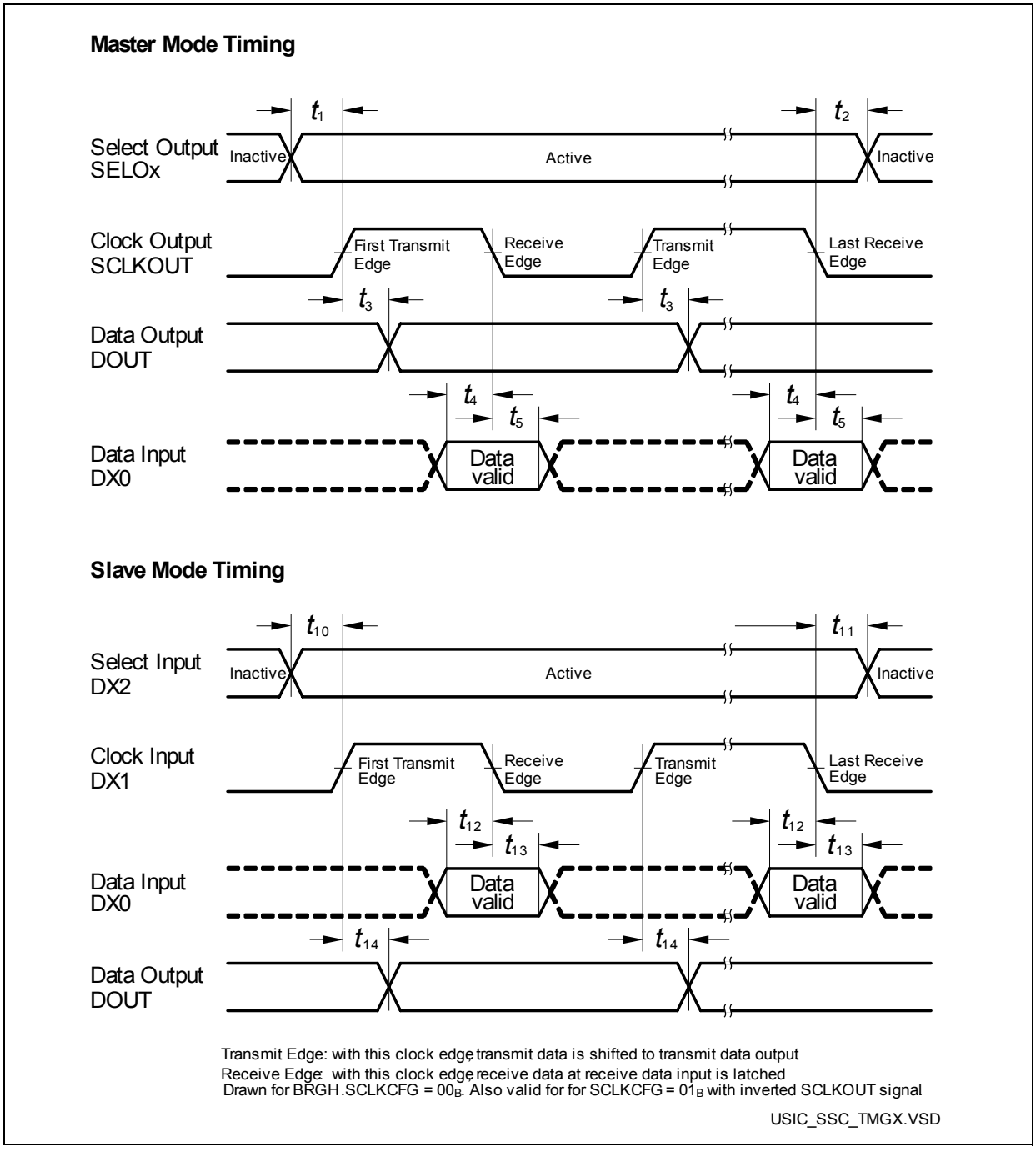

Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.