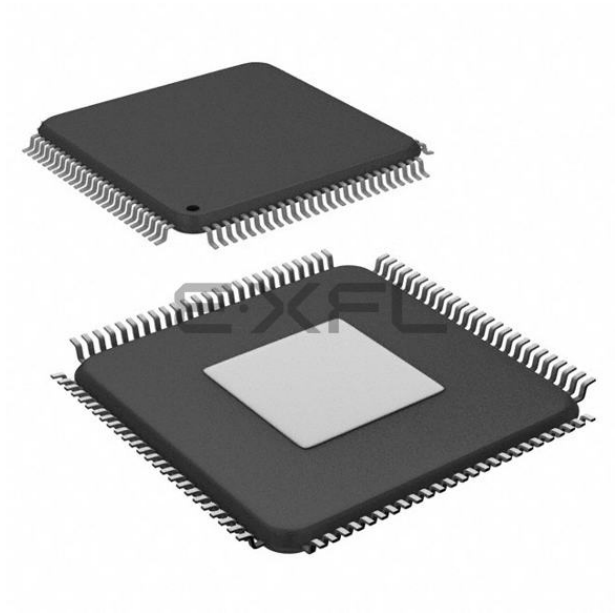
Infineon Technologies - XE164K96F66LACFXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164k96f66lacfxuma1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
23	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**
24	P5.3	I	In/A	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/A	**Analog Input Channel 3 for ADC0**
	T3IN	I	In/A	**GPT1 Timer T3 Count/Gate Input**
28	P5.4	I	In/A	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/A	**Analog Input Channel 4 for ADC0**
	T3EUD	I	In/A	**GPT1 Timer T3 External Up/Down Control Input**
	TMS_A	I	In/A	**JTAG Test Mode Selection Input**
29	P5.5	I	In/A	**Bit 5 of Port 5, General Purpose Input**
	ADC0_CH5	I	In/A	**Analog Input Channel 5 for ADC0**
	CCU60_ T12HRB	I	In/A	**External Run Control Input for T12 of CCU60**
30	P5.8	I	In/A	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/A	**Analog Input Channel 8 for ADC0**
	CCU6x_ T12HRC	I	In/A	**External Run Control Input for T12 of CCU6x**
	CCU6x_ T13HRC	I	In/A	**External Run Control Input for T13 of CCU6x**
31	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
32	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	$\overline{\text{BRKIN\_A}}$	I	In/A	**OCDS Break Signal Input**
33	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
34	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
	EX0BINB	I	In/A	**External Interrupt Trigger Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
58	P0.2	O0 / I	St/B	**Bit 2 of Port 0, General Purpose Input/Output**
	U1C0_ SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_ CC62	O3 / I	St/B	**CCU61 Channel 2 Input/Output**
	A2	OH	St/B	**External Bus Interface Address Line 2**
	U1C0_DX1B	I	St/B	**USIC1 Channel 0 Shift Clock Input**
59	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_ CC60	O2 / I	St/B	**CCU60 Channel 0 Input/Output**
	AD0	OH / I	St/B	**External Bus Interface Address/Data Line 0**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
60	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_ CC61	O2 / I	St/B	**CCU60 Channel 1 Input/Output**
	AD1	OH / I	St/B	**External Bus Interface Address/Data Line 1**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
61	P0.3	O0 / I	St/B	**Bit 3 of Port 0, General Purpose Input/Output**
	U1C0_ SELO0	O1	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U1C1_ SELO1	O2	St/B	**USIC1 Channel 1 Select/Control 1 Output**
	CCU61_ COUT60	O3	St/B	**CCU61 Channel 0 Output**
	A3	OH	St/B	**External Bus Interface Address Line 3**
	U1C0_DX2A	I	St/B	**USIC1 Channel 0 Shift Control Input**
	RxDC0B	I	St/B	**CAN Node 0 Receive Data Input**
62	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_ SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_ CC62	O2 / I	St/B	**CCU60 Channel 2 Input/Output**
	AD2	OH / I	St/B	**External Bus Interface Address/Data Line 2**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
63	P0.4	O0 / I	St/B	**Bit 4 of Port 0, General Purpose Input/Output**
	U1C1_ SELO0	O1	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C0_ SELO1	O2	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	CCU61_ COUT61	O3	St/B	**CCU61 Channel 1 Output**
	A4	OH	St/B	**External Bus Interface Address Line 4**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**
65	TRef	IO	Sp/1	**Control Pin for Core Voltage Generation** 2)

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
85	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	TDO_B	O3	St/B	**JTAG Test Data Output**
	AD12	OH / I	St/B	**External Bus Interface Address/Data Line 12**
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**
86	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC3	O2	St/B	**CAN Node 3 Transmit Data Output**
	U1C0_ SELO3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{WR}$/$\overline{WRL}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{WR}$, active for ext. writes to the low byte, when $\overline{WRL}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
87	P1.3	O0 / I	St/B	**Bit 3 of Port 1, General Purpose Input/Output**
	CCU62_ COUT63	O1	St/B	**CCU62 Channel 3 Output**
	U1C0_ SELO7	O2	St/B	**USIC1 Channel 0 Select/Control 7 Output**
	U2C0_ SELO4	O3	St/B	**USIC2 Channel 0 Select/Control 4 Output**
	A11	OH	St/B	**External Bus Interface Address Line 11**
	ESR2_4	I	St/B	**ESR2 Trigger Input 4**
	CCU62_ T12HRB	I	St/B	**External Run Control Input for T12 of CCU62**
	EX3AINA	I	St/B	**External Interrupt Trigger Input**

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to four external $\overline{CS}$ signals (three windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

With this hardware most XE164 instructions can be executed in a single machine cycle of 12.5 ns with an 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XE164 instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Table 6 XE164 Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 16, or ERU Request 0	CC2_CC16IC	xx'0040$_H$	10$_H$ / 16$_D$
CAPCOM Register 17, or ERU Request 1	CC2_CC17IC	xx'0044$_H$	11$_H$ / 17$_D$
CAPCOM Register 18, or ERU Request 2	CC2_CC18IC	xx'0048$_H$	12$_H$ / 18$_D$
CAPCOM Register 19, or ERU Request 3	CC2_CC19IC	xx'004C$_H$	13$_H$ / 19$_D$
CAPCOM Register 20, or USIC0 Request 6	CC2_CC20IC	xx'0050$_H$	14$_H$ / 20$_D$
CAPCOM Register 21, or USIC0 Request 7	CC2_CC21IC	xx'0054$_H$	15$_H$ / 21$_D$
CAPCOM Register 22, or USIC1 Request 6	CC2_CC22IC	xx'0058$_H$	16$_H$ / 22$_D$
CAPCOM Register 23, or USIC1 Request 7	CC2_CC23IC	xx'005C$_H$	17$_H$ / 23$_D$
CAPCOM Register 24, or ERU Request 0	CC2_CC24IC	xx'0060$_H$	18$_H$ / 24$_D$
CAPCOM Register 25, or ERU Request 1	CC2_CC25IC	xx'0064$_H$	19$_H$ / 25$_D$
CAPCOM Register 26, or ERU Request 2	CC2_CC26IC	xx'0068$_H$	1A$_H$ / 26$_D$
CAPCOM Register 27, or ERU Request 3	CC2_CC27IC	xx'006C$_H$	1B$_H$ / 27$_D$
CAPCOM Register 28, or USIC2 Request 6	CC2_CC28IC	xx'0070$_H$	1C$_H$ / 28$_D$
CAPCOM Register 29, or USIC2 Request 7	CC2_CC29IC	xx'0074$_H$	1D$_H$ / 29$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0078$_H$	1E$_H$ / 30$_D$
CAPCOM Register 31	CC2_CC31IC	xx'007C$_H$	1F$_H$ / 31$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0080$_H$	20$_H$ / 32$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'0084$_H$	21$_H$ / 33$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0088$_H$	22$_H$ / 34$_D$

Table 6 XE164 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
USIC2 Cannel 1, Request 0	U2C1_0IC	xx'017C$_H$	5F$_H$ / 95$_D$
USIC2 Cannel 1, Request 1	U2C1_1IC	xx'0180$_H$	60$_H$ / 96$_D$
USIC2 Cannel 1, Request 2	U2C1_2IC	xx'0184$_H$	61$_H$ / 97$_D$
Unassigned node	–	xx'0188$_H$	62$_H$ / 98$_D$
Unassigned node	–	xx'018C$_H$	63$_H$ / 99$_D$
Unassigned node	–	xx'0190$_H$	64$_H$ / 100$_D$
Unassigned node	–	xx'0194$_H$	65$_H$ / 101$_D$
Unassigned node	–	xx'0198$_H$	66$_H$ / 102$_D$
Unassigned node	–	xx'019C$_H$	67$_H$ / 103$_D$
Unassigned node	–	xx'01A0$_H$	68$_H$ / 104$_D$
Unassigned node	–	xx'01A4$_H$	69$_H$ / 105$_D$
Unassigned node	–	xx'01A8$_H$	6A$_H$ / 106$_D$
SCU Request 1	SCU_1IC	xx'01AC$_H$	6B$_H$ / 107$_D$
SCU Request 0	SCU_0IC	xx'01B0$_H$	6C$_H$ / 108$_D$
Program Flash Modules	PFM_IC	xx'01B4$_H$	6D$_H$ / 109$_D$
RTC	RTC_IC	xx'01B8$_H$	6E$_H$ / 110$_D$
End of PEC Subchannel	EOPIC	xx'01BC$_H$	6F$_H$ / 111$_D$

1) Register VECSEG defines the segment where the vector table is located.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting with a distance of 4 (two words) between two vectors.

3.6 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to a number of prescaled values of the internal system clock. It may also be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range for the timer period and resolution while allowing precise adjustments for application-specific requirements. An external count input for CAPCOM2 timer T7 allows event scheduling for the capture/compare registers with respect to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers. Each may be individually allocated to either CAPCOM2 timer T7 or T8 and programmed for a capture or compare function.
12 registers of the CAPCOM2 module have one port pin associated with it. This serves as an input pin to trigger the capture function or as an output pin to indicate the occurrence of a compare event.

Table 8 Compare Modes (CAPCOM2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

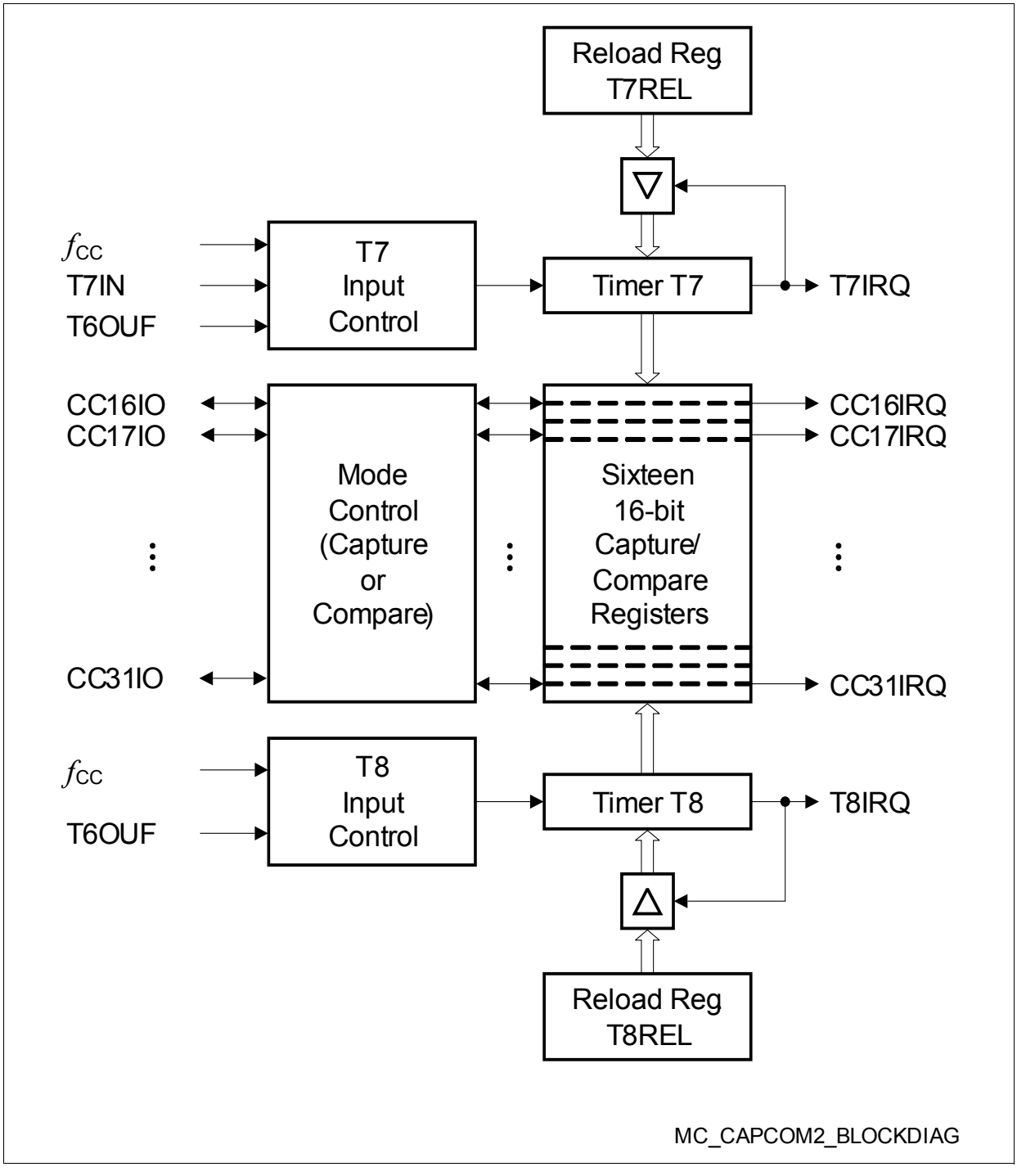

Figure 5 CAPCOM2 Unit Block Diagram

3.10 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 11 + 5 multiplexed input channels and a sample and hold circuit have been integrated on-chip. They use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically.

For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XE164 support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features, such as limit checking or result accumulation, reduce the number of required CPU access operations allowing the precise evaluation of analoginputs (high conversion rate) even at a low CPU speed.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately with registers P5_DIDIS and P15_DIDIS (Port x Digital Input Disable).

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - maximum baud rate: f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - maximum baud rate: f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
  - maximum baud rate in slave mode: f_{SYS}
  - maximum baud rate in master mode: f_{SYS} / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - maximum baud rate: f_{SYS} / 2 for transmitter, f_{SYS} for receiver

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

Table 9 Summary of the XE164's Parallel Ports (cont'd)

Port	Width	Alternate Functions
Port 6	4	ADC control lines, Serial interface lines of USIC1, Timer control signals, OCDS control
Port 7	5	ADC control lines, Serial interface lines of USIC0, Input/Output lines for CCU62, Timer control signals, JTAG, OCDS control,system clock output
Port 10	16	Address and/or data lines, bus control, Serial interface lines of USIC0, USIC1, CAN2 and CAN3, Input/Output lines for CCU60, JTAG, OCDS control
Port 15	8	Analog input channels to ADC1, Timer control signals

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction[1)]	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

Parameter Interpretation

The parameters listed in the following include both the characteristics of the XE164 and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XE164 provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XE164.

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE164 can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE164 are designed to operate in various driver modes. The DC parameter specifications refer to the current limits in **Table 13**.

Table 13 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]		Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)	
	$V_{DDP} \geq$ 4.5 V	$V_{DDP} <$ 4.5 V	$V_{DDP} \geq$ 4.5 V	$V_{DDP} <$ 4.5 V
Strong driver	10 mA	10 mA	2.5 mA	2.5 mA
Medium driver	4.0 mA	2.5 mA	1.0 mA	1.0 mA
Weak driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Pullup/Pulldown Device Behavior

Most pins of the XE164 feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 12** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

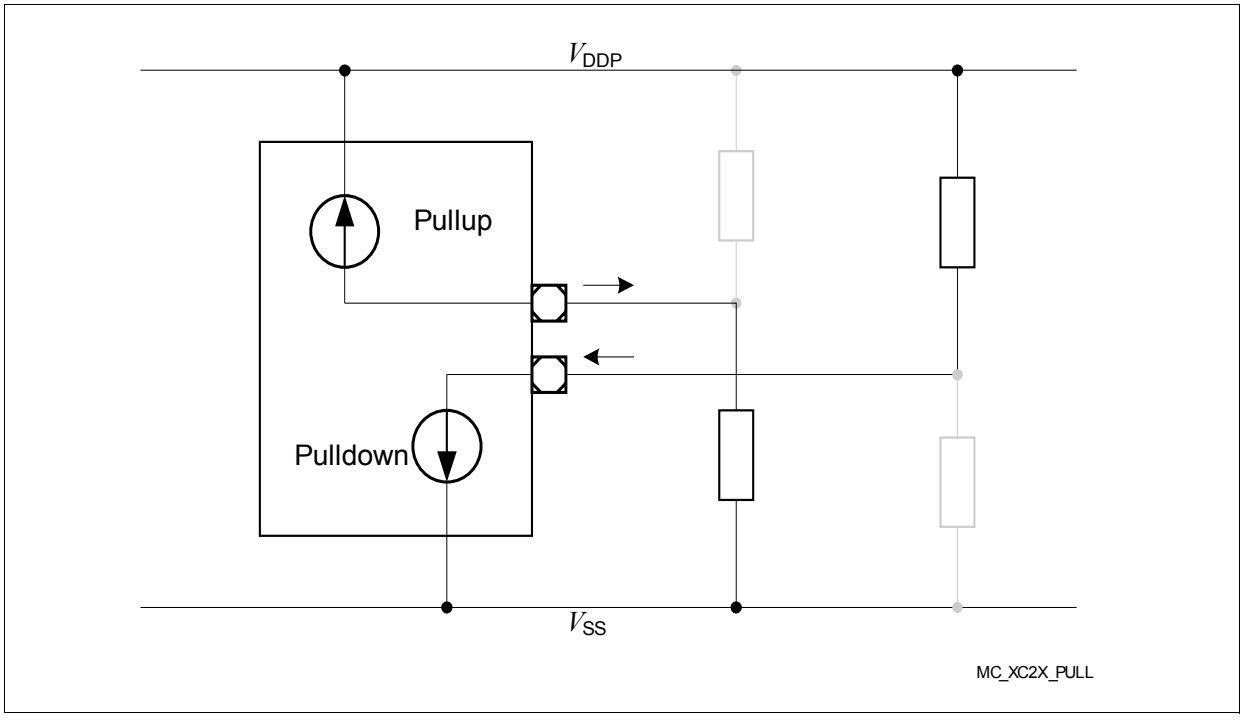

Figure 12 Pullup/Pulldown Current Definition

4.3 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Table 18 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	V_{AGND} + 1.0	V_{DDPA} + 0.05	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.05	V_{AREF} - 1.0	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Analog clock frequency	f_{ADCI}		0.5	20	MHz	3)
Conversion time for 10-bit result[4)]	t_{C10}	CC	(13 + STC) × t_{ADCI} + 2 × t_{SYS}		–	–
Conversion time for 8-bit result[4)]	t_{C8}	CC	(11 + STC) × t_{ADCI} + 2 × t_{SYS}		–	–
Wakeup time from analog powerdown, fast mode	t_{WAF}	CC	–	1	µs	–
Wakeup time from analog powerdown, slow mode	t_{WAS}	CC	–	10	µs	–
Total unadjusted error[5)]	TUE	CC	–	±2	LSB	V_{AREF} = 5.0 V[1)]
DNL error	EA_{DNL}	CC	–	±1	LSB	
INL error	EA_{INL}	CC	–	±1.2	LSB	
Gain error	EA_{GAIN}	CC	–	±0.8	LSB	
Offset error	EA_{OFF}	CC	–	±0.8	LSB	
Total capacitance of an analog input	C_{AINT}	CC	–	10	pF	6)7)
Switched capacitance of an analog input	C_{AINS}	CC	–	4	pF	6)7)
Resistance of the analog input path	R_{AIN}	CC	–	1.5	kΩ	6)7)
Total capacitance of the reference input	C_{AREFT}	CC	–	15	pF	6)7)

4.6.4 External Bus Timing

The following parameters specify the behavior of the XE164 bus interface.

Table 27 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit	Note / Test Condition
			Min.	Max.		
CLKOUT cycle time	t_5	CC	40/25/12.5[1)]		ns	
CLKOUT high time	t_6	CC	3	–	ns	
CLKOUT low time	t_7	CC	3	–	ns	
CLKOUT rise time	t_8	CC	–	3	ns	
CLKOUT fall time	t_9	CC	–	3	ns	

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{SYS} = 25/40/80 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

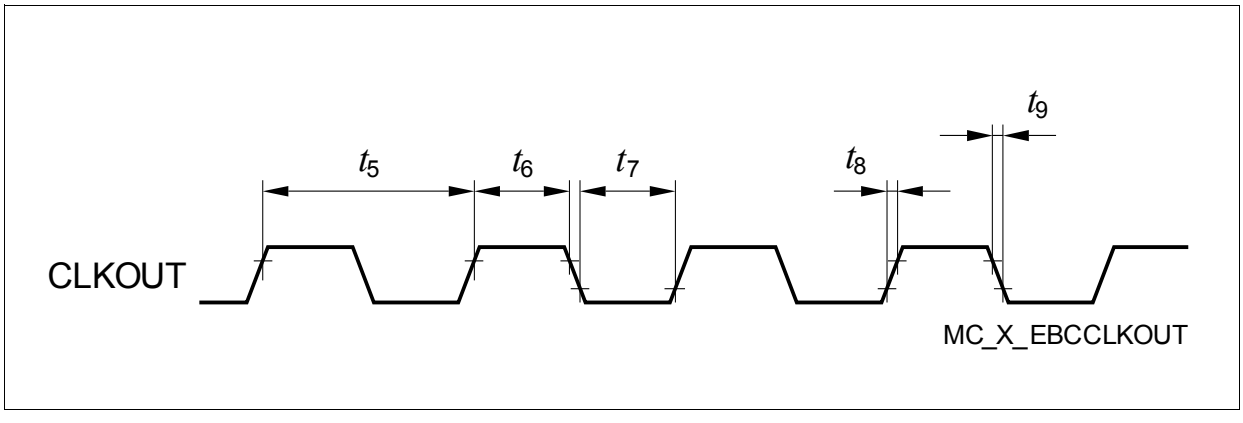

Figure 21 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

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