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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lah2016g



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Development Features

Table 1 lists the features of ZiLOG®'s Z8 GP™ OTP MCU Family family members.

Table 1. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323L OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–3.6V

- Low power consumption—6mW (typical)
- T = Temperature
S = Standard 0° to +70°C
E = Extended -40° to +105°C
A = Automotive -40° to +125°C
- Three standby modes:
 - STOP—2μA (typical)
 - HALT—0.8mA (typical)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors

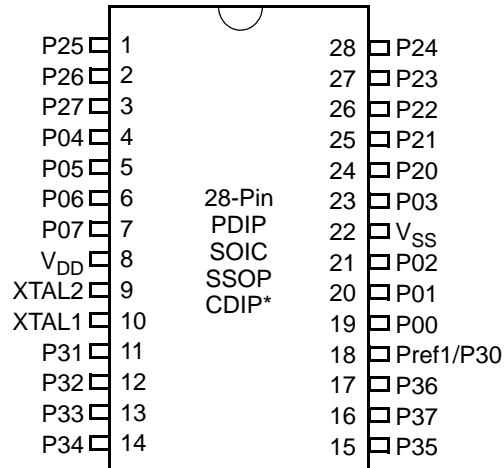


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V _{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Table 10. AC Characteristics

T _A =0°C to +70°C 8.0MHz							Watch-Dog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1
3	TwC	Input Clock Width	2.0–3.6	37		ns	1
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2
10	Twsm	Stop-Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms	

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

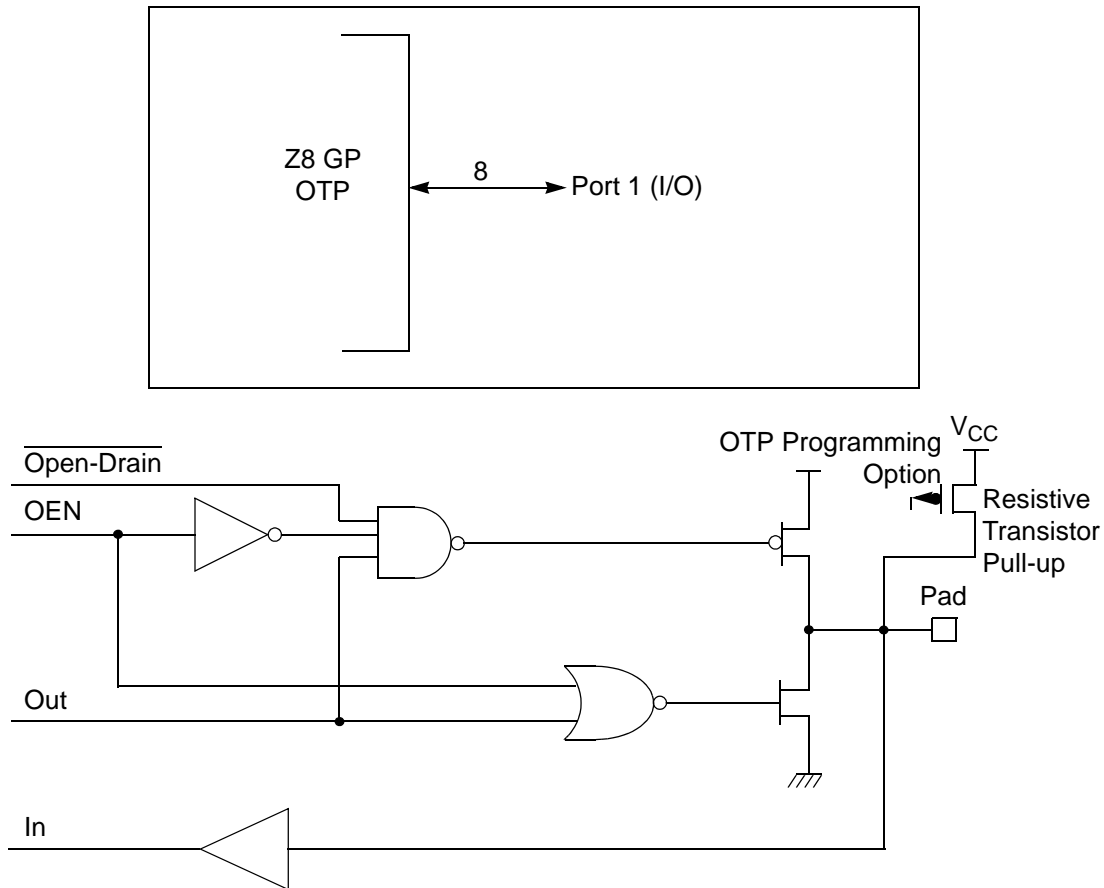


Figure 10. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

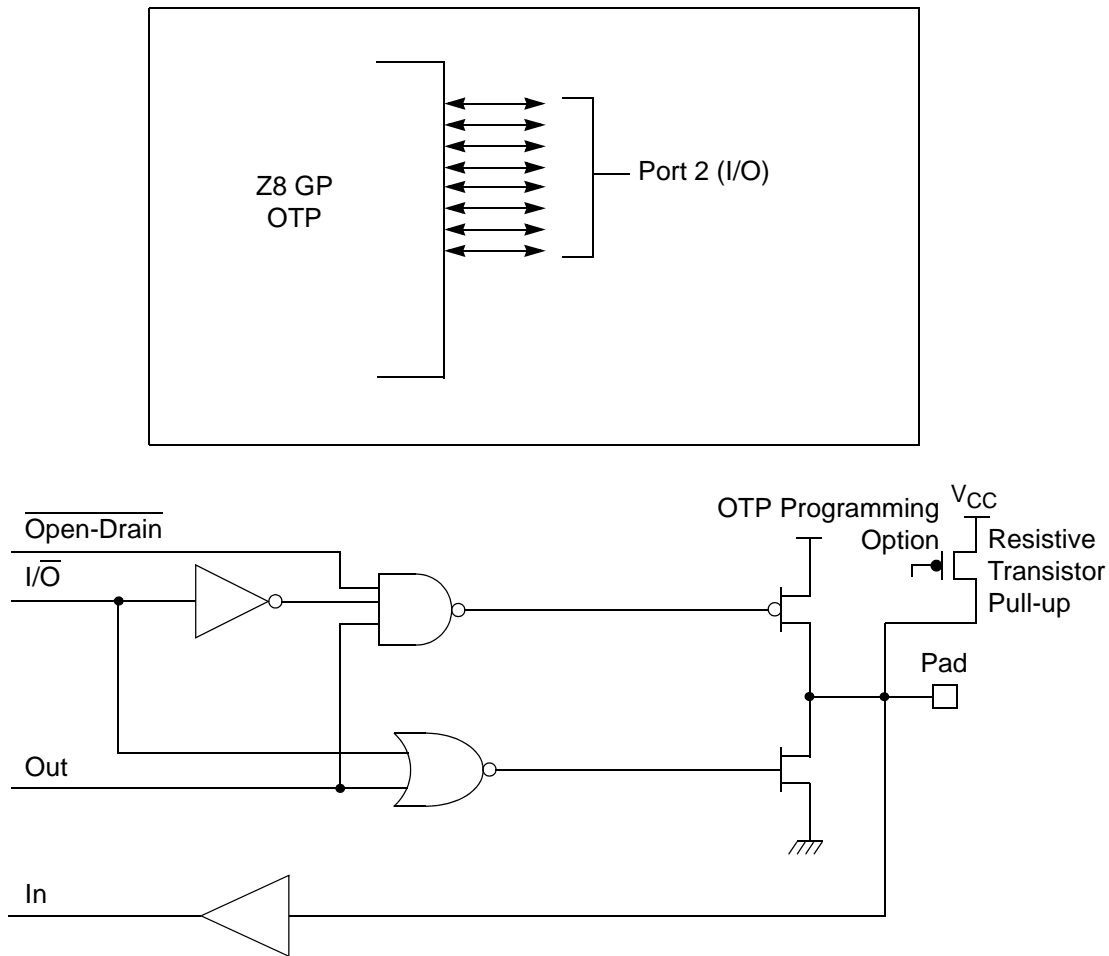


Figure 11. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

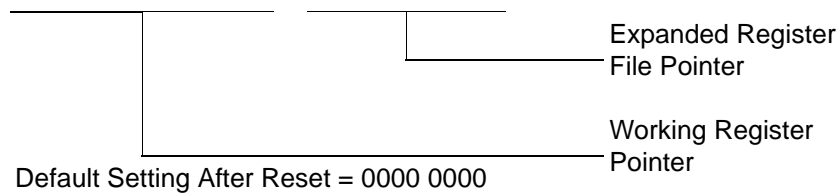


Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 26)

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTRL0

R1 = CTRL1

R2 = CTRL2

R3 = Reserved

Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_LO	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

Table 12. CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	-----1-	R/W	0	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-----0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:

*Indicates the value upon Power-On Reset.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.



Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

This bit defines the frequency of the input signal to T8.

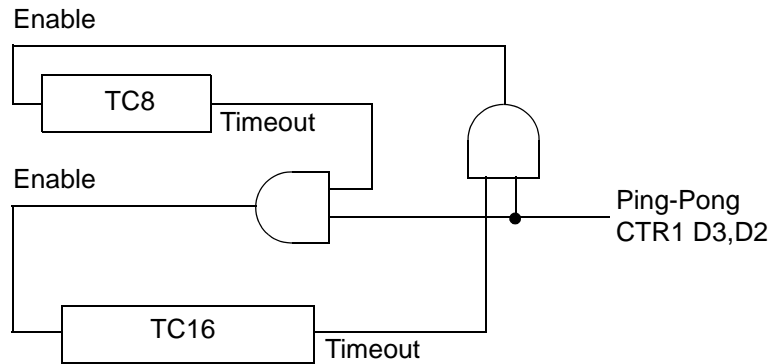


Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

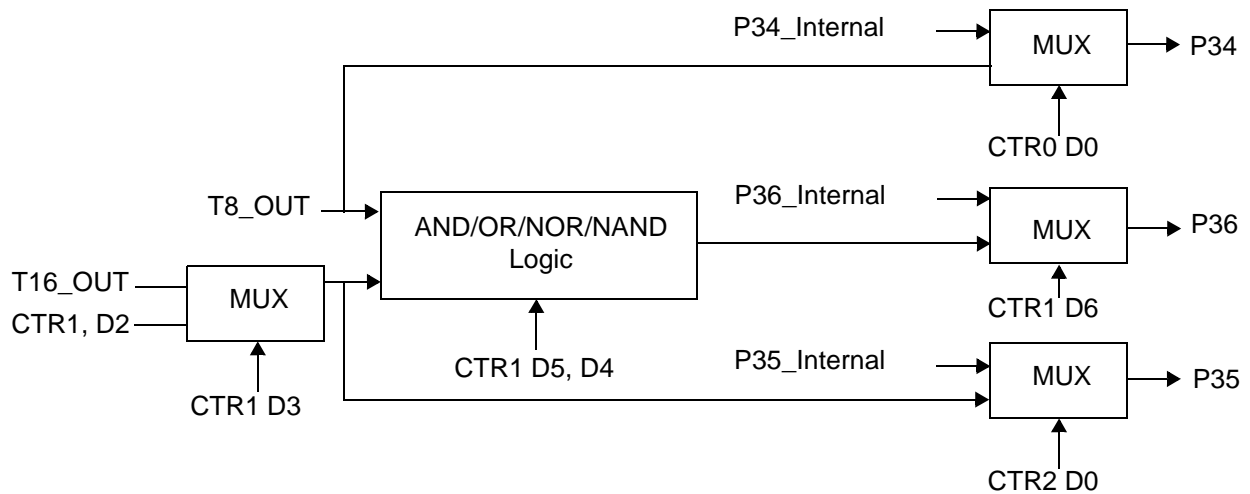


Figure 29. Output Circuit

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

```
FF      NOP      ; clear the pipeline
6F      Stop     ; enter Stop Mode
```

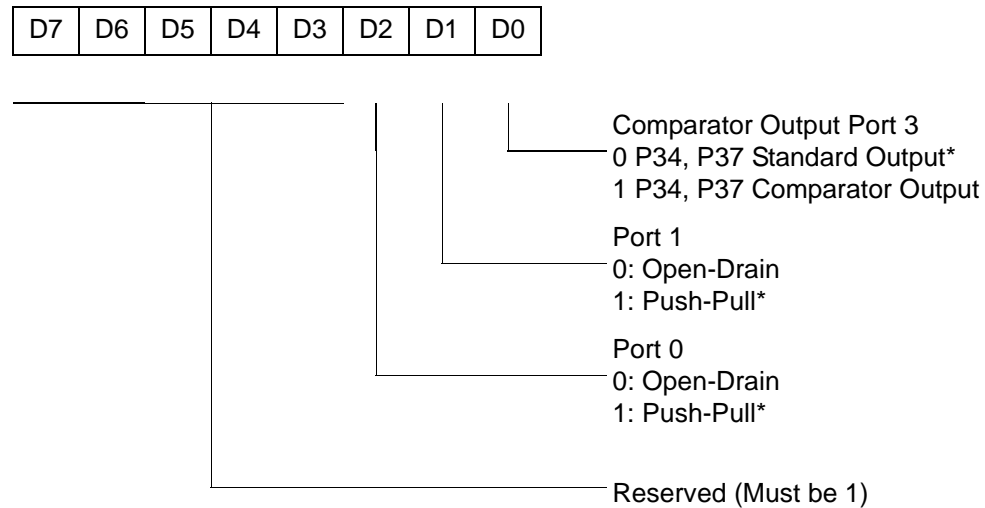
or

```
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H



* Default setting after reset

Figure 32. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 57) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

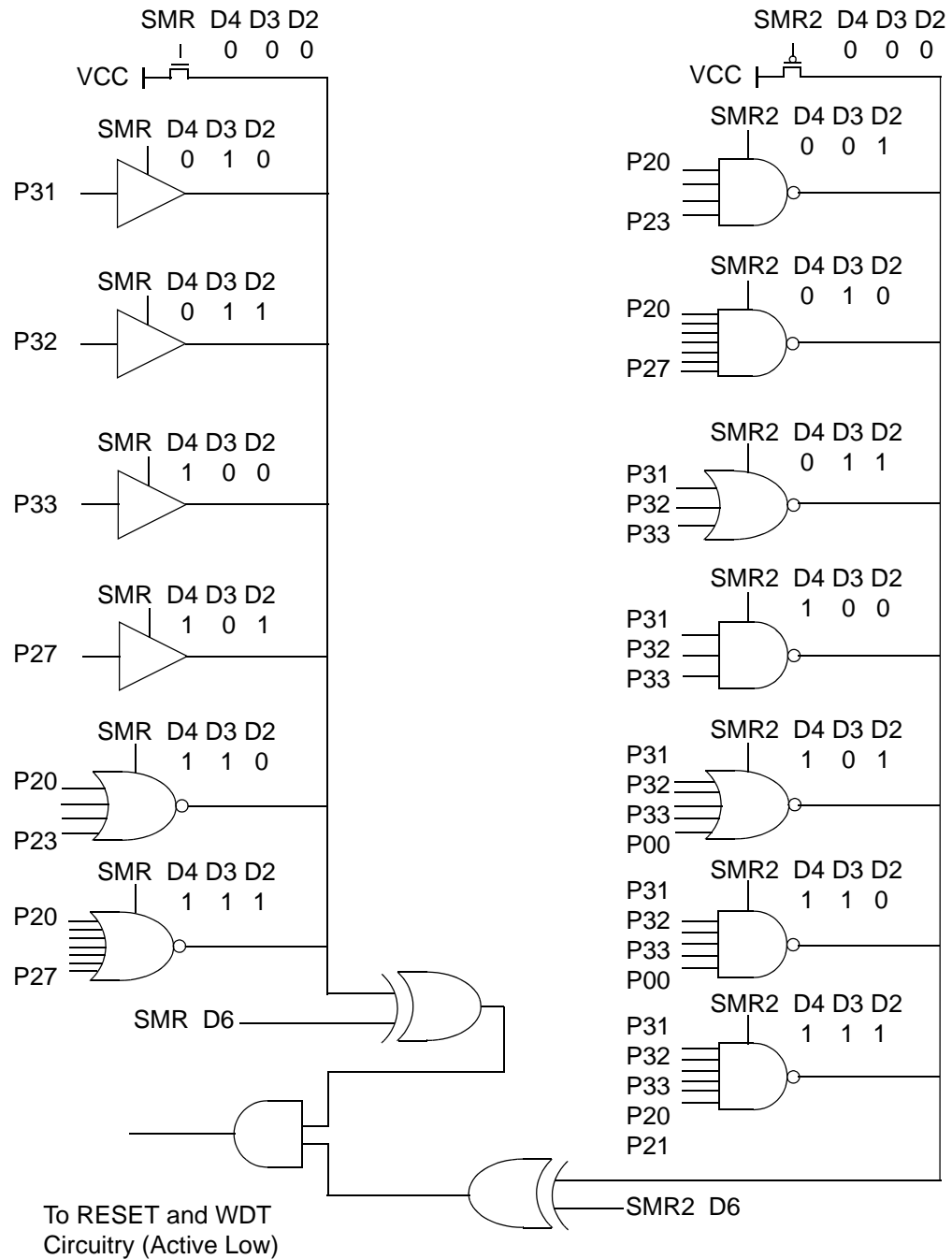
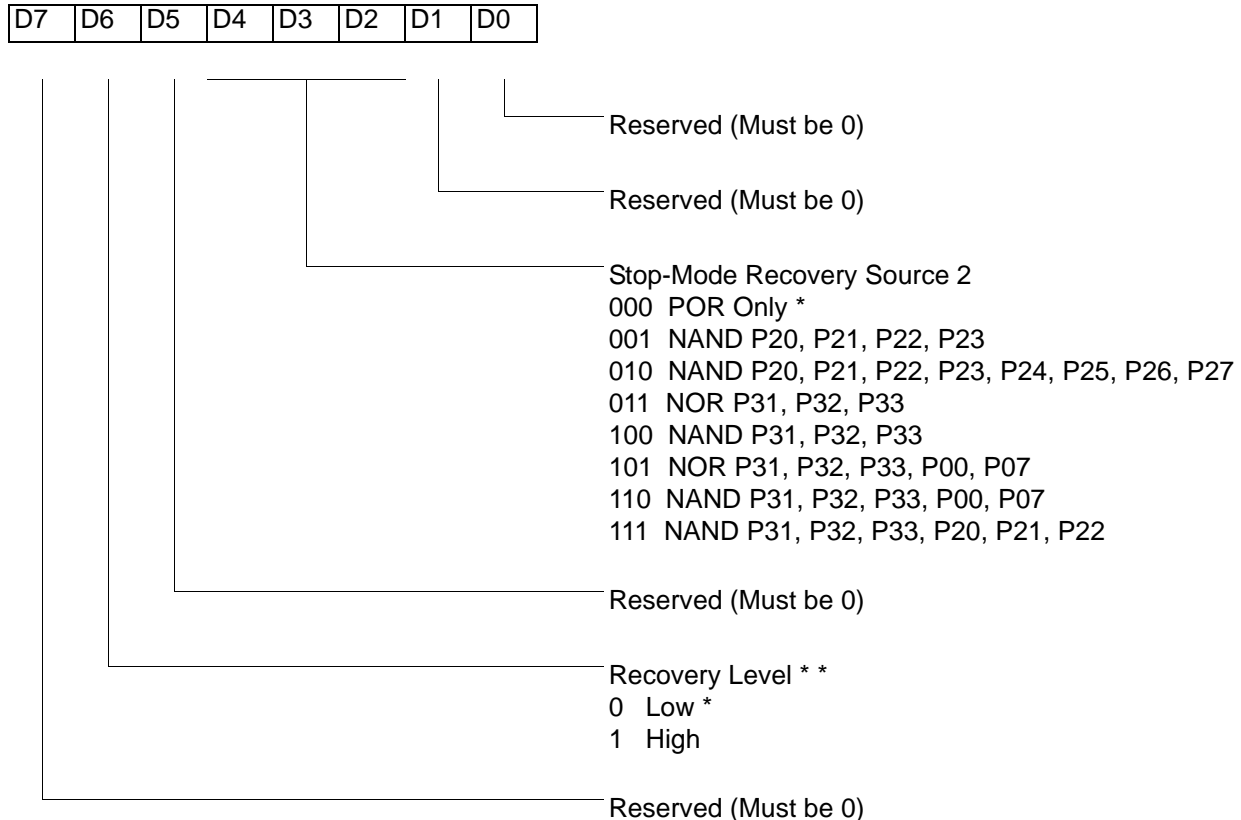


Figure 35. Stop Mode Recovery Source

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

** At the XOR gate input

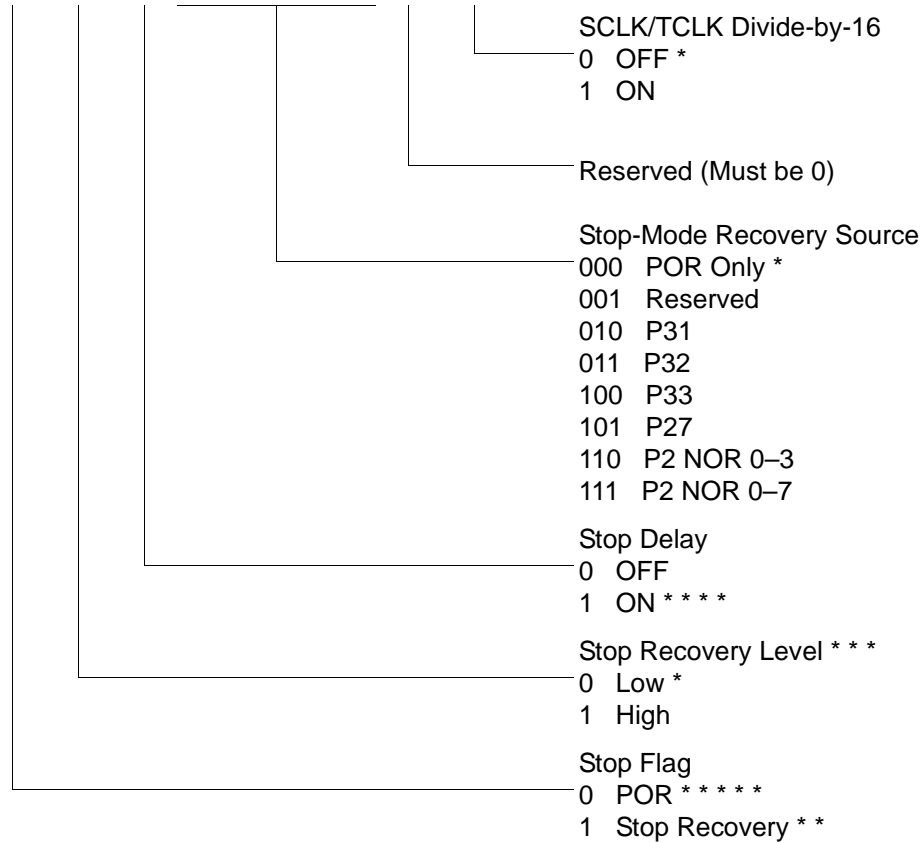
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

► **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after Reset

* * Set after STOP Mode Recovery

* * * At the XOR gate input

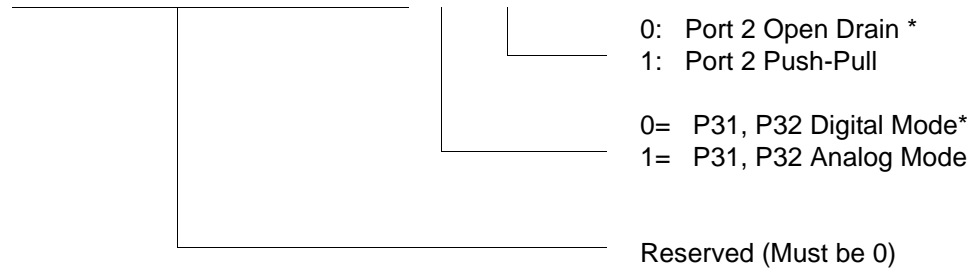
* * * * Default setting after Reset. Must be 1 if using a crystal or resonator clock source.

* * * * * Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

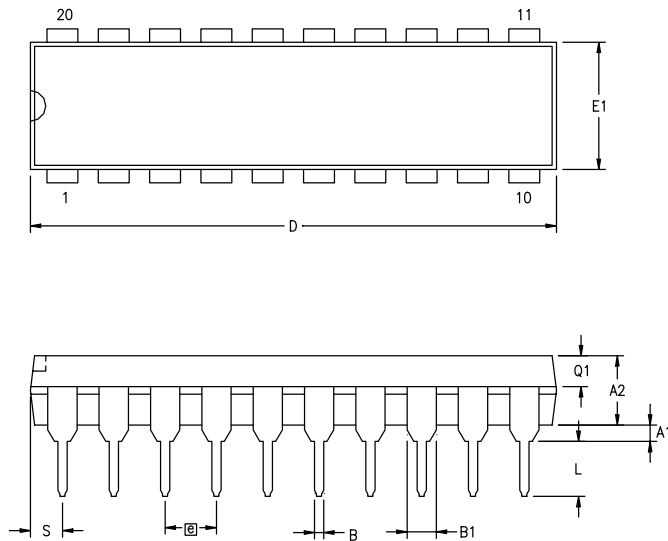
R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset. Not reset with Stop Mode recovery.

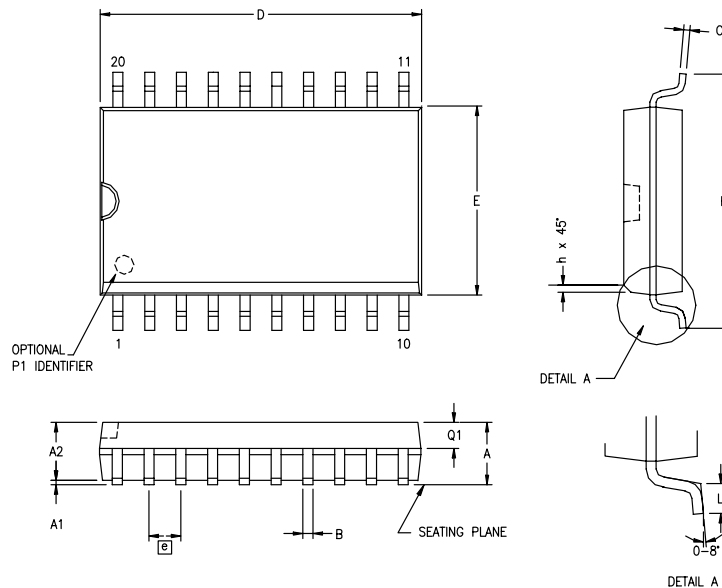
Figure 49. Port 3 Mode Register (F7H: Write Only)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
Ⓢ	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

Figure 59. 20-Pin PDIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
Ⓢ	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 60. 20-Pin SOIC Package Diagram



8KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4808C	48-pin SSOP 8K OTP	ZGP323LSS2808C	28-pin SOIC 8K OTP
ZGP323LSP4008C	40-pin PDIP 8K OTP	ZGP323LSH2008C	20-pin SSOP 8K OTP
ZGP323LSH2808C	28-pin SSOP 8K OTP	ZGP323LSP2008C	20-pin PDIP 8K OTP
ZGP323LSP2808C	28-pin PDIP 8K OTP	ZGP323LSS2008C	20-pin SOIC 8K OTP

8KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4808C	48-pin SSOP 8K OTP	ZGP323LES2808C	28-pin SOIC 8K OTP
ZGP323LEP4008C	40-pin PDIP 8K OTP	ZGP323LEH2008C	20-pin SSOP 8K OTP
ZGP323LEH2808C	28-pin SSOP 8K OTP	ZGP323LEP2008C	20-pin PDIP 8K OTP
ZGP323LEP2808C	28-pin PDIP 8K OTP	ZGP323LES2008C	20-pin SOIC 8K OTP

8KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4808C	48-pin SSOP 8K OTP	ZGP323LAS2808C	28-pin SOIC 8K OTP
ZGP323LAP4008C	40-pin PDIP 8K OTP	ZGP323LAH2008C	20-pin SSOP 8K OTP
ZGP323LAH2808C	28-pin SSOP 8K OTP	ZGP323LAP2008C	20-pin PDIP 8K OTP
ZGP323LAP2808C	28-pin PDIP 8K OTP	ZGP323LAS2008C	20-pin SOIC 8K OTP

Note: Replace C with G for Lead-Free Packaging



Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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