# Zilog - ZGP323LAH2032C00TR Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 16 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323lah2032c00tr |

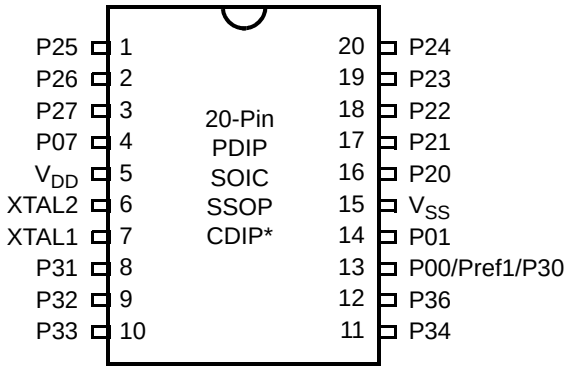



**Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration**

**Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1–3 | P25–P27 | Port 2, Bits 5,6,7 | Input/Output |
| 4 | P07 | Port 0, Bit 7 | Input/Output |
| 5 | $V_{DD}$ | Power Supply | |
| 6 | XTAL2 | Crystal Oscillator Clock | Output |
| 7 | XTAL1 | Crystal Oscillator Clock | Input |
| 8–10 | P31–P33 | Port 3, Bits 1,2,3 | Input |
| 11,12 | P34. P36 | Port 3, Bits 4,6 | Output |
| 13 | P00/Pref1/P30 | Port 0, Bit 0/Analog reference input<br>Port 3 Bit 0 | Input/Output for P00<br>Input for Pref1/P30 |
| 14 | P01 | Port 0, Bit 1 | Input/Output |
| 15 | $V_{SS}$ | Ground | |
| 16–20 | P20–P24 | Port 2, Bits 0,1,2,3,4 | Input/Output |

**Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

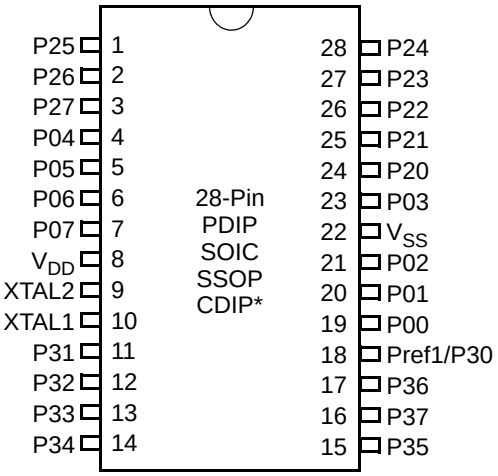



**Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration**

**Table 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification**

| Pin | Symbol | Direction | Description |
|---|---|---|---|
| 1-3 | P25-P27 | Input/Output | Port 2, Bits 5,6,7 |
| 4-7 | P04-P07 | Input/Output | Port 0, Bits 4,5,6,7 |
| 8 | $V_{DD}$ | | Power supply |
| 9 | XTAL2 | Output | Crystal, oscillator clock |
| 10 | XTAL1 | Input | Crystal, oscillator clock |
| 11-13 | P31-P33 | Input | Port 3, Bits 1,2,3 |
| 14 | P34 | Output | Port 3, Bit 4 |
| 15 | P35 | Output | Port 3, Bit 5 |
| 16 | P37 | Output | Port 3, Bit 7 |
| 17 | P36 | Output | Port 3, Bit 6 |
| 18 | Pref1/P30<br>Port 3 Bit 0 | Input | Analog ref input; connect to $V_{CC}$ if not used<br>Input for Pref1/P30 |
| 19-21 | P00-P02 | Input/Output | Port 0, Bits 0,1,2 |
| 22 | $V_{SS}$ | | Ground |
| 23 | P03 | Input/Output | Port 0, Bit 3 |
| 24-28 | P20-P24 | Input/Output | Port 2, Bits 0-4 |

**Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

**Table 5. 40- and 48-Pin Configuration (Continued)**

| 40-Pin PDIP/CDIP* # | 48-Pin SSOP # | Symbol |
|---|---|---|
| 33 | 40 | P13 |
| 8 | 9 | P14 |
| 9 | 10 | P15 |
| 12 | 15 | P16 |
| 13 | 16 | P17 |
| 35 | 42 | P20 |
| 36 | 43 | P21 |
| 37 | 44 | P22 |
| 38 | 45 | P23 |
| 39 | 46 | P24 |
| 2 | 2 | P25 |
| 3 | 3 | P26 |
| 4 | 4 | P27 |
| 16 | 19 | P31 |
| 17 | 20 | P32 |
| 18 | 21 | P33 |
| 19 | 22 | P34 |
| 22 | 26 | P35 |
| 24 | 28 | P36 |
| 23 | 27 | P37 |
| 20 | 23 | NC |
| 40 | 47 | NC |
| 1 | 1 | NC |
| 21 | 25 | $\overline{\text{RESET}}$ |
| 15 | 18 | XTAL1 |
| 14 | 17 | XTAL2 |
| 11 | 12, 13 | $V_{DD}$ |
| 31 | 24, 37, 38 | $V_{SS}$ |
| 25 | 29 | Pref1/P30 |
|  | 48 | NC |

# AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.

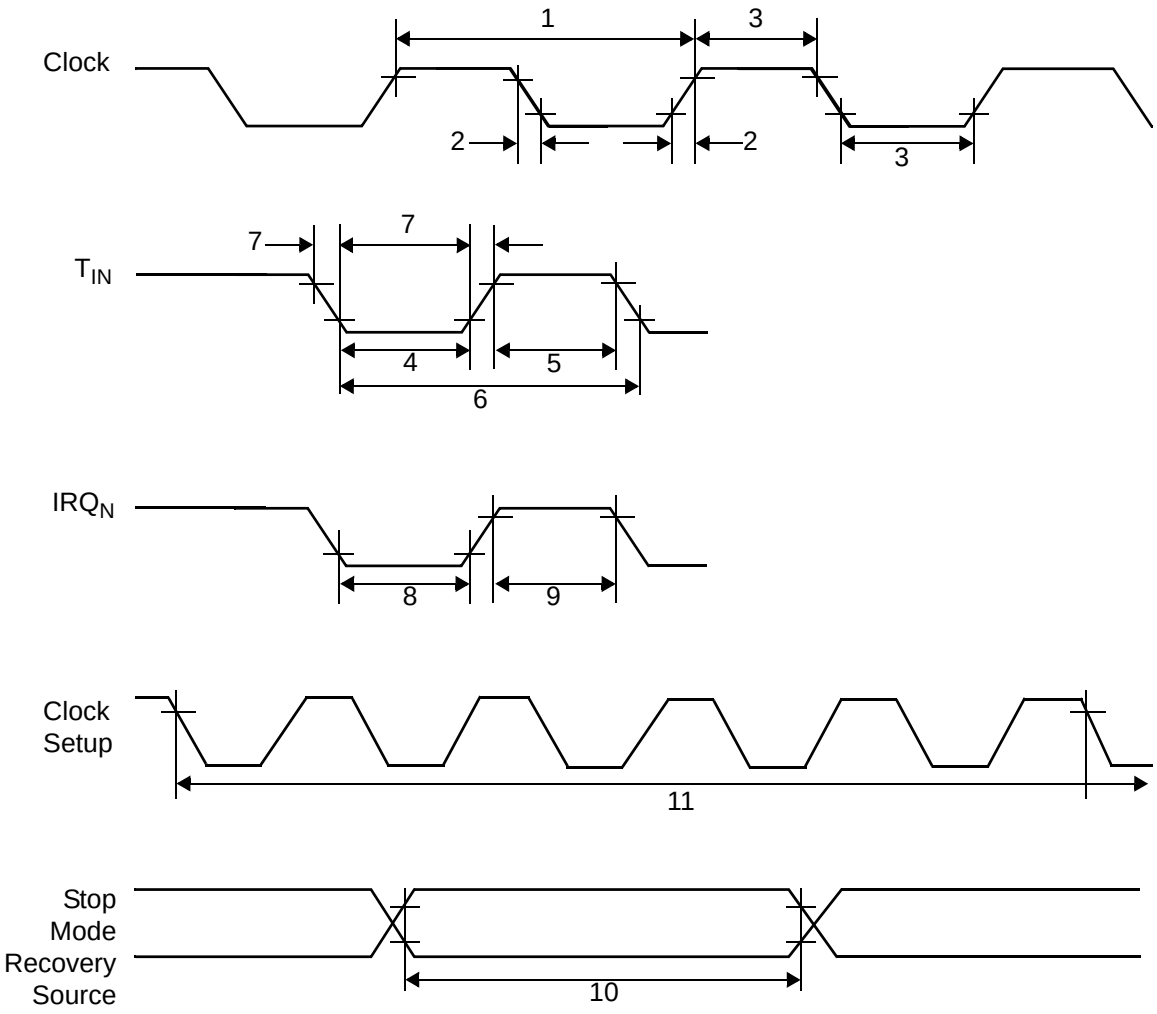



**Figure 8. AC Timing Diagram**

### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## $\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP™ asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP™ does not assert the $\overline{\text{RESET}}$ pin when under VBO.

**Note:** The external Reset does not initiate an exit from STOP mode.

# Functional Description

This device incorporates special functions to enhance the Z8®, functionality in consumer and battery-operated applications.

## Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

## RAM

This device features 256B of RAM. See Figure 14.

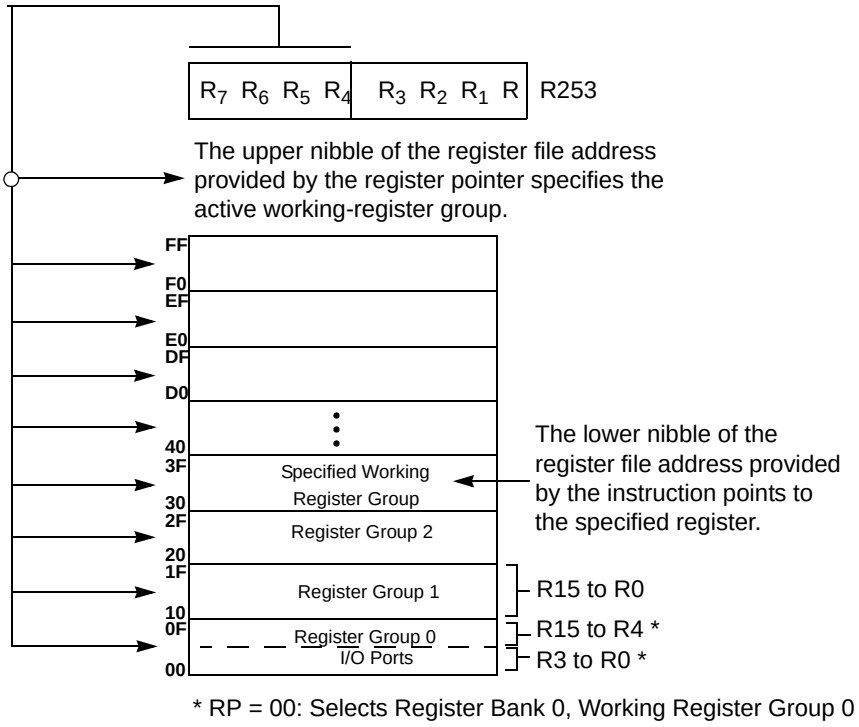



**Figure 17. Register Pointer—Detail**

## Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

### T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

### Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

### Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

### Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

**Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

### CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 14 lists and briefly describes the fields for this register.

**Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Reserved | ---43210 | R<br>W | 1<br>x | Always reads 11111<br>No Effect |

Note: *Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

## Counter/Timer Functional Blocks

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

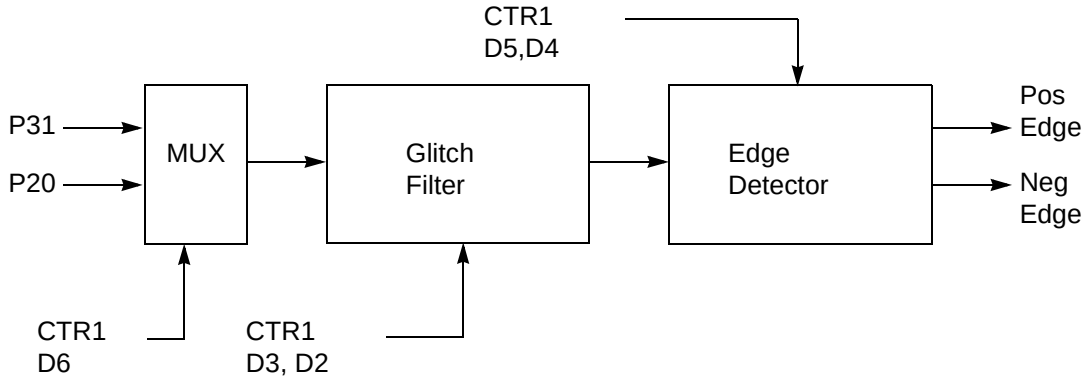



**Figure 18. Glitch Filter Circuitry**

### T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.

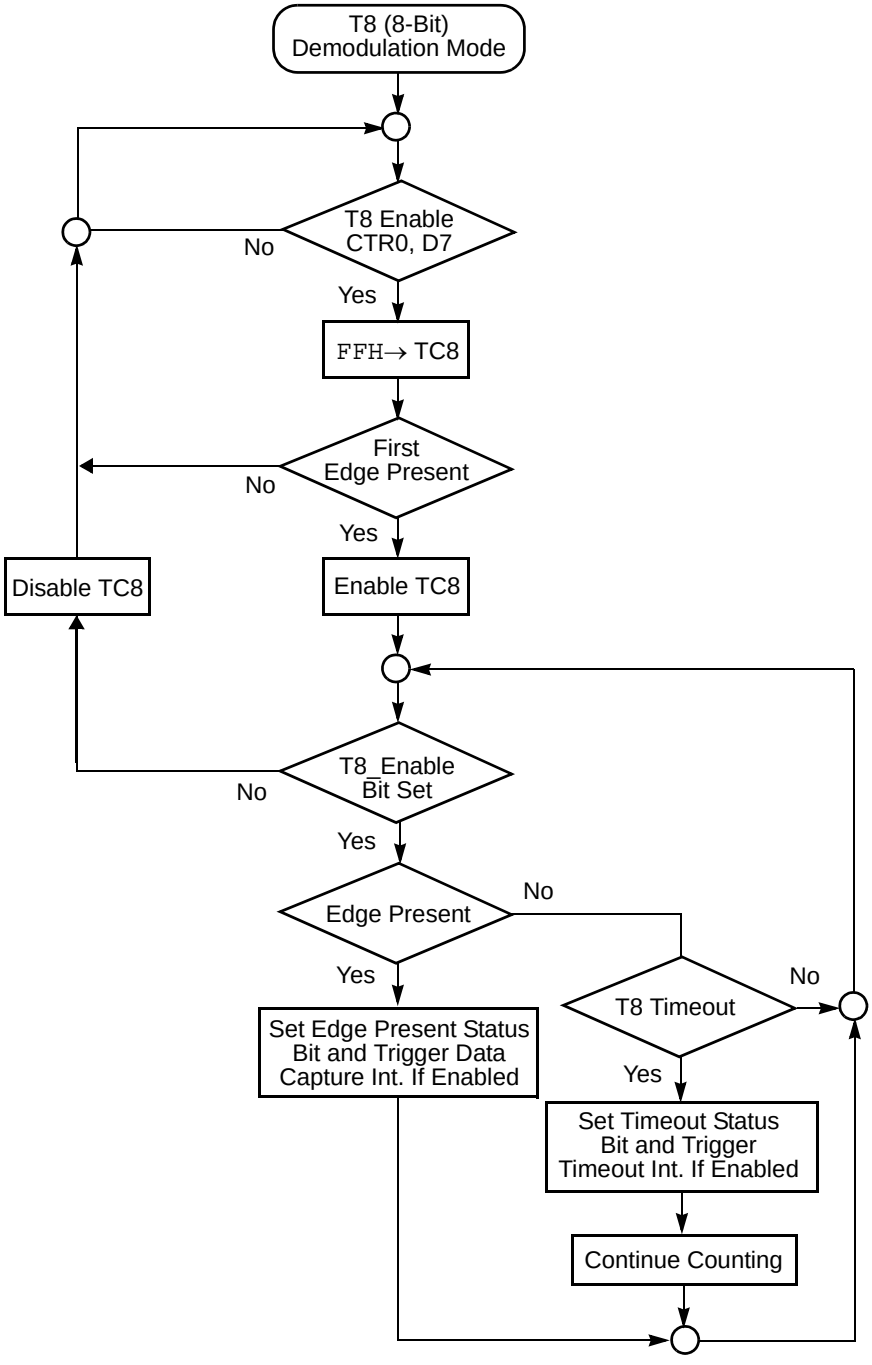



**Figure 24. Demodulation Mode Flowchart**

**Table 16. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | P32 | 0,1 | External (P32), Rising, Falling Edge Triggered |
| IRQ1 | P33 | 2,3 | External (P33), Falling Edge Triggered |
| IRQ2 | P31, $T_{IN}$ | 4,5 | External (P31), Rising, Falling Edge Triggered |
| IRQ3 | T16 | 6,7 | Internal |
| IRQ4 | T8 | 8,9 | Internal |
| IRQ5 | LVD | 10,11 | Internal |

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z8 GP™ OTP MCU Family interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 17.

**Table 17. IRQ Register**

| IRQ | | Interrupt Edge | |
|---|---|---|---|
| **D7** | **D6** | **IRQ2 (P31)** | **IRQ0 (P32)** |
| 0 | 0 | F | F |
| 0 | 1 | F | R |
| 1 | 0 | R | F |
| 1 | 1 | R/F | R/F |

**Note:** F = Falling Edge; R = Rising Edge

### Low-Voltage Detection Register—LVD(D)0Ch

**Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

| Field | Bit Position | | | Description |
|---|---|---|---|---|
| LVD | 76543--- | | | Reserved<br>No Effect |
| | -----2-- | R | 1<br>0* | HVD flag set<br>HVD flag reset |
| | ------1- | R | 1<br>0* | LVD flag set<br>LVD flag reset |
| | -------0 | R/W | 1<br>0* | Enable VD<br>Disable VD |

***Default after POR

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the $V_{CC}$ voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the $V_{CC}$ level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if $V_{CC}$ is higher than $V_{HVD.}$ The LVD flag (bit 1 of the LVD register) is set only if $V_{CC}$ is lower than the $V_{LVD}$. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

**Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

CTR2(0D)02H

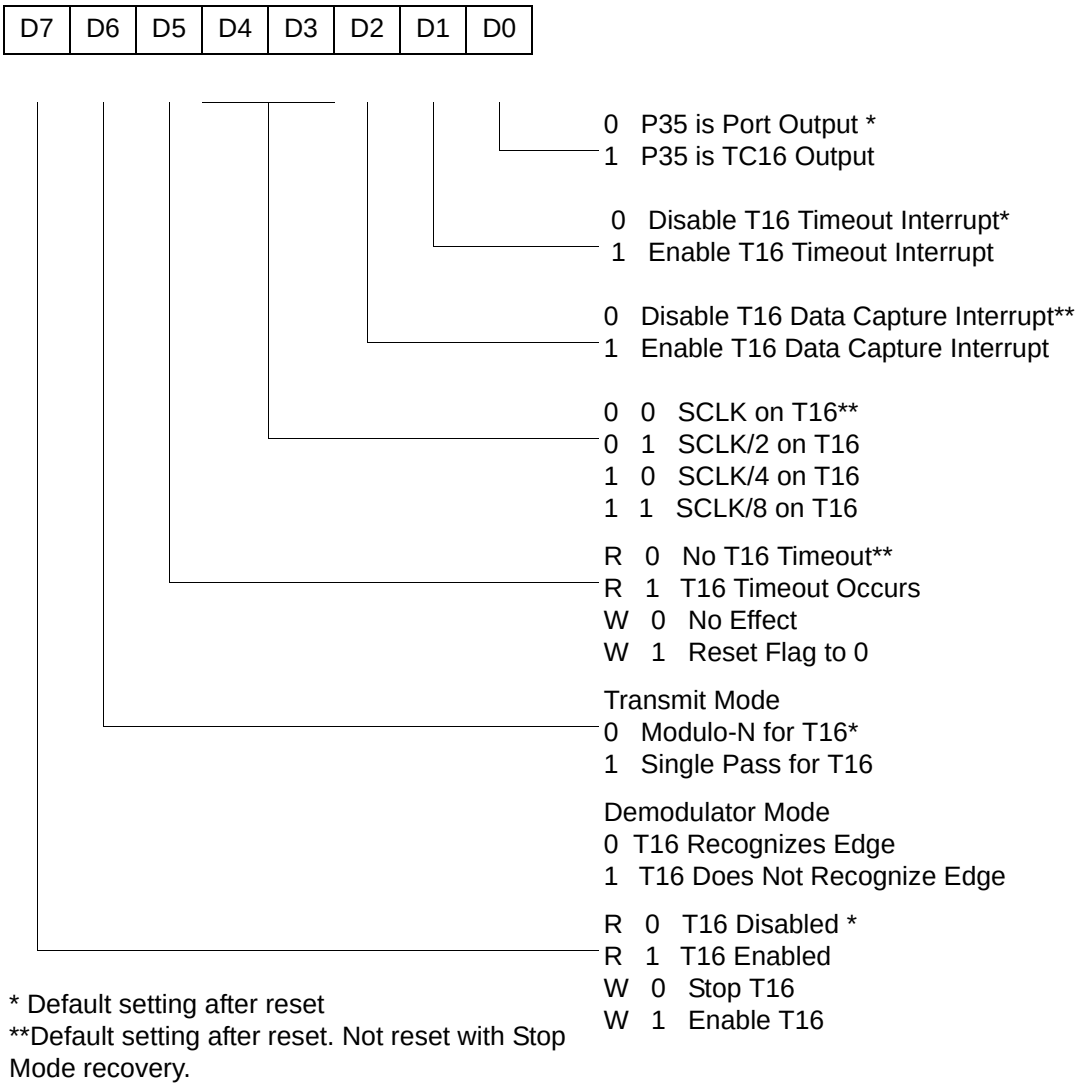
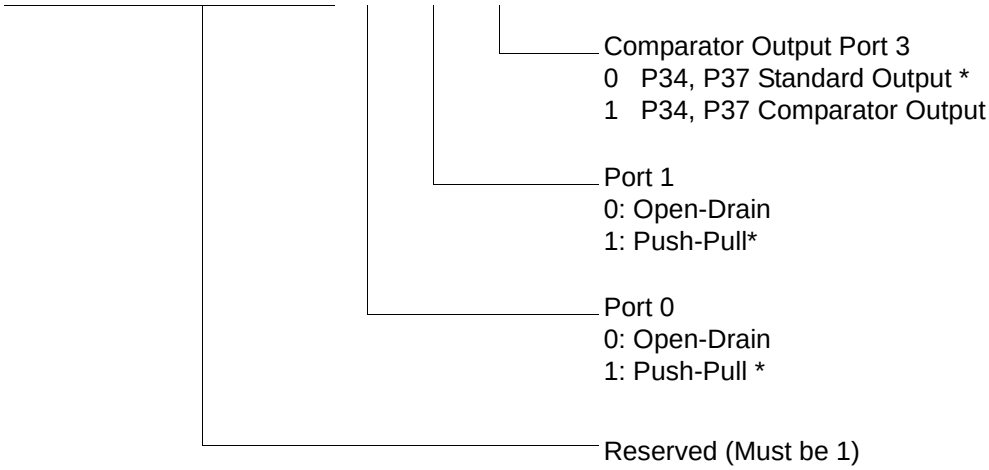



**Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

PCON(0F)00H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|




* Default setting after reset

**Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)**

R249 IPR(F9H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

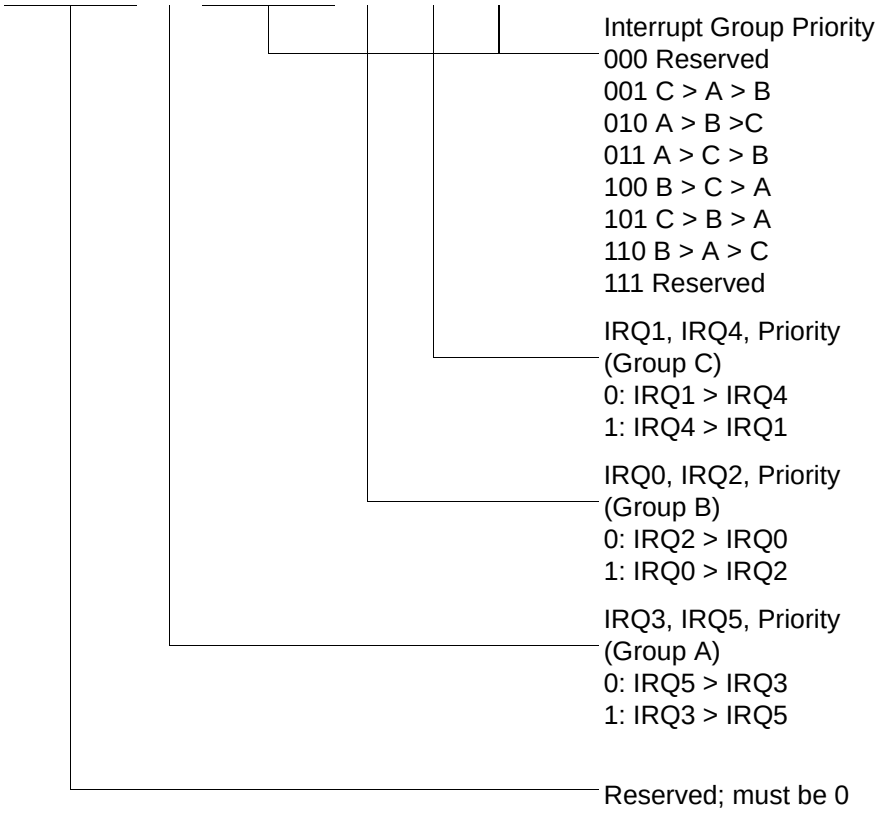



**Figure 51. Interrupt Priority Register (F9H: Write Only)**

R250 IRQ(FAH)

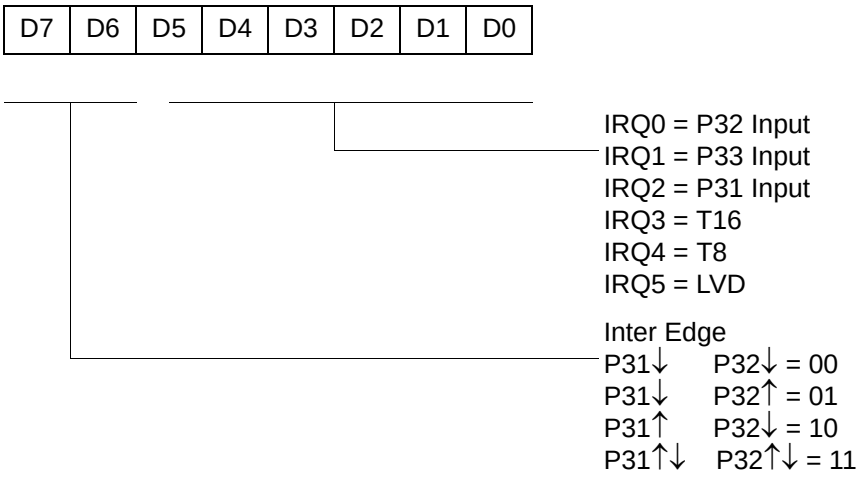
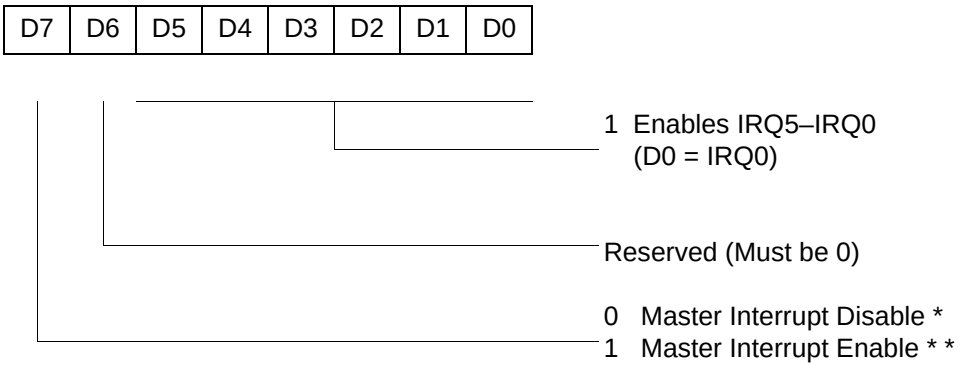



**Figure 52. Interrupt Request Register (FAH: Read/Write)**

R251 IMR(FBH)




* Default setting after reset
* * Only by using EI, DI instruction; DI is required before changing the IMR register

**Figure 53. Interrupt Mask Register (FBH: Read/Write)**

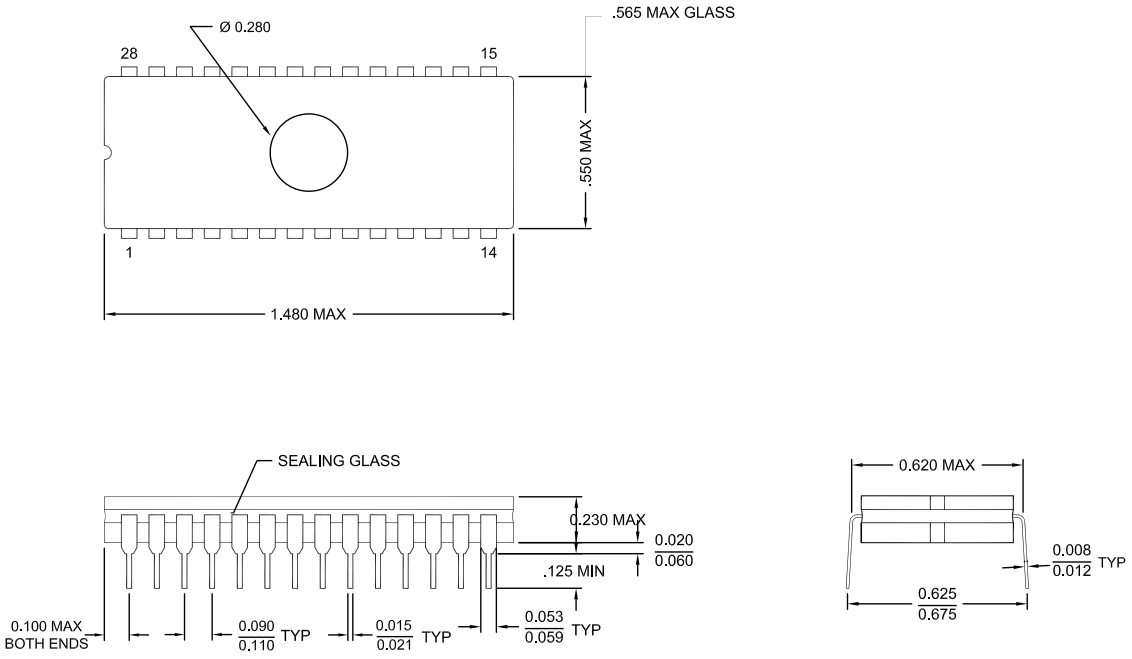
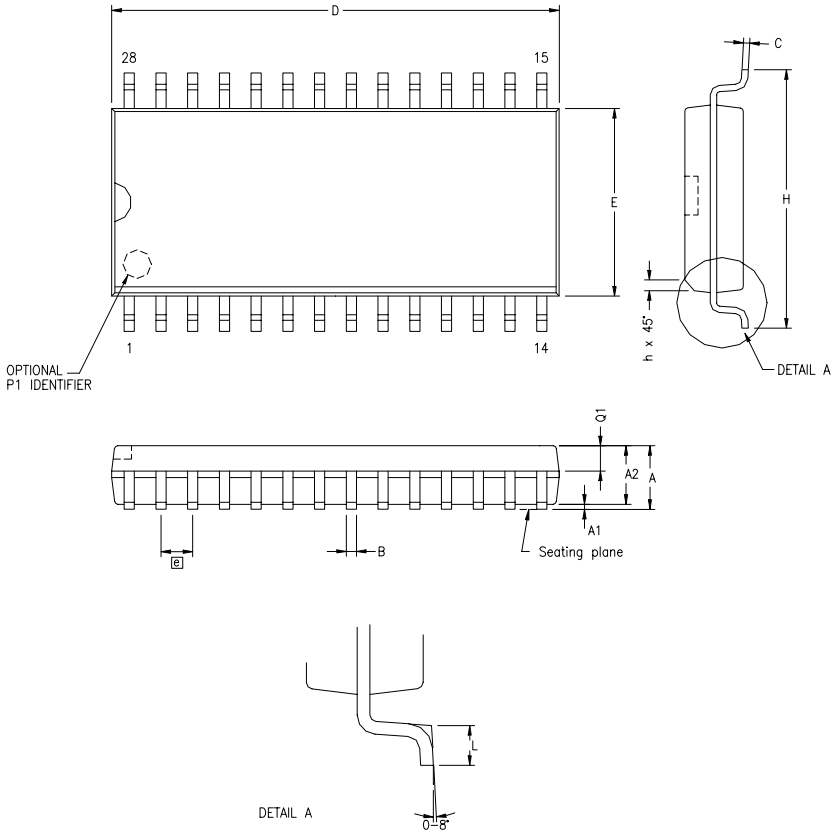


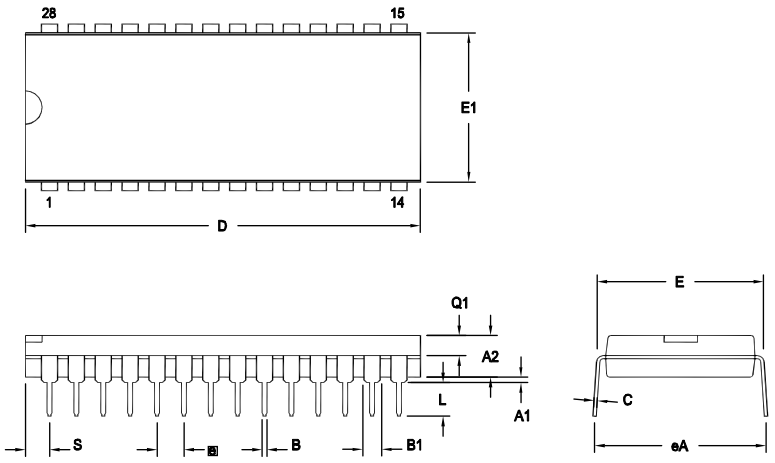

**Figure 62. 28-Pin CDIP Package**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.64 | .094 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.24 | 2.44 | .088 | .096 |
| B | 0.36 | 0.46 | .014 | .018 |
| C | 0.23 | 0.30 | .009 | .012 |
| D | 17.78 | 18.00 | .700 | .710 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 BSC | | .050 BSC | |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.30 | 0.71 | .012 | .028 |
| L | 0.61 | 1.00 | .024 | .039 |
| Q1 | 0.97 | 1.09 | .038 | .043 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 63. 28-Pin SOIC Package Diagram**




| SYMBOL | OPT # | MILLIMETER | | INCH | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| A1 | | 0.38 | 1.02 | .015 | .040 |
| A2 | | 3.18 | 4.19 | .125 | .165 |
| B | | 0.38 | 0.53 | .015 | .021 |
| B1 | 01 | 1.40 | 1.65 | .055 | .065 |
| | 02 | 1.14 | 1.40 | .045 | .055 |
| C | | 0.23 | 0.38 | .009 | .015 |
| D | 01 | 36.58 | 37.34 | 1.440 | 1.470 |
| | 02 | 35.31 | 35.94 | 1.390 | 1.415 |
| E | | 15.24 | 15.75 | .600 | .620 |
| E1 | 01 | 13.59 | 14.10 | .535 | .555 |
| | 02 | 12.83 | 13.08 | .505 | .515 |
| e | | 2.54 TYP | | .100 BSC | |
| eA | | 15.49 | 16.76 | .610 | .660 |
| L | | 3.05 | 3.81 | .120 | .150 |
| Q1 | 01 | 1.40 | 1.91 | .055 | .075 |
| | 02 | 1.40 | 1.78 | .055 | .070 |
| S | 01 | 1.52 | 2.29 | .060 | .090 |
| | 02 | 1.02 | 1.52 | .040 | .060 |

CONTROLLING DIMENSIONS : INCH

| OPTION TABLE | |
|---|---|
| OPTION # | PACKAGE |
| 01 | STANDARD |
| 02 | IDF |

Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

**Figure 64. 28-Pin PDIP Package Diagram**

# Index

## Numerics



## A



## B



## C

## S



## T



## V



## W



## X