Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lah2816c

Development Features

Table 1 lists the features of ZiLOG®'s Z8 GP™ OTP MCU Family family members.

Table 1. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323L OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–3.6V

- Low power consumption–6mW (typical)
- T = Temperature
  S = Standard 0° to +70°C
  E = Extended -40° to +105°C
  A = Automotive -40° to +125°C
- Three standby modes:
  - STOP—2μA (typical)
  - HALT—0.8mA (typical)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors

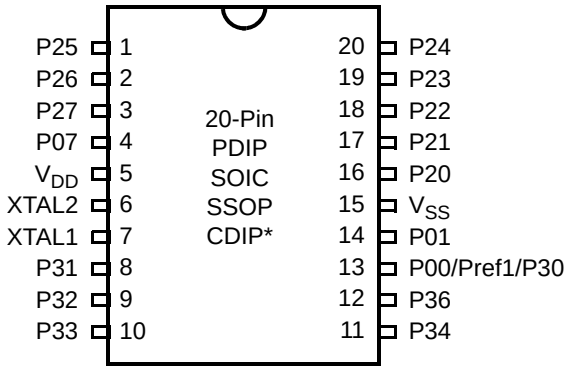


Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V_{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V_{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Capacitance

Table 7 lists the capacitances.

Table 7. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: T_A = 25° C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND	

DC Characteristics

Table 8. DC Characteristics

			T_A= 0°C to +70°C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	**Notes**
V_{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-3.6	0.8		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-3.6	V_{CC}–0.4			V	I_{OH} = –0.5mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V_{CC}–0.8			V	I_{OH} = –7mA	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	I_{OL} = 1.0mA I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-3.6	–1		1	µA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
I_{OL}	Output Leakage	2.0-3.6	–1		1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0 3.6			10 15	mA mA	at 8.0 MHz at 8.0 MHz	1, 2 1, 2

AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.

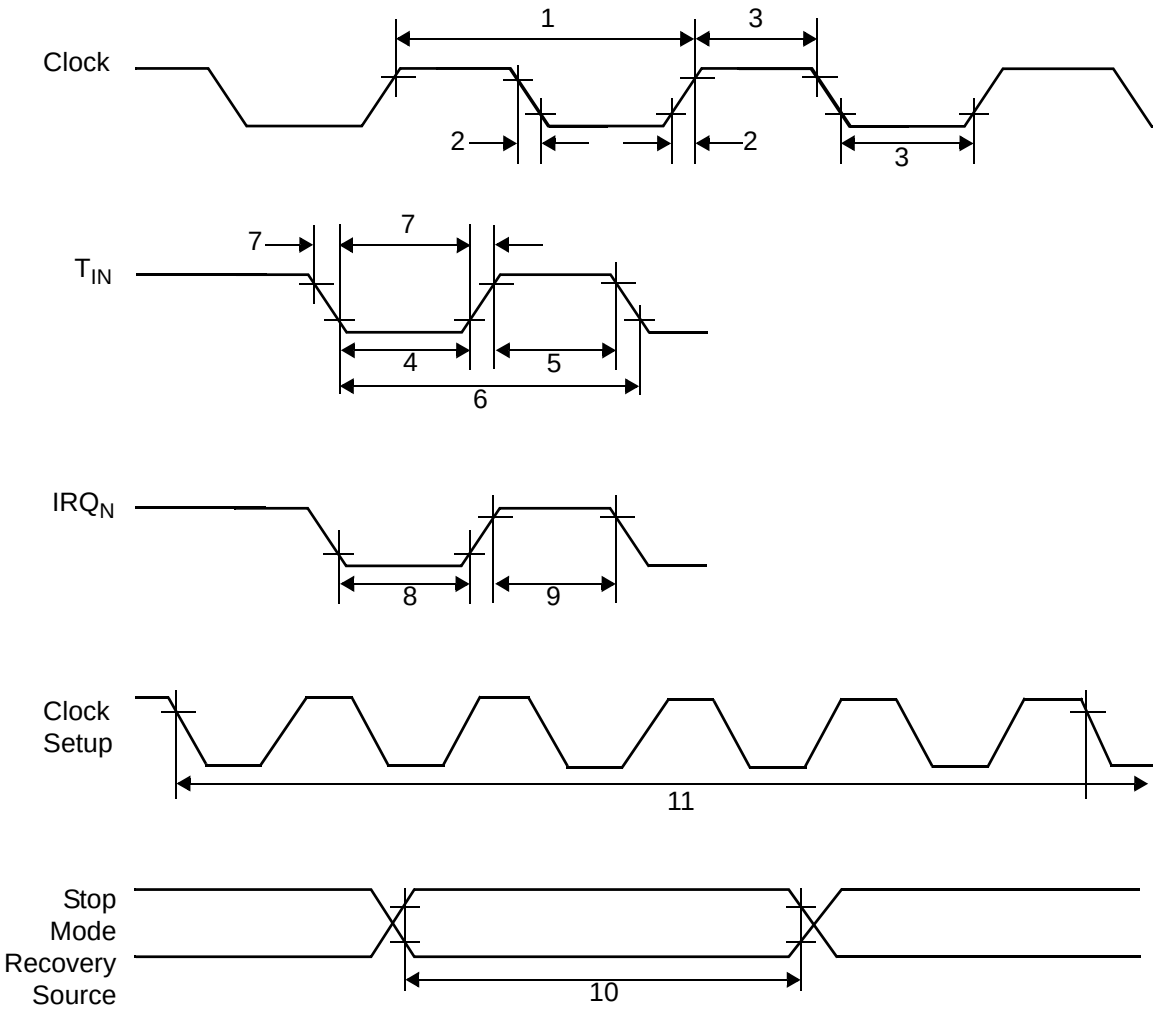


Figure 8. AC Timing Diagram

CTR1(0D)01H" on page 33). Other edge detect and IRQ modes are described in Table 11.

Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Table 11. Port 3 Pin Function Summary

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

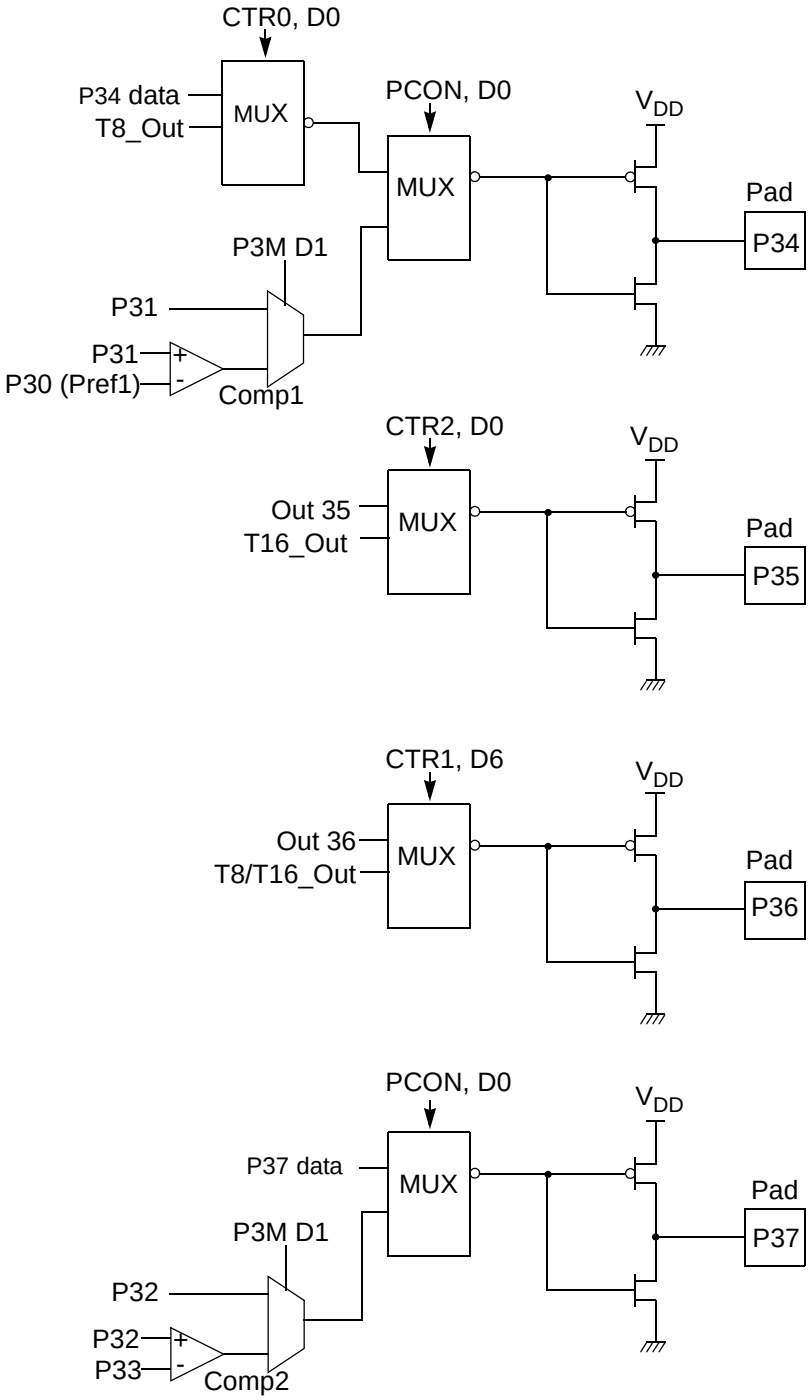


Figure 13. Port 3 Counter/Timer Output Configuration

ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: An expanded register bank is also referred to as an expanded register group (see Figure 15).

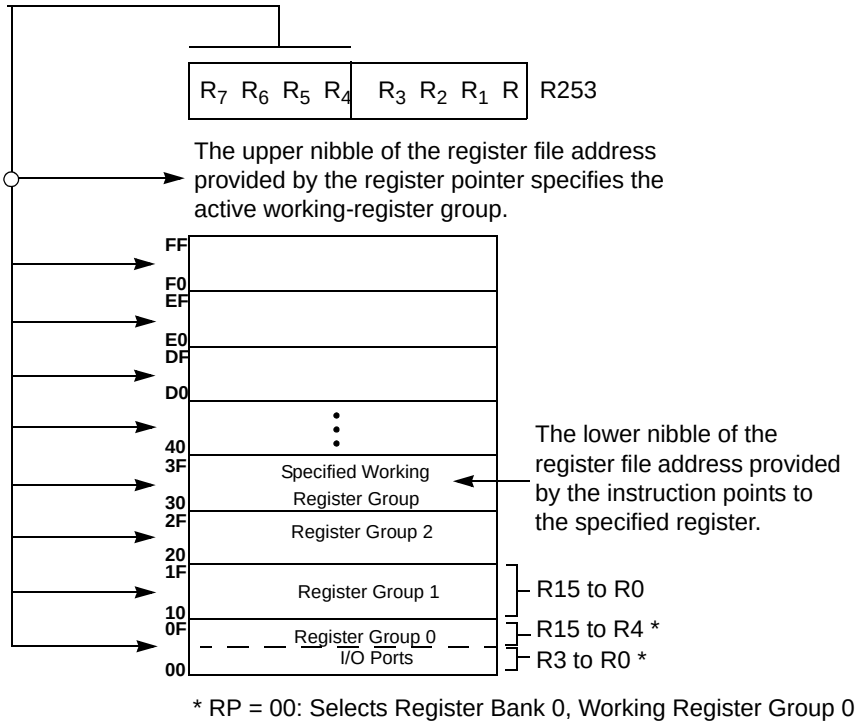


Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.

Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.

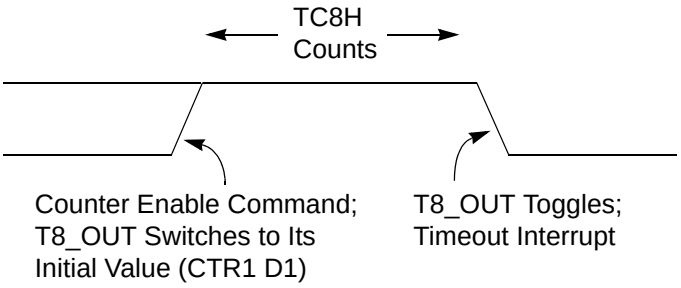


Figure 21. T8_OUT in Single-Pass Mode

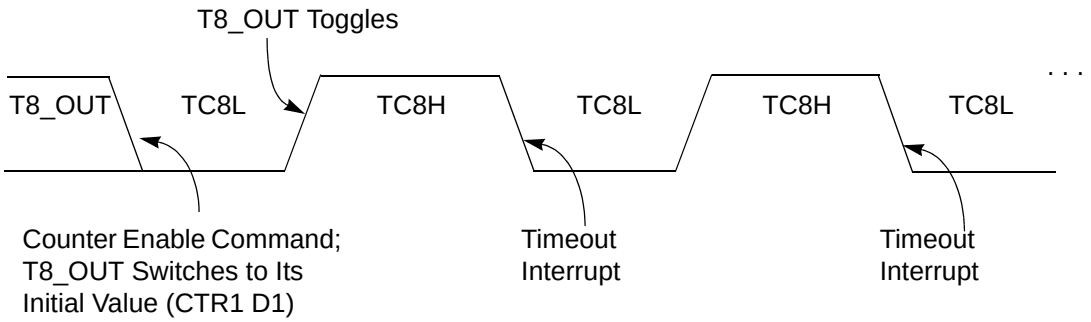


Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).

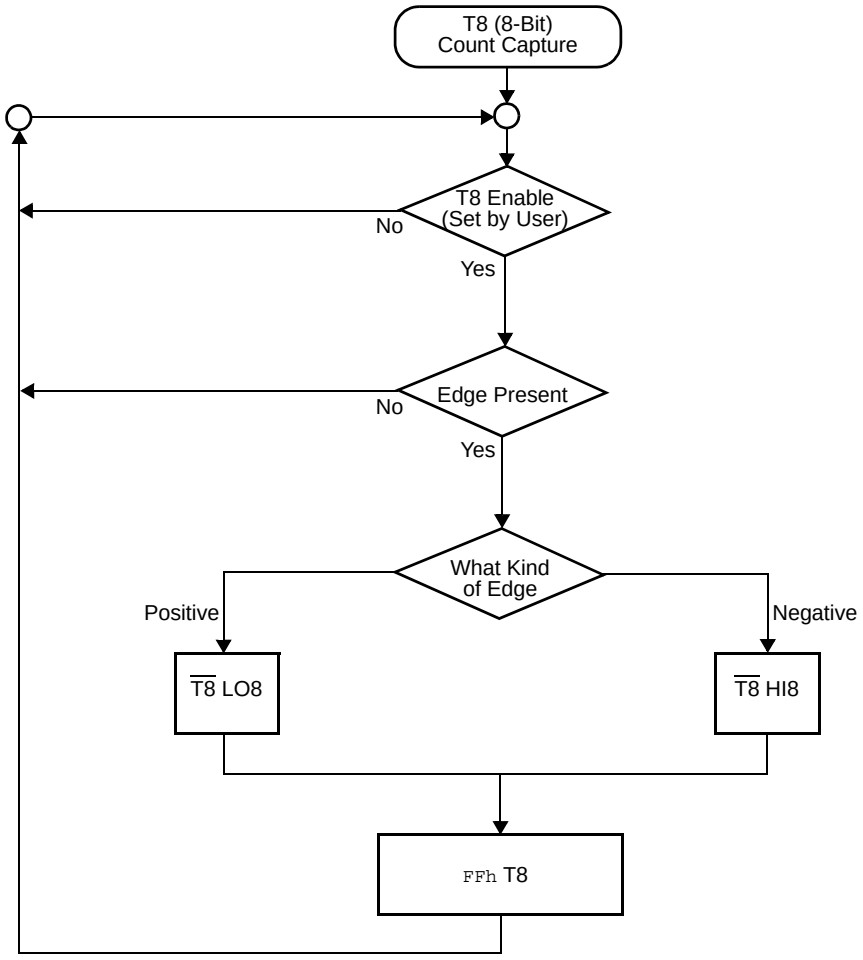
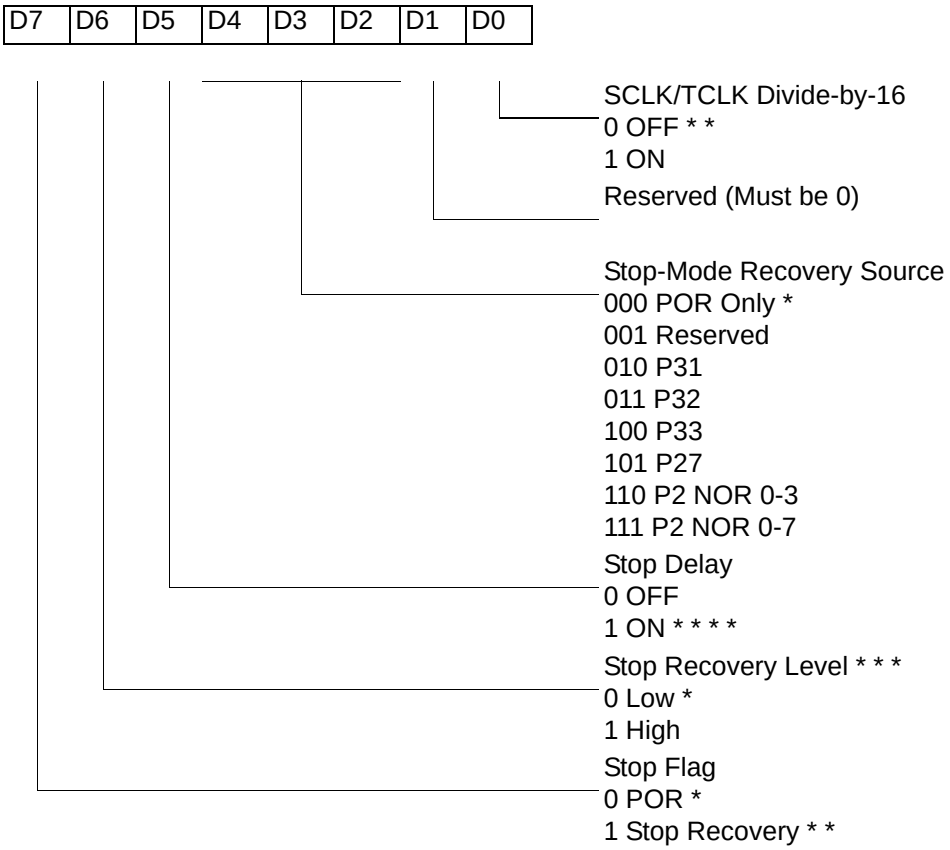


Figure 23. Demodulation Mode Count Capture Flowchart

SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset
* * Set after STOP Mode Recovery
* * * At the XOR gate input
* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

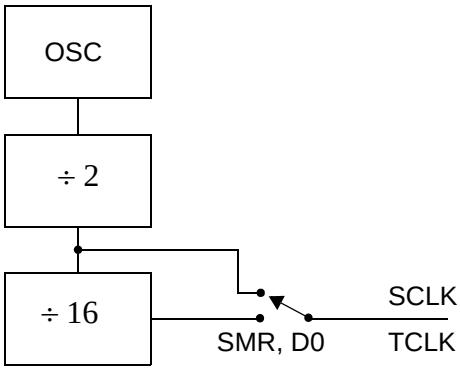


Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 19).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 18 lists and briefly describes the fields for this register.

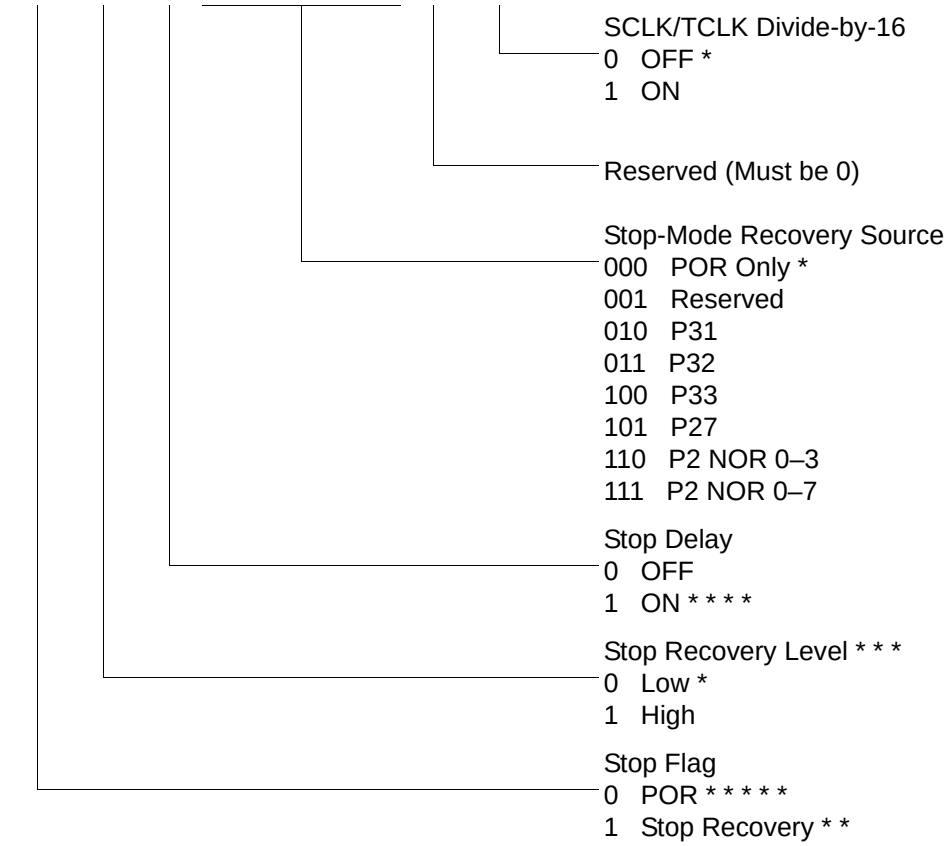
Table 18. SMR2(F)0DH:Stop Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0† 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000† 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND of P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Port pins configured as outputs are ignored as a SMR recovery source.
† Indicates the value upon Power-On Reset

SMR(0F)0BH

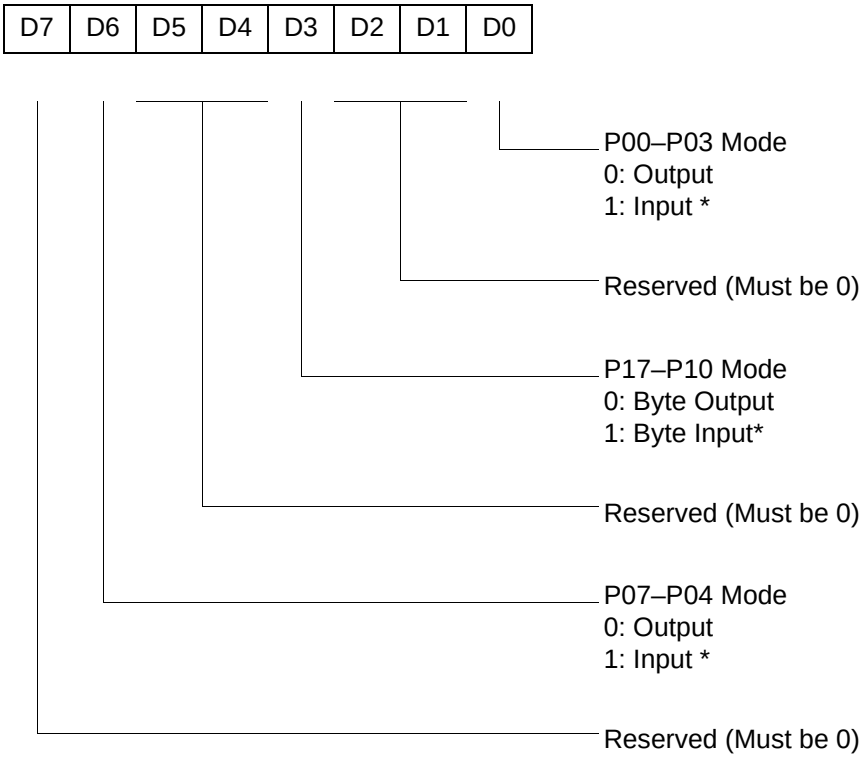
D7	D6	D5	D4	D3	D2	D1	D0



* Default setting after Reset
* * Set after STOP Mode Recovery
* * * At the XOR gate input
* * * * Default setting after Reset. Must be 1 if using a crystal or resonator clock source.
* * * * * Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

R248 P01M(F8H)



* Default setting after reset; only P00, P01 and P07 are available in 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)

R250 IRQ(FAH)

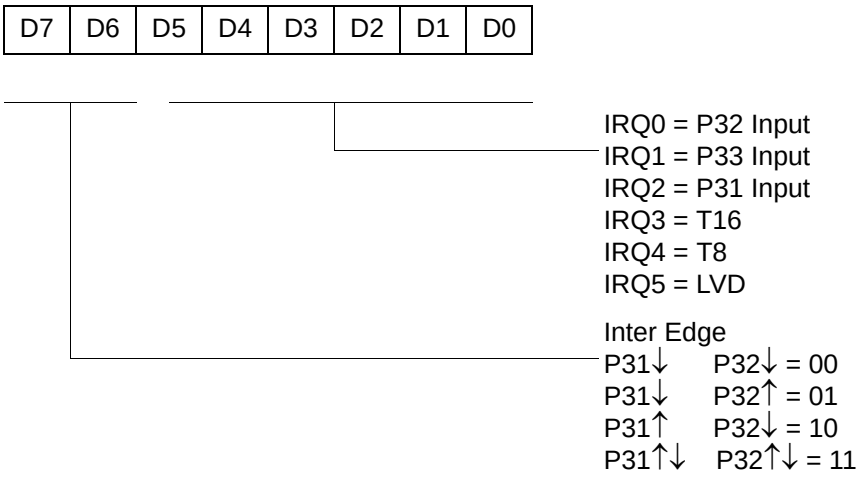
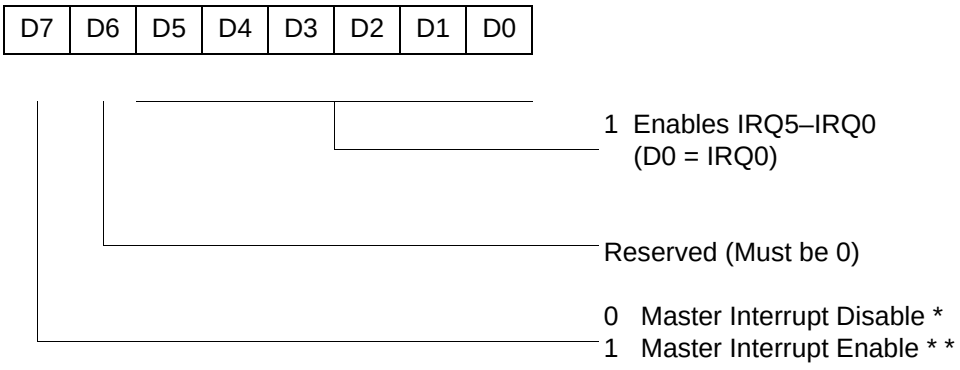


Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset
* * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)

R252 Flags(FCH)

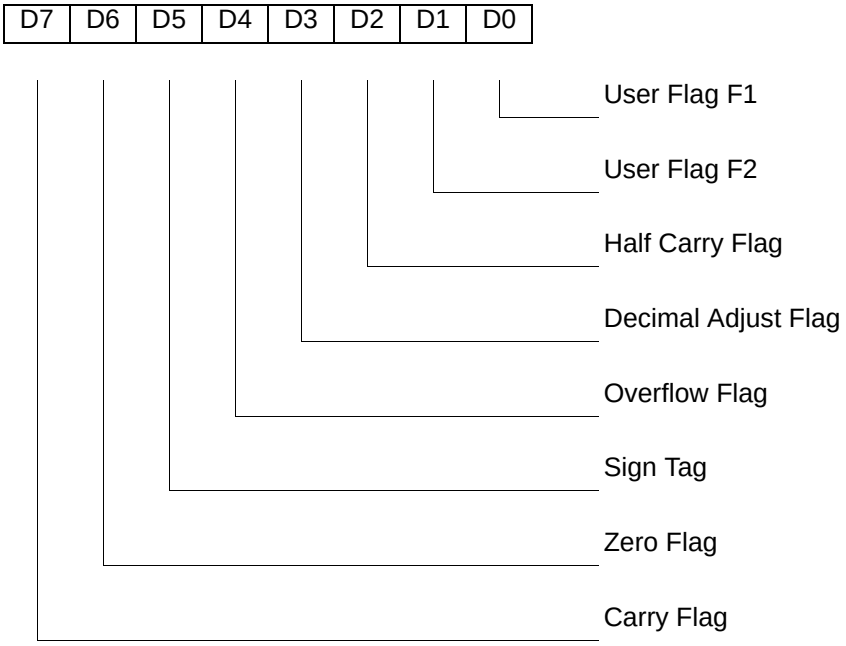
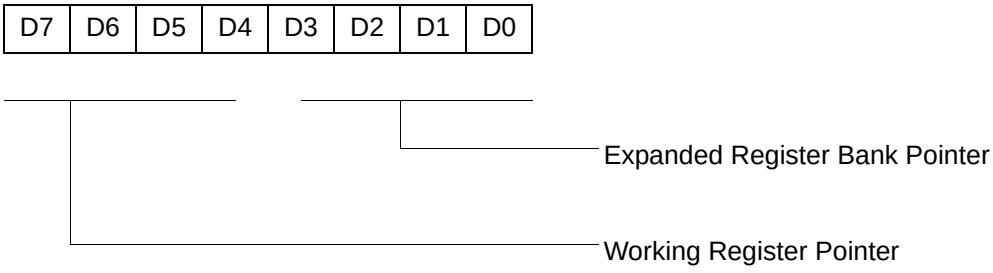


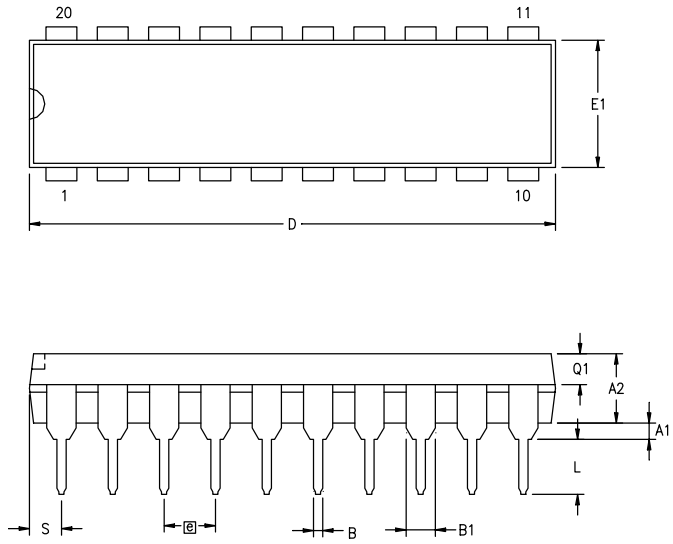
Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

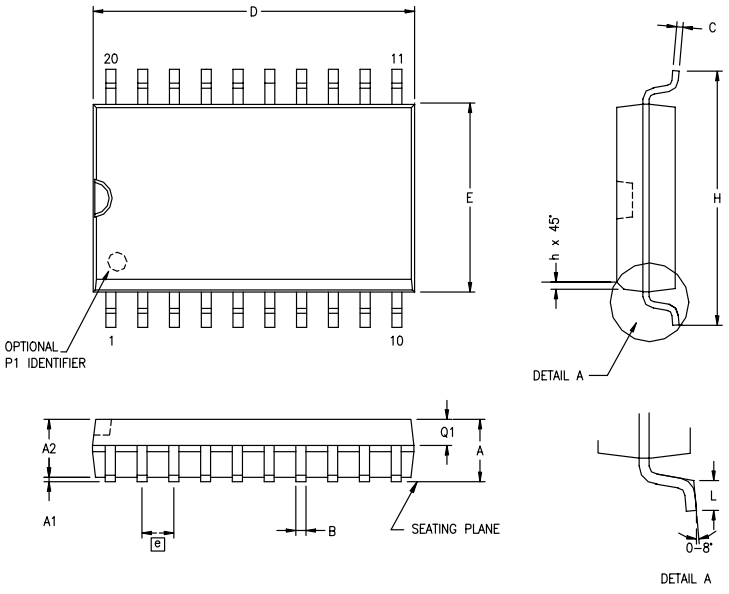
Figure 55. Register Pointer (FDH: Read/Write)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

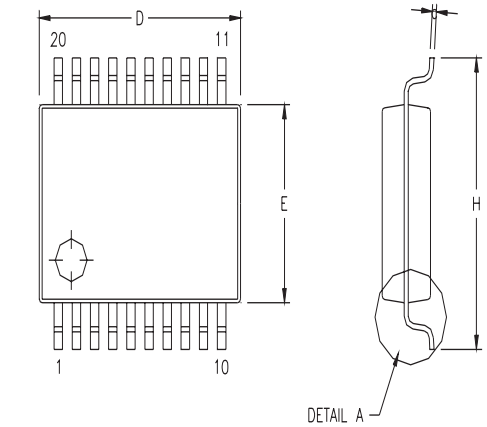
Figure 59. 20-Pin PDIP Package Diagram



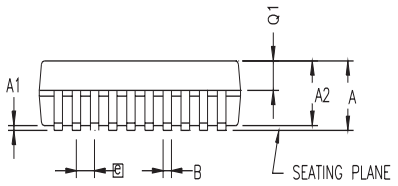
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	**.496**	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

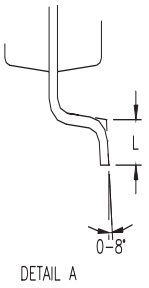
CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 60. 20-Pin SOIC Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram

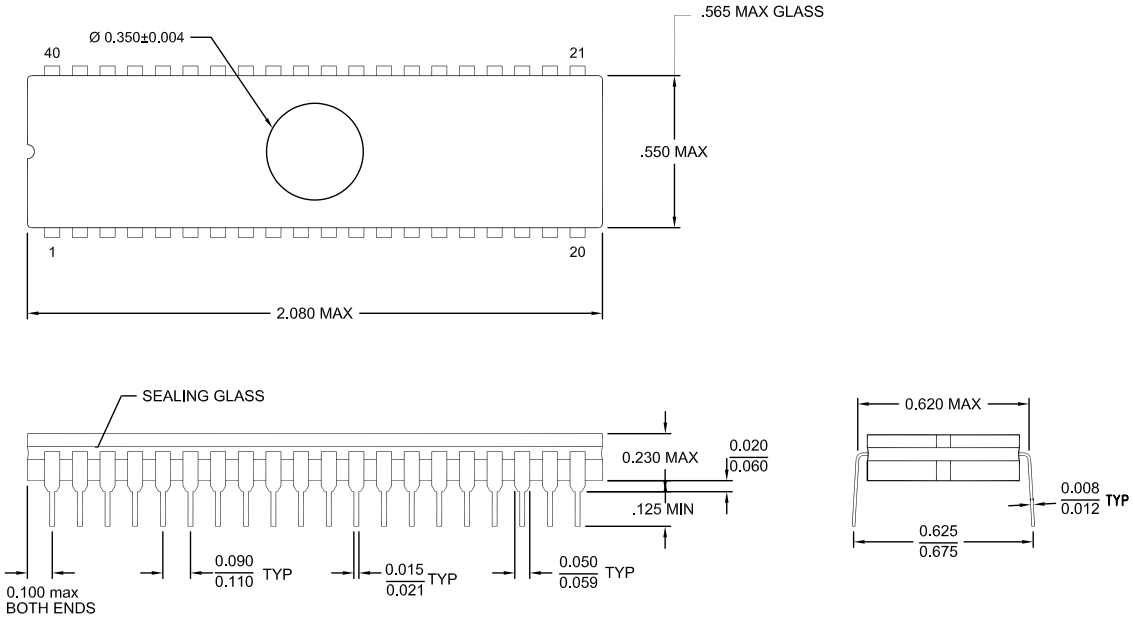
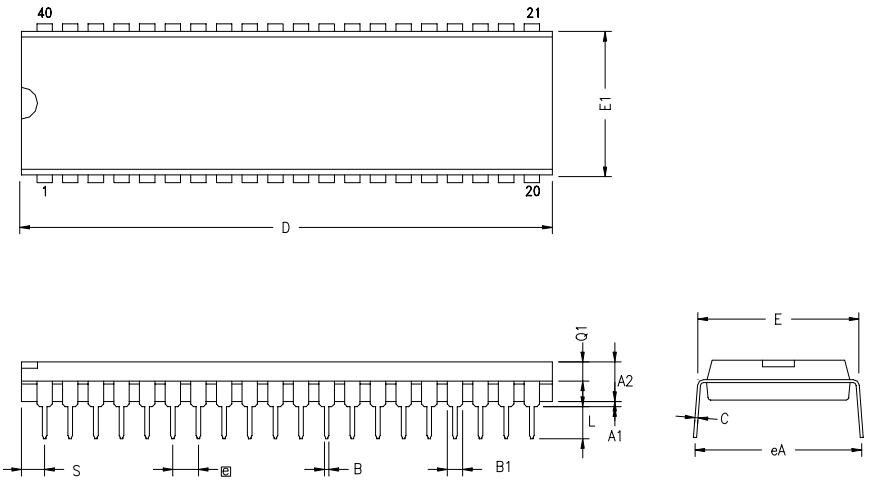


Figure 66. 40-Pin CDIP Package



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 67. 40-Pin PDIP Package Diagram

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

E = -40 to +105 degrees C (Extended)

A = -40 to +125 degrees C (Automotive)

P = Package Type:

K = Windowed Cerdip
P = PDIP
H = SSOP
S = SOIC

= Number of Pins

CC = Memory Size

M = Packaging Options

C = Non Lead-Free

G = Lead-Free

E = CDIP