Zilog - ZGP323LAH2832C Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lah2832c

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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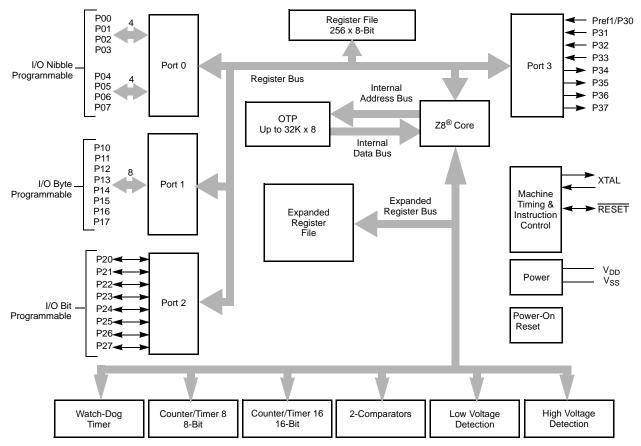
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Table 2. Power Connections

Connection	Circuit	Device	
Power	V _{CC}	V _{DD}	
Ground	GND	V _{SS}	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram





		\bigcirc	
NC			40 ⊐ NC
P25			39 □ P24
P26			38 🗖 P23
P27	□ 4		37 🗖 P22
P04	□ 5		36 🗖 P21
P05	□ 6	40-Pin	35 🗖 P20
P06	– 7	PDIP	34 🗖 P03
P14	□ 8	CDIP*	33 🗖 P13
P15	□ 9	ODI	32 🗖 P12
P07	1 0		31 🗖 VSS
VDD	– 11		30 🗖 P02
P16	1 2		39 🗖 P11
P17	1 3		28 🗖 P10
XTAL2	□ 14		27 🗖 P01
XTAL1	□ 15		26 🗖 P00
P31	1 6		25 🗖 Pref1/P30
P32	17		24 🗖 P36
P33	1 8		23 🗖 P37
P34	□ 19		22 🗖 P35
NC	20		21 🗖 RESET

Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.



40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC

Table 5. 40- and 48-Pin Configuration (Continued)

11

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Capacitance

Table 7 lists the capacitances.

Table 7. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ C$, $V_{CC} = GND = 0^\circ$	V, $f = 1.0$ MHz, unmeasured pins returned to GND

DC Characteristics

			T _A = 0°C	to +7	′0°C			
Symbol	Parameter	V _{CC}	Min	Тур	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-3.6	0.8		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-3.6	V _{SS} -0.3		0.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-3.6	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-3.6	V _{SS} -0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-3.6	V _{CC} -0.4			V	I _{OH} = -0.5mA	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 1.0 \text{mA}$ $I_{OL} = 4.0 \text{mA}$	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-3.6	0		V _{DD} -1.75	V		
۱ _{IL}	Input Leakage	2.0-3.6	-1		1	μΑ	V _{IN} = 0V, V _{CC} Pull-ups disabled	
IOL	Output Leakage	2.0-3.6	-1		1	μΑ	$V_{IN} = 0V, V_{CC}$	
ICC	Supply Current	2.0 3.6			10 15	mA mA	at 8.0 MHz at 8.0 MHz	1, 2 1, 2



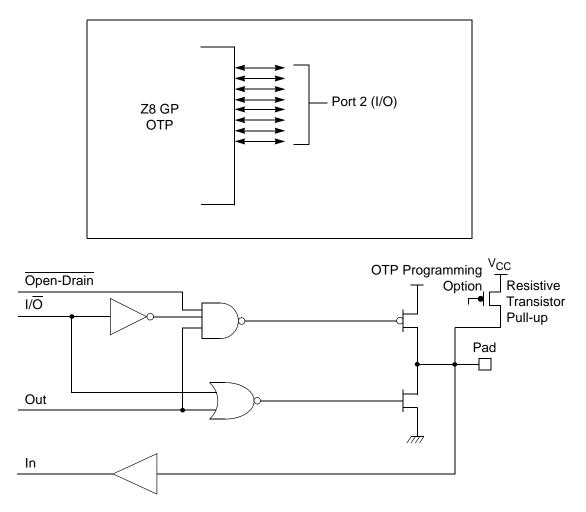


Figure 11. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

>

Note: An expanded register bank is also referred to as an expanded register group (see Figure 15).



Z8 [®] Standard (Control Registers	Reset Condition
	Expanded Reg. Bank 0/Group 15*	* D7 D6 D5 D4 D3 D2 D1 D0
	FF SPL	
	FE SPH	U U U U U U U U
Register Pointer	FD RP	0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	FC FLAGS	U U U U U U U U
	FB IMR	U U U U U U U U
Working Register Expanded Register	er FA IRQ	0 0 0 0 0 0 0 0
Group Pointer Bank Pointer	F9 IPR	U U U U U U U U
	F8 P01M	1 1 0 0 1 1 1 1
	* F7 P3M	00000000
	* F6 P2M	1 1 1 1 1 1 1 1
	F5 Reserved	U U U U U U U U
	F4 Reserved	U U U U U U U U
	F3 Reserved	$\cup \cup \cup \cup \cup \cup \cup \cup \cup$
Register File (Bank 0)** /	F2 Reserved	$\cup \cup \cup \cup \cup \cup \cup \cup \cup$
FF F0	F1 Reserved	$\cup \cup \cup \cup \cup \cup \cup \cup \cup$
F0	F0 Reserved	U U U U U U U U
	Expanded Reg. Bank F/Group 0**	
	(F) OF WDTMR	UU001101
	(F) 0E Reserved	
	* (F) 0D SMR2	0 0 0 0 0 0 0 0
	(F) 0C Reserved	
7F	↑ (F) 0B SMR	U 0 1 0 0 0 U 0
/F	(F) 0A Reserved	
	(F) 09 Reserved	
	(F) 08 Reserved	
	(F) 07 Reserved	
	(F) 06 Reserved	
	(F) 05 Reserved	
₀₅ ┝━━━━━━┓┛┙	(F) 04 Reserved	
	(F) 03 Reserved	
	(F) 02 Reserved	
	(F) 01 Reserved	
Expanded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1 1 1 1 1 0
(0) 03 P3 0 U	Expanded Reg. Bank D/Group 0	
	(D) 0C LVD	$\cup \cup \cup \cup \cup \cup \cup 0$
(0) 02 P2 U	* (D) 0B HI8	000000000
* (0) 01 P1 U	* (D) 0A LO8	000000000
	* (D) 09 HI16	0 0 0 0 0 0 0 0
(0) 00 P0 U	* (D) 08 LO16	0 0 0 0 0 0 0 0
U = Unknown	* (D) 07 TC16H	0 0 0 0 0 0 0 0
* Is not reset with a Stop-Mode Recovery	* (D) 06 TC16L	0 0 0 0 0 0 0
** All addresses are in hexadecimal	* (D) 05 TC8H	0 0 0 0 0 0 0
↑ Is not reset with a Stop-Mode Recovery, except Bit 0	* (D) 04 TC8L	0 0 0 0 0 0 0 0
↑↑ Bit 5 Is not reset with a Stop-Mode Recovery	1↑ (D) 03 CTR3	0 0 0 1 1 1 1 1
↑↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery	↑↑↑ (D) 02 CTR2	0 0 0 0 0 0 0 0
↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery	^^↑↑↑ (D) 01 CTR1	0 0 0 0 0 0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	000000000
		-

Figure 15. Expanded Register File Architecture

Z i L 0 G 36

Field	Bit Position		Value	Description
T16_Enable	7	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W		Transmit Mode
			0*	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	5	R	0*	No Counter Timeout
			1	Counter Timeout
				Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	43	R/W	00**	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	1-	R/W	0	Disable Timeout Int.
			1	Enable Timeout Int.
P35_Out	0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Table 14. CTR2(D)02H: Counter/Timer16 Control Register

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset.Not reset with Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

38

Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	43210	R	1	Always reads 11111
		W	х	No Effect

Note: *Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5– D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

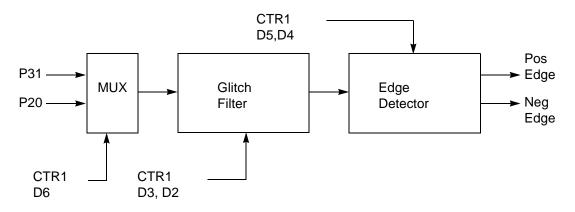


Figure 18. Glitch Filter Circuitry

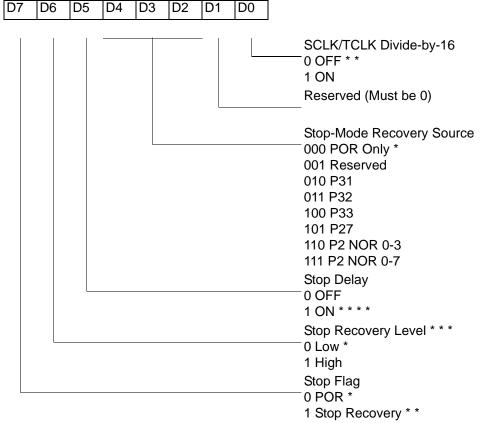
T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.





SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

- * * Set after STOP Mode Recovery
- * * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

Table 21. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.



CTR1(0D)01H D7 D6 D5 D3 D1 D0 D4 D2 Transmit Mode* R/W 0 T16_OUT is 0 initially* 1 T16_OUT is 1 initially **Demodulation Mode** R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially **Demodulation Mode** R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 **Demodulation Mode** 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 1 Reserved Transmit Mode/T8/T16 Logic 0 0 AND** 0 1 OR 1 0 NOR 1 1 NAND **Demodulation Mode** 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 1 Reserved Transmit Mode 0 P36 as Port Output * 1 P36 as T8/T16_OUT **Demodulation Mode** 0 P31 as Demodulator Input 1 P20 as Demodulator Input Transmit/Demodulation Mode 0 Transmit Mode * * Default setting after reset **Default setting after reset. Not reset with Stop Mode 1 Demodulation Mode recovery





R252 Flags(FCH)

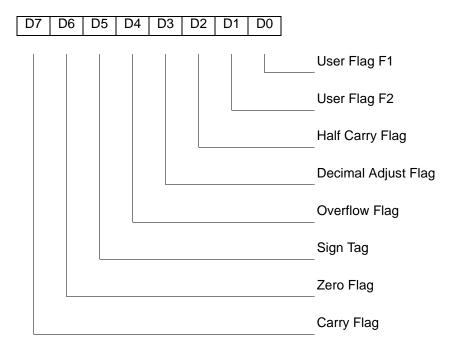
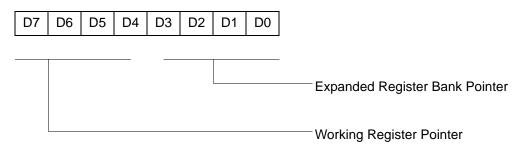


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)

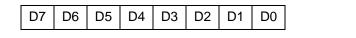


Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)



R254 SPH(FEH)



General-Purpose Register

Figure 56. Stack Pointer High (FEH: Read/Write)

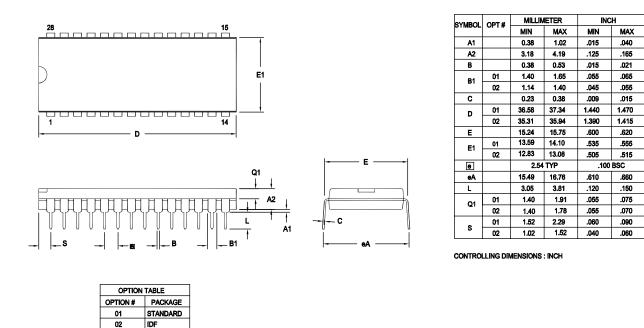
R255 SPL(FFH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Stack Pointer Low Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)





Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 64. 28-Pin PDIP Package Diagram

INCH

NOM

0.073

0.005

0.068

0.006

0.402

0.209

0.307

0.030

0.0256 TYP



MAX

0.078

0.008

0.070

0.015

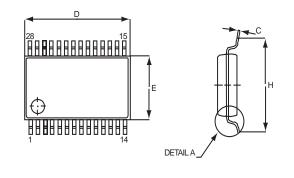
0.008

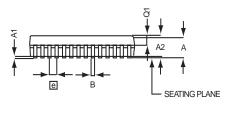
0.407

0.212

0.311

0.037





0-8°

DETAIL 'A'

SYMBOL

А

A1

A2

В

С

D

Е

е

Н

L

MIN

1.73

0.05

1.68

0.25

0.09

10.07

5.20

7.65

0.63

CONTROLLING DIMENSIONS: MM LEADS ARE COPLANAR WITHIN .004 INCHES.

MILLIMETER

NOM

1.86

0.13

1.73

_

10.20

5.30

0.65 TYP

7.80

0.75

MAX

1.99

0.21

1.78

0.38

0.20

10.33

5.38

7.90

0.95

MIN

0.068

0.002

0.066

0.010

0.004

0.397

0.205

0.301

0.025

Figure 65. 28-Pin SSOP Package Diagram

Z i L 0 G 92

4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4804C	48-pin SSOP 4K OTP	ZGP323LSS2804C	28-pin SOIC 4K OTP
ZGP323LSP4004C	40-pin PDIP 4K OTP	ZGP323LSH2004C	20-pin SSOP 4K OTP
ZGP323LSH2804C	28-pin SSOP 4K OTP	ZGP323LSP2004C	20-pin PDIP 4K OTP
ZGP323LSP2804C	28-pin PDIP 4K OTP	ZGP323LSS2004C	20-pin SOIC 4K OTP

4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4804C	48-pin SSOP 4K OTP	ZGP323LES2804C	28-pin SOIC 4K OTP
ZGP323LEP4004C	40-pin PDIP 4K OTP	ZGP323LEH2004C	20-pin SSOP 4K OTP
ZGP323LEH2804C	28-pin SSOP 4K OTP	ZGP323LEP2004C	20-pin PDIP 4K OTP
ZGP323LEP2804C	28-pin PDIP 4K OTP	ZGP323LES2004C	20-pin SOIC 4K OTP

4KB Automotive Temperature: -40° to +125°C

	•		
Part Number	Description	Part Number	Description
ZGP323LAH4804C	48-pin SSOP 4K OTP	ZGP323LAS2804C	28-pin SOIC 4K OTP
ZGP323LAP4004C	40-pin PDIP 4K OTP	ZGP323LAH2004C	20-pin SSOP 4K OTP
ZGP323LAH2804C	28-pin SSOP 4K OTP	ZGP323LAP2004C	20-pin PDIP 4K OTP
ZGP323LAP2804C	28-pin PDIP 4K OTP	ZGP323LAS2004C	20-pin SOIC 4K OTP

Note: Replace C with G for Lead-Free Packaging

Additional Components

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer	ZGP32300100ZPR	Programming System

93

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

- 323 = Family Designation
- L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

- E = -40 to +105 degrees C (Extended)
- A = -40 to +125 degrees C (Automotive)
- P = Package Type:
 - K = Windowed Cerdip
 - P = PDIP
 - H = SSOP
 - S = SOIC
- ## = Number of Pins
- CC = Memory Size
- M = Packaging Options
 - C = Non Lead-Free
 - G = Lead-Free
 - E = CDIP



Μ

memory, program 23 modulo-N mode T16_OUT 45 T8_OUT 41

0

oscillator configuration 51 output circuit, counter/timer 47

Ρ

package information 20-pin DIP package diagram 81 20-pin SSOP package diagram 82 28-pin DIP package diagram 85 28-pin SOIC package diagram 84 28-pin SSOP package diagram 86 40-pin DIP package diagram 87 48-pin SSOP package diagram 88 pin configuration 20-pin DIP/SOIC/SSOP 5 28-pin DIP/SOIC/SSOP 6 40- and 48-pin 8 40-pin DIP 7 48-pin SSOP 8 pin functions port 0 (P07 - P00) 16 port 0 (P17 - P10) 17 port 0 configuration 17 port 1 configuration 18 port 2 (P27 - P20) 18 port 2 (P37 - P30) 19 port 2 configuration 19 port 3 configuration 20 port 3 counter/timer configuration 22 reset) 23 XTAL1 (time-based input 16 XTAL2 (time-based output) 16 ping-pong mode 46 port 0 configuration 17 port 0 pin function 16

port 1 configuration 18 port 1 pin function 17 port 2 configuration 19 port 2 pin function 18 port 3 configuration 20 port 3 pin function 19 port 3counter/timer configuration 22 port configuration register 53 power connections 3 power supply 5 precharacterization product 95 program memory 23 map 24

R

ratings, absolute maximum 10 register 59 CTR(D)01h 33 CTR0(D)00h 31 CTR2(D)02h 35 CTR3(D)03h 37 flag 78 HI16(D)09h 30 HI8(D)0Bh 30 interrupt priority 76 interrupt request 77 interruptmask 77 L016(D)08h 30 L08(D)0Ah 30 LVD(D)0Ch 63 pointer 78 port 0 and 1 75 port 2 configuration 73 port 3 mode 74 port configuration 53, 73 SMR2(F)0Dh 38 stack pointer high 79 stack pointer low 79 stop mode recovery 55 stop mode recovery 2 59 stop-mode recovery 71 stop-mode recovery 2 72 T16 control 67