Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lah2832g

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
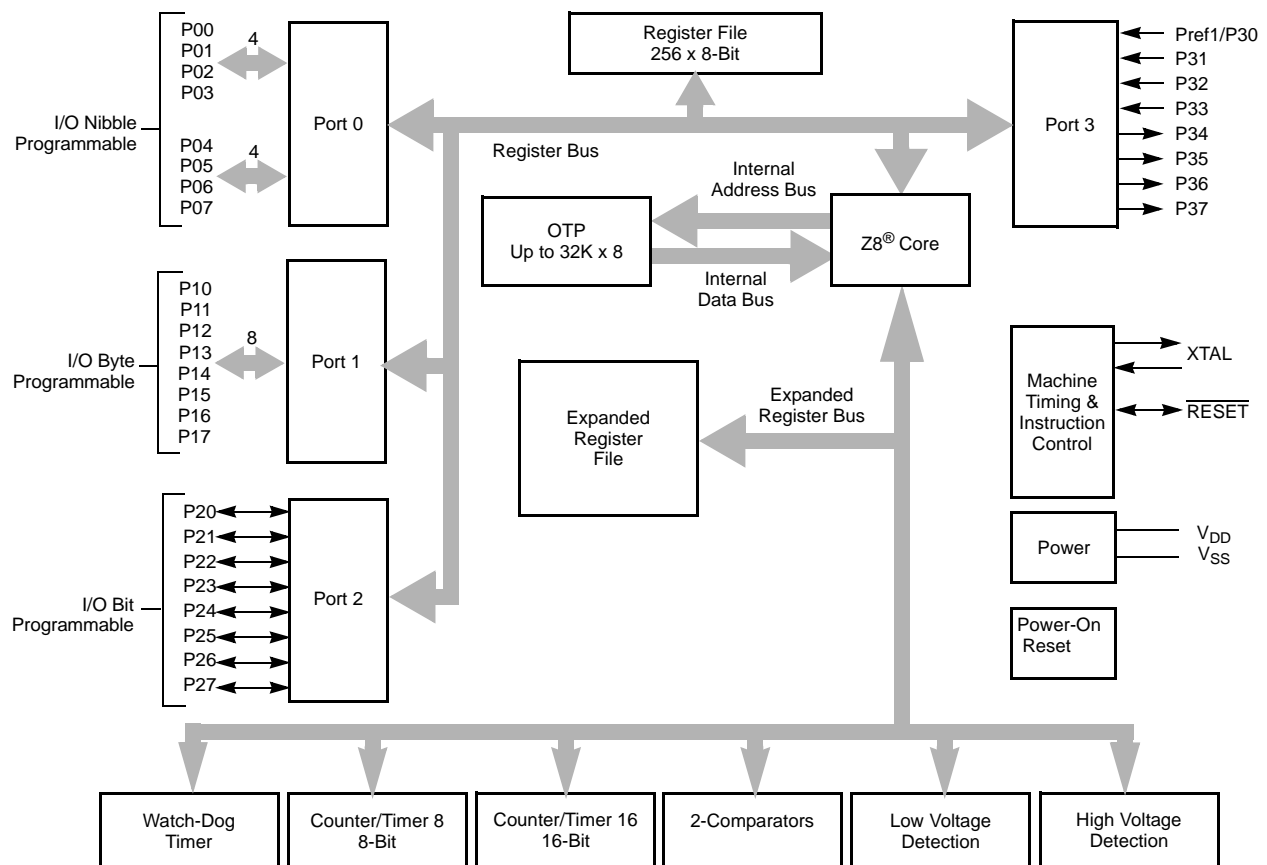Fax: 408.558.8300
www.zilog.com

Document Disclaimer

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

Capacitance

Table 7 lists the capacitances.

Table 7. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF

Note: T_A = 25° C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND

DC Characteristics

Table 8. DC Characteristics

Symbol	Parameter	V_{CC}	T_A= 0°C to +70°C			Units	Conditions	Notes
			Min	Typ	Max			
V_{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-3.6	0.8		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	V_{SS}−0.3		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-3.6	V_{SS}−0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-3.6	V_{CC}−0.4			V	I_{OH} = −0.5mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V_{CC}−0.8			V	I_{OH} = −7mA	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	I_{OL} = 1.0mA I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-3.6	−1		1	µA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
I_{OL}	Output Leakage	2.0-3.6	−1		1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0			10	mA	at 8.0 MHz	1, 2
		3.6			15	mA	at 8.0 MHz	1, 2
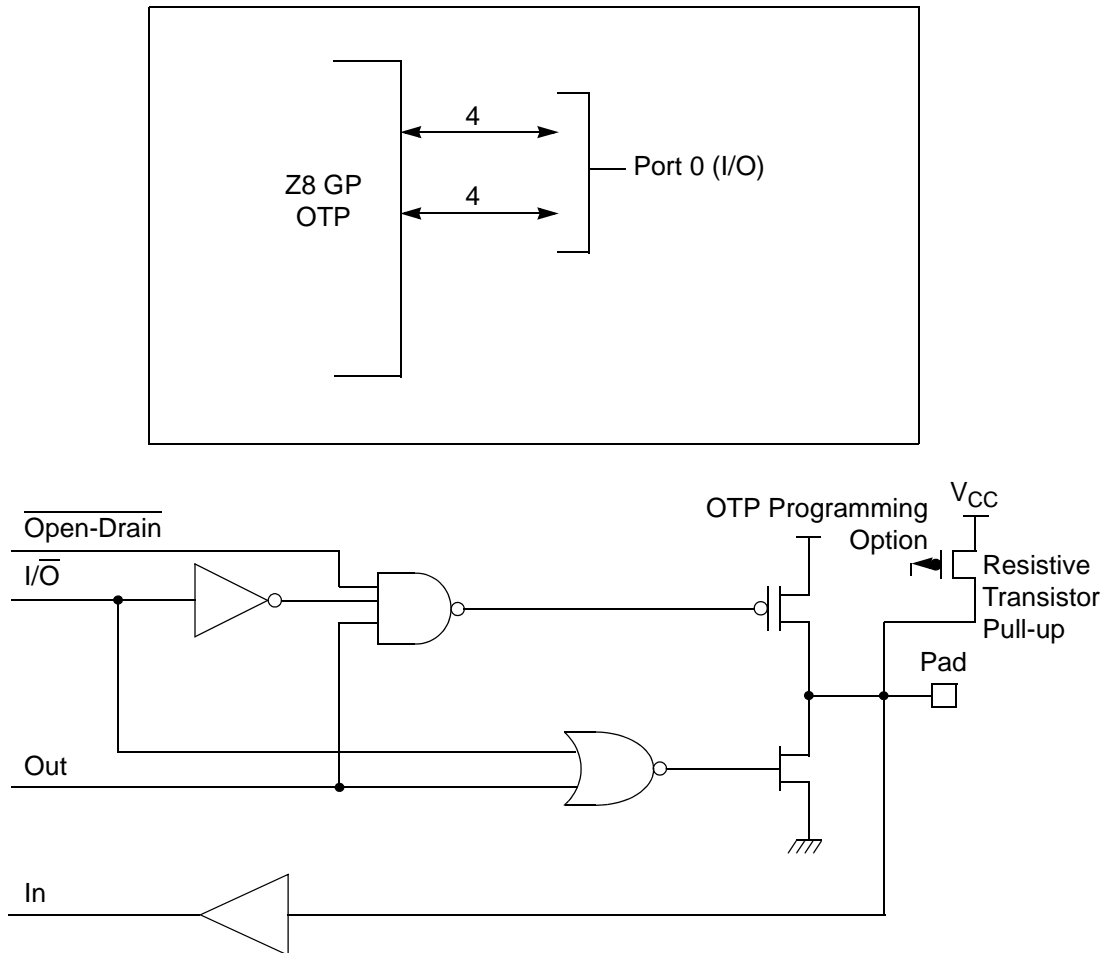
Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

▶ **Note:** The Port 1 direction is reset to be input following an SMR.
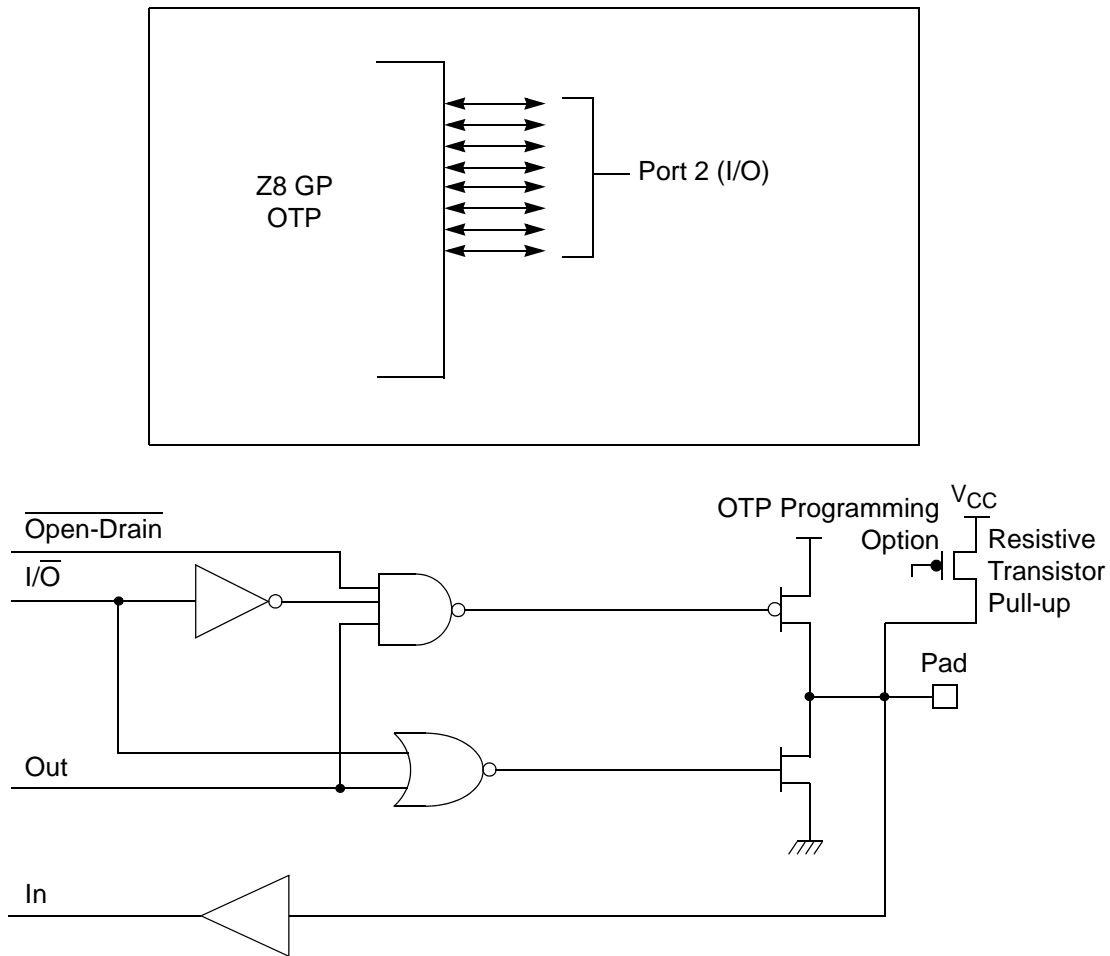
Figure 11. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

Z8® Standard Control Registers

Reset Condition

Register Pointer

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Working Register Group Pointer

Expanded Register Bank Pointer

Register File (Bank 0)**

FF
F0

7F

0F
00

Expanded Reg. Bank 0/Group 15**

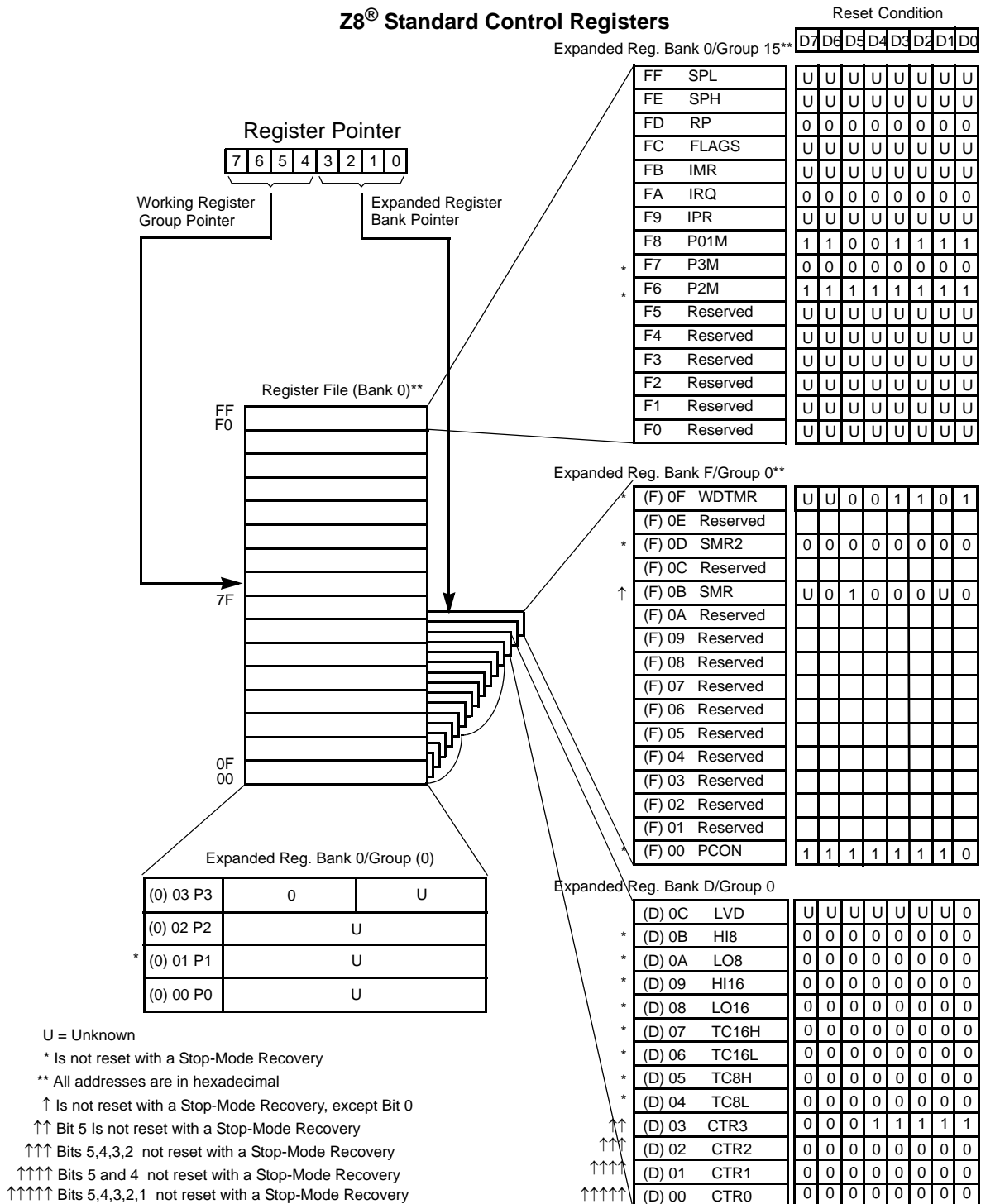|		D7	D6	D5	D4	D3	D2	D1	D0
FF	SPL	U	U	U	U	U	U	U	U
FE	SPH	U	U	U	U	U	U	U	U
FD	RP	0	0	0	0	0	0	0	0
FC	FLAGS	U	U	U	U	U	U	U	U
FB	IMR	U	U	U	U	U	U	U	U
FA	IRQ	0	0	0	0	0	0	0	0
F9	IPR	U	U	U	U	U	U	U	U
F8	P01M	1	1	0	0	1	1	1	1
* F7	P3M	0	0	0	0	0	0	0	0
* F6	P2M	1	1	1	1	1	1	1	1
F5	Reserved	U	U	U	U	U	U	U	U
F4	Reserved	U	U	U	U	U	U	U	U
F3	Reserved	U	U	U	U	U	U	U	U
F2	Reserved	U	U	U	U	U	U	U	U
F1	Reserved	U	U	U	U	U	U	U	U
F0	Reserved	U	U	U	U	U	U	U	U

Expanded Reg. Bank F/Group 0**

			D7	D6	D5	D4	D3	D2	D1	D0
*	(F) 0F	WDTMR	U	U	0	0	1	1	0	1
	(F) 0E	Reserved								
*	(F) 0D	SMR2	0	0	0	0	0	0	0	0
	(F) 0C	Reserved								
↑	(F) 0B	SMR	U	0	1	0	0	0	U	0
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
*	(F) 00	PCON	1	1	1	1	1	1	1	0

Expanded Reg. Bank 0/Group (0)

(0) 03 P3	0	U
(0) 02 P2	U	
* (0) 01 P1	U	
(0) 00 P0	U	

U = Unknown

* Is not reset with a Stop-Mode Recovery

** All addresses are in hexadecimal

↑ Is not reset with a Stop-Mode Recovery, except Bit 0

↑↑ Bit 5 Is not reset with a Stop-Mode Recovery

↑↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery

↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery

↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery

Expanded Reg. Bank D/Group 0

			D7	D6	D5	D4	D3	D2	D1	D0
	(D) 0C	LVD	U	U	U	U	U	U	U	0
*	(D) 0B	HI8	0	0	0	0	0	0	0	0
*	(D) 0A	LO8	0	0	0	0	0	0	0	0
*	(D) 09	HI16	0	0	0	0	0	0	0	0
*	(D) 08	LO16	0	0	0	0	0	0	0	0
*	(D) 07	TC16H	0	0	0	0	0	0	0	0
*	(D) 06	TC16L	0	0	0	0	0	0	0	0
*	(D) 05	TC8H	0	0	0	0	0	0	0	0
*	(D) 04	TC8L	0	0	0	0	0	0	0	0
↑↑	(D) 03	CTR3	0	0	0	1	1	1	1	1
↑↑↑	(D) 02	CTR2	0	0	0	0	0	0	0	0
↑↑↑↑	(D) 01	CTR1	0	0	0	0	0	0	0	0
↑↑↑↑↑	(D) 00	CTR0	0	0	0	0	0	0	0	0

Figure 15. Expanded Register File Architecture

Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

Table 12. CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-------0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:
*Indicates the value upon Power-On Reset.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the termi- nal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.

Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

This bit defines the frequency of the input signal to T8.

T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.
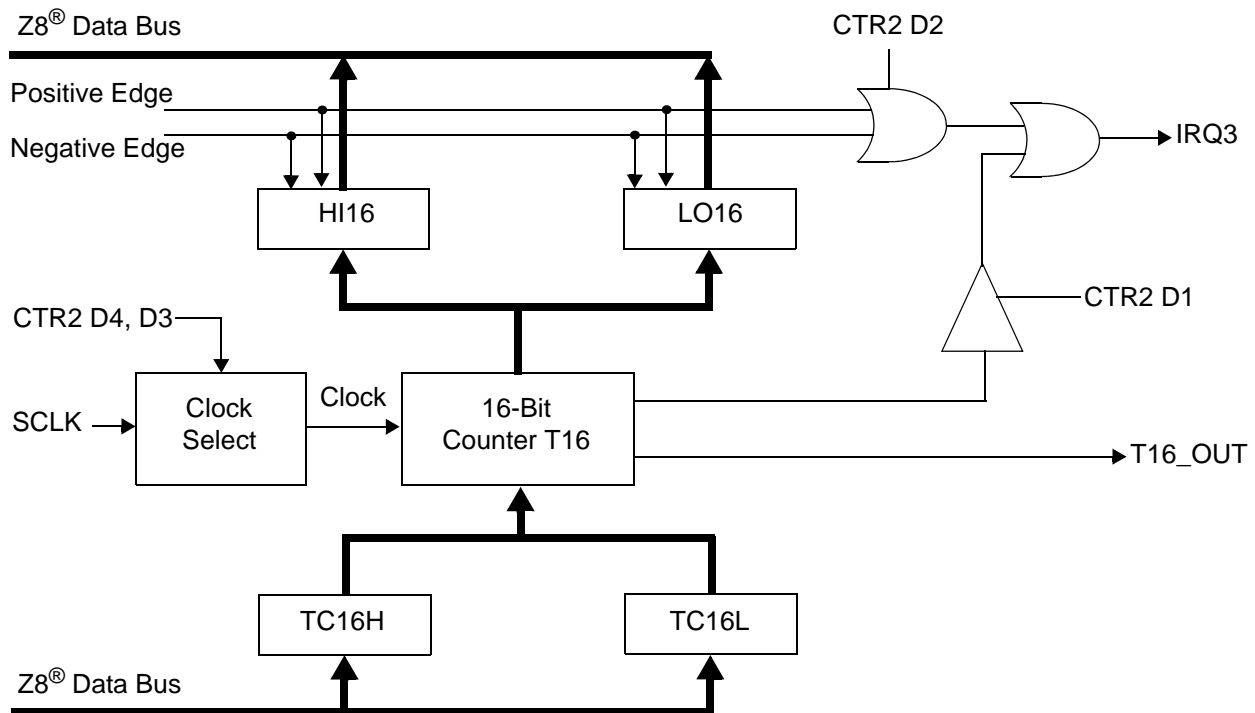
Figure 25. 16-Bit Counter/Timer Circuits

▶ **Note:** Global interrupts override this function as described in "Interrupts" on page 48.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

⚠ **Caution:**   Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFEH. Transition from 0 to FFFFH is not a timeout condition.
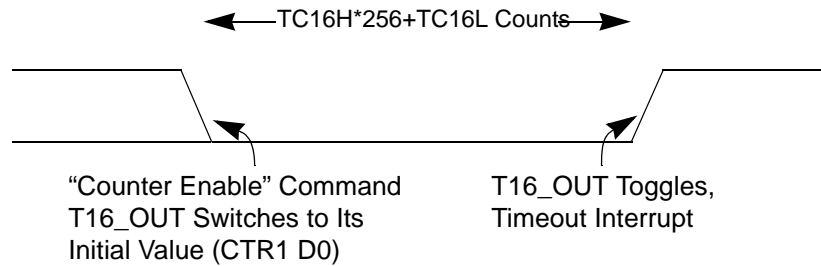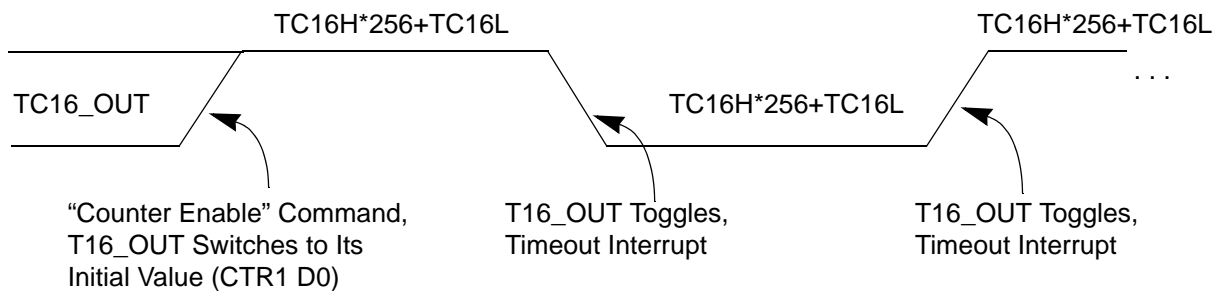

Figure 26. T16_OUT in Single-Pass Mode

Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

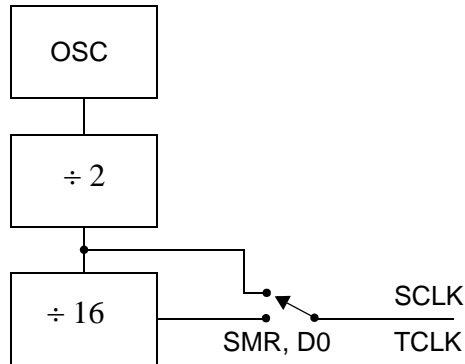This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 19).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 18 lists and briefly describes the fields for this register.

Table 18. SMR2(F)0DH: Stop Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0[†]	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000[†]	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Port pins configured as outputs are ignored as a SMR recovery source.
[†] Indicates the value upon Power-On Reset

Table 19. Stop Mode Recovery Source

SMR:432			Operation
D4	**D3**	**D2**	**Description of Action**
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

> **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 59 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

> **Note:** It is recommended that this bit be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

Table 20. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.
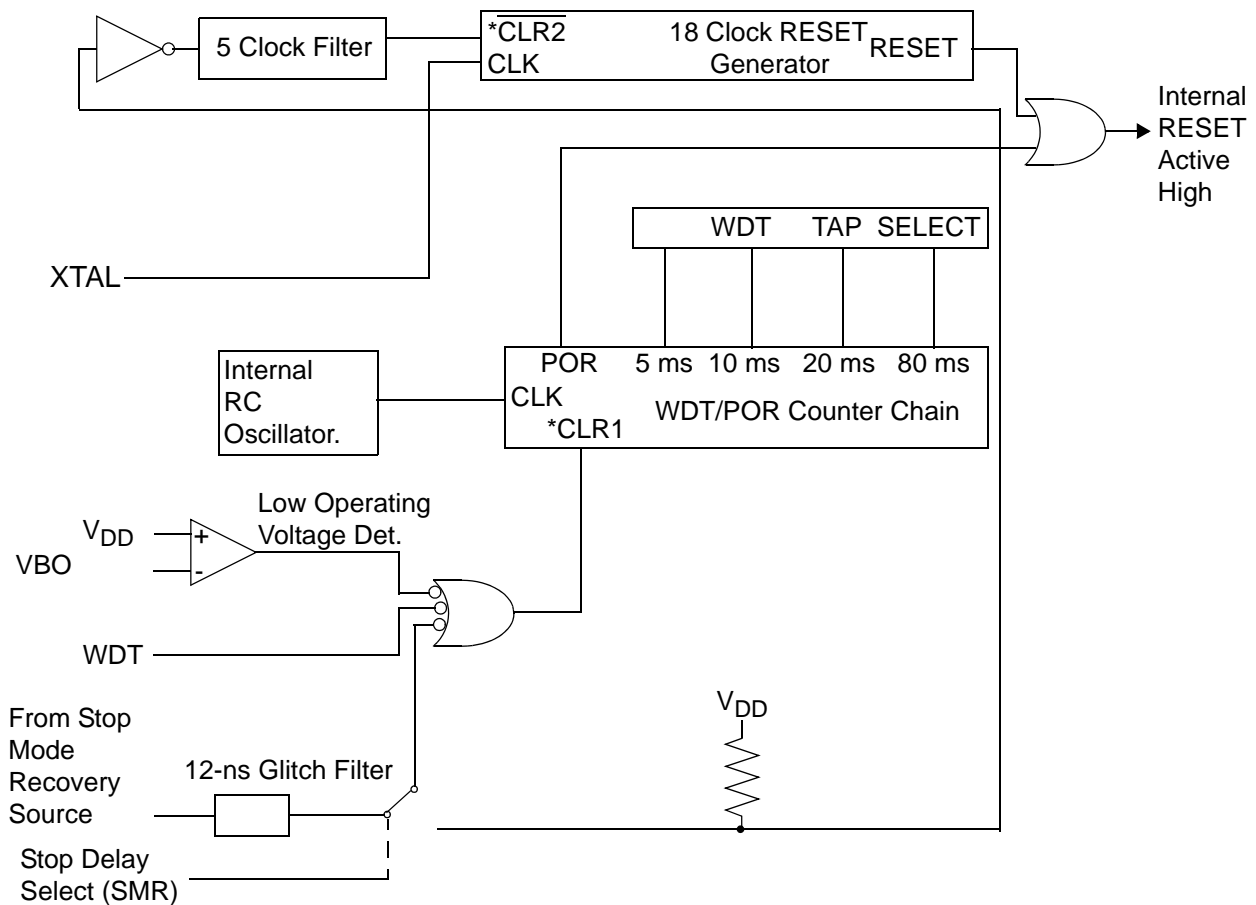
* CLR1 and $\overline{CLR2}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

Figure 38. Resets and WDT

Low-Voltage Detection Register—LVD(D)0Ch

▶ **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	-----2--	R	1	HVD flag set
			0*	HVD flag reset
	------1-	R	1	LVD flag set
			0*	LVD flag reset
	-------0	R/W	1	Enable VD
			0*	Disable VD

*Default after POR

▶ **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register $0CH$ at the expanded register bank $0Dh$) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.
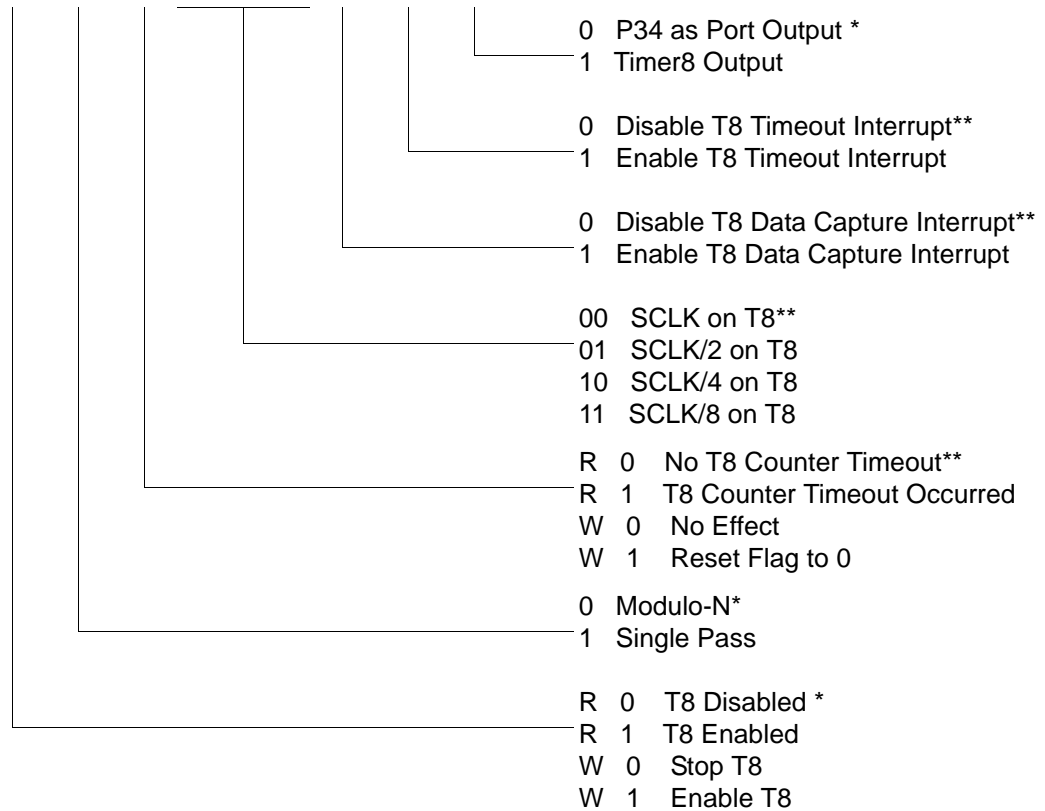
▶ **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

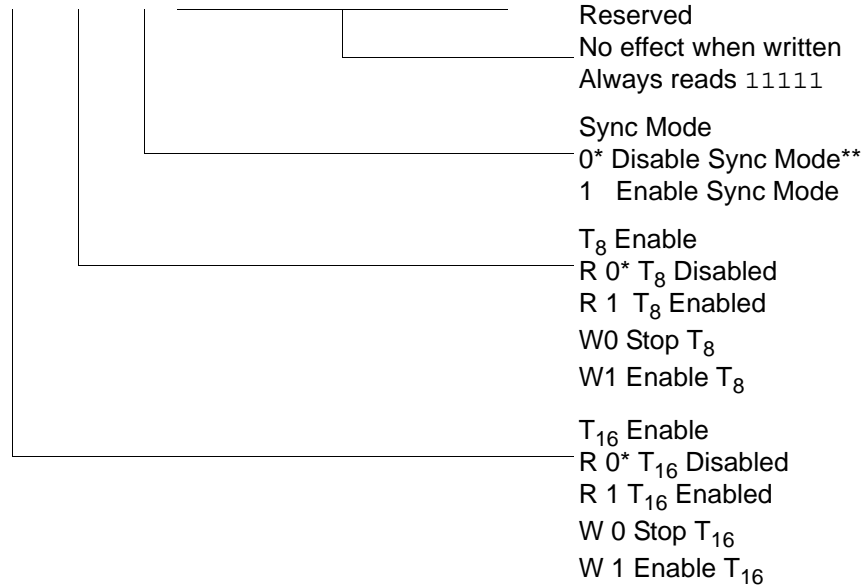| D7	D6	D5	D4	D3	D2	D1	D0

```
                                    0  P34 as Port Output *
                                    1  Timer8 Output

                                    0  Disable T8 Timeout Interrupt**
                                    1  Enable T8 Timeout Interrupt

                                    0  Disable T8 Data Capture Interrupt**
                                    1  Enable T8 Data Capture Interrupt

                                    00  SCLK on T8**
                                    01  SCLK/2 on T8
                                    10  SCLK/4 on T8
                                    11  SCLK/8 on T8

                                    R  0   No T8 Counter Timeout**
                                    R  1   T8 Counter Timeout Occurred
                                    W  0   No Effect
                                    W  1   Reset Flag to 0

                                    0  Modulo-N*
                                    1  Single Pass

                                    R  0   T8 Disabled *
                                    R  1   T8 Enabled
                                    W  0   Stop T8
                                    W  1   Enable T8
```

* Default setting after reset
**Default setting after reset. Not reset with Stop Mode recovery.

Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)

CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0

Reserved
No effect when written
Always reads `11111`

Sync Mode
0* Disable Sync Mode**
1   Enable Sync Mode

T_8 Enable
R 0* T_8 Disabled
R 1 T_8 Enabled
W0 Stop T_8
W1 Enable T_8

T_{16} Enable
R 0* T_{16} Disabled
R 1 T_{16} Enabled
W 0 Stop T_{16}
W 1 Enable T_{16}

* Default setting after reset.
** Default setting after reset. Not reset with Stop
Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

▶ **Note:** If Sync Mode is enabled, the first pulse of T8 carrier is always
synchronized with T16 (demodulated signal). It can always
provide a full carrier pulse.
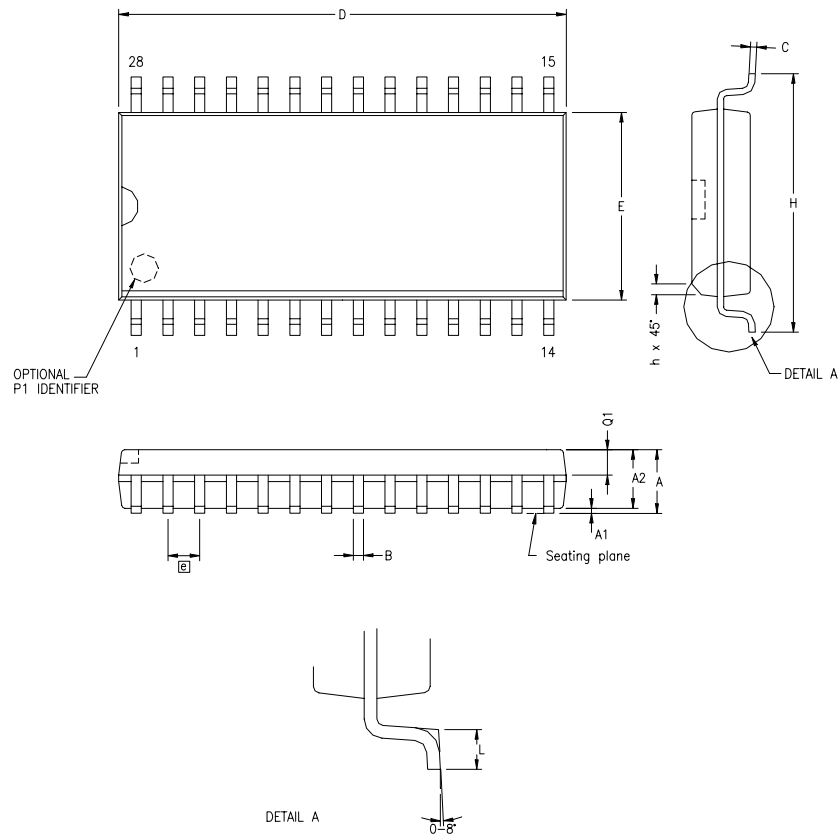
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 63. 28-Pin SOIC Package Diagram

Ordering Information

32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4832C	48-pin SSOP 32K OTP	ZGP323LSS2832C	28-pin SOIC 32K OTP
ZGP323LSP4032C	40-pin PDIP 32K OTP	ZGP323LSH2032C	20-pin SSOP 32K OTP
ZGP323LSH2832C	28-pin SSOP 32K OTP	ZGP323LSP2032C	20-pin PDIP 32K OTP
ZGP323LSP2832C	28-pin PDIP 32K OTP	ZGP323LSS2032C	20-pin SOIC 32K OTP
ZGP323LSK2032E	20-pin CDIP 32K OTP	ZGP323LSK4032E	40-pin CDIP 32K OTP
		ZGP323LSK2832E	28-pin CDIP 32K OTP

32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4832C	48-pin SSOP 32K OTP	ZGP323LES2832C	28-pin SOIC 32K OTP
ZGP323LEP4032C	40-pin PDIP 32K OTP	ZGP323LEH2032C	20-pin SSOP 32K OTP
ZGP323LEH2832C	28-pin SSOP 32K OTP	ZGP323LEP2032C	20-pin PDIP 32K OTP
ZGP323LEP2832C	28-pin PDIP 32K OTP	ZGP323LES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4832C	48-pin SSOP 32K OTP	ZGP323LAS2832C	28-pin SOIC 32K OTP
ZGP323LAP4032C	40-pin PDIP 32K OTP	ZGP323LAH2032C	20-pin SSOP 32K OTP
ZGP323LAH2832C	28-pin SSOP 32K OTP	ZGP323LAP2032C	20-pin PDIP 32K OTP
ZGP323LAP2832C	28-pin PDIP 32K OTP	ZGP323LAS2032C	20-pin SOIC 32K OTP

Note: Replace C with G for Lead-Free Packaging

8KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4808C	48-pin SSOP 8K OTP	ZGP323LSS2808C	28-pin SOIC 8K OTP
ZGP323LSP4008C	40-pin PDIP 8K OTP	ZGP323LSH2008C	20-pin SSOP 8K OTP
ZGP323LSH2808C	28-pin SSOP 8K OTP	ZGP323LSP2008C	20-pin PDIP 8K OTP
ZGP323LSP2808C	28-pin PDIP 8K OTP	ZGP323LSS2008C	20-pin SOIC 8K OTP

8KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4808C	48-pin SSOP 8K OTP	ZGP323LES2808C	28-pin SOIC 8K OTP
ZGP323LEP4008C	40-pin PDIP 8K OTP	ZGP323LEH2008C	20-pin SSOP 8K OTP
ZGP323LEH2808C	28-pin SSOP 8K OTP	ZGP323LEP2008C	20-pin PDIP 8K OTP
ZGP323LEP2808C	28-pin PDIP 8K OTP	ZGP323LES2008C	20-pin SOIC 8K OTP

8KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4808C	48-pin SSOP 8K OTP	ZGP323LAS2808C	28-pin SOIC 8K OTP
ZGP323LAP4008C	40-pin PDIP 8K OTP	ZGP323LAH2008C	20-pin SSOP 8K OTP
ZGP323LAH2808C	28-pin SSOP 8K OTP	ZGP323LAP2008C	20-pin PDIP 8K OTP
ZGP323LAP2808C	28-pin PDIP 8K OTP	ZGP323LAS2008C	20-pin SOIC 8K OTP

Note: Replace C with G for Lead-Free Packaging