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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lah4808g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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**ZiLOG Worldwide Headquarters** 532 Race Street

San Jose, CA 95126-3432 Telephone: 408.558.8500 Fax: 408.558.8300 www.zilog.com

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#### Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 3.	20-Pin PDIP/SOIC/SSOP/CDIP*	Pin	Identification
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Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20-P24	Port 2, Bits 0,1,2,3,4	Input/Output

**Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

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#### Table 9. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	25			Cycles	1

Notes:

1. For windowed cerdip package only.

2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

AF = exp[(Ea/k)\*(1/Tuse - 1/TStress)] Where: Ea is the intrinsic activation energy (eV; typ. 0.8) k is Boltzman's constant (8.67 x 10-5 eV/°K) °K = -273.16°C Tuse = Use Temperature in °K TStress = Stress Temperature in °K 3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>



# **Pin Functions**

# XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

# XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

# Port 0 (P07-P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

**Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to be input following an SMR.





#### Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—

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Location of 32	768	Not Accessible
first Byte of		On-Chip
executed		ROW
after RESET	12	Reset Start Address
	11	IRQ5
	10	IRQ5
	9	IRQ4
	8	IRQ4
Interrupt Vector	7	IRQ3
(Lower Byte)	6	IRQ3
	5	► IRQ2
Interrupt Vector	4	┍ IRQ2
(Upper Byte)	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0

Figure 14. Program Memory Map (32K OTP)

# **Expanded Register File**

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The  $Z8^{\ensuremath{\mathbb{R}}}$  register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTRL0
LD	1, #xx	;	load CTRL1
LD	R1, 2	;	$CTRL2 \rightarrow CTRL1$
LD	RP. #0Dh	;	Select ERF D
for access to bank D	,	,	
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 $\rightarrow$ register 71h			
LD	R1, 2		
; CTRL2 $\rightarrow$ register 71h			

# **Register File**

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The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.









\* RP = 00: Selects Register Bank 0, Working Register Group 0

Figure 17. Register Pointer—Detail

# Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

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#### Table 12. CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	<b>Bit Position</b>		Value	Description
Counter_INT_Mask	1-	R/W	0 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	0	R/W	0* 1	P34 as Port Output T8 Output on P34

#### Note:

\*Indicates the value upon Power-On Reset.

# T8 Enable

This field enables T8 when set (written) to 1.

# Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

# Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

# **T8 Clock**

This bit defines the frequency of the input signal to T8.



# Capture\_INT\_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

# Counter\_INT\_Mask

Set this bit to allow an interrupt when T8 has a timeout.

# P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

# T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 13 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Mode	7	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/	-6	R/W		Transmit Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/	54	R/W		Transmit Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

#### Table 13. CTR1(0D)01H T8 and T16 Common Functions

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Field	Bit Position		Value	Description
Transmit_Submode/	32	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

#### Table 13. CTR1(0D)01H T8 and T16 Common Functions (Continued)

#### Note:

\*Default at Power-On Reset.

\*\*Default at Power-On Reset.Not reset with Stop Mode recovery.

# Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

# P36\_Out/Demodulator\_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.



Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T <sub>IN</sub>	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	Т8	8,9	Internal
IRQ5	LVD	10,11	Internal

#### Table 16. Interrupt Types, Sources, and Vectors

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z8 GP<sup>TM</sup> OTP MCU Family interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 17.

IRQ		Interrupt Edge			
D7	D6	IRQ2 (P31)	IRQ0 (P32)		
0	0	F	F		
0	1	F	R		
1	0	R	F		
1	1	R/F	R/F		
<b>Note:</b> F = Falling Edge; R = Rising Edge					

#### Table 17. IRQ Register



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line
e

# Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

# PCON(FH)00H



\* Default setting after reset

# Figure 32. Port Configuration Register (PCON) (Write Only)

# Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

# Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.





# SMR(0F)0BH



\* Default after Power On Reset or Watch-Dog Reset

- \* \* Set after STOP Mode Recovery
- \* \* \* At the XOR gate input

\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

# Figure 33. STOP Mode Recovery Register

# SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



# WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

# **EPROM Selectable Options**

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

#### Table 21. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

# Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V<sub>DD</sub> is at the required level for correct operation of the device. Reset is globally driven when V<sub>DD</sub> falls below V<sub>BO</sub>. A small drop in V<sub>DD</sub> causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V<sub>DD</sub> is allowed to stay above V<sub>RAM</sub>, the RAM content is preserved. When the power level is returned to above V<sub>BO</sub>, the device performs a POR and functions normally.



# R247 P3M(F7H)



\* Default setting after reset. Not reset with Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)



# R248 P01M(F8H)



\* Default setting after reset; only P00, P01 and P07 are available in 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)









Figure 62. 28-Pin CDIP Package

# Z8 GP<sup>TM</sup> OTP MCU Family Product Specification





Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 64. 28-Pin PDIP Package Diagram



#### 16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4816C	48-pin SSOP 16K OTP	ZGP323LSS2816C	28-pin SOIC 16K OTP
ZGP323LSP4016C	40-pin PDIP 16K OTP	ZGP323LSH2016C	20-pin SSOP 16K OTP
ZGP323LSH2816C	28-pin SSOP 16K OTP	ZGP323LSP2016C	20-pin PDIP 16K OTP
ZGP323LSP2816C	28-pin PDIP 16K OTP	ZGP323LSS2016C	20-pin SOIC 16K OTP

# 16KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4816C	48-pin SSOP 16K OTP	ZGP323LES2816C	28-pin SOIC 16K OTP
ZGP323LEP4016C	40-pin PDIP 16K OTP	ZGP323LES2016C	20-pin SOIC 16K OTP
ZGP323LEH2816C	28-pin SSOP 16K OTP	ZGP323LEH2016C	20-pin SSOP 16K OTP
ZGP323LEP2816C	28-pin PDIP 16K OTP	ZGP323LEP2016C	20-pin PDIP 16K OTP

# 16KB Automotive Temperature: -40° to +125°C

Dort Number	Description	Dort Number	Description	
Part Number	Description	Part Number	Description	
ZGP323LAH4816C	48-pin SSOP 16K OTP	ZGP323LAS2816C	28-pin SOIC 16K OTP	
ZGP323LAP4016C	40-pin PDIP 16K OTP	ZGP323LAH2016C	20-pin SSOP 16K OTP	
ZGP323LAH2816C	28-pin SSOP 16K OTP	ZGP323LAP2016C	20-pin PDIP 16K OTP	
ZGP323LAP2816C	28-pin PDIP 16K OTP	ZGP323LAS2016C	20-pin SOIC 16K OTP	
Note: Replace C with G for Lead-Free Packaging				

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