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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lah4816c

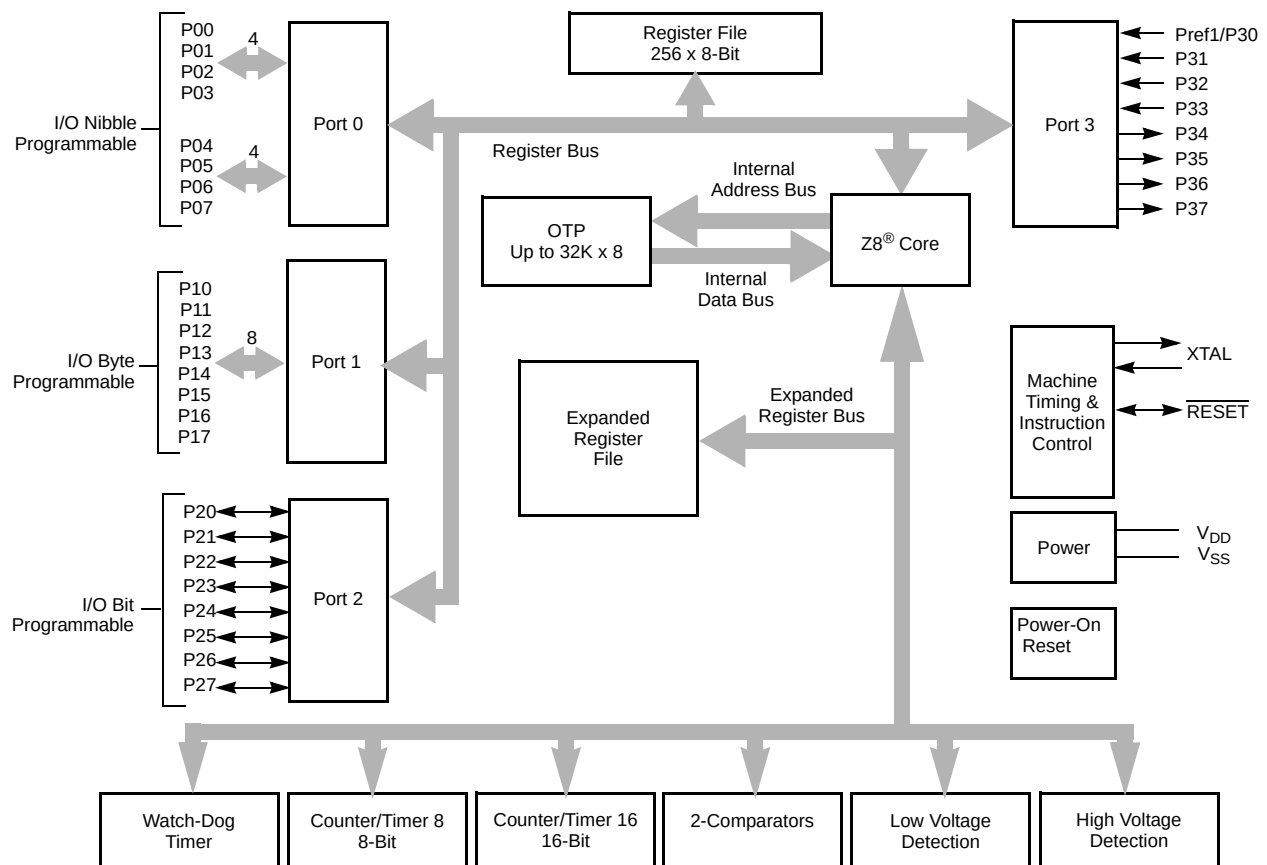


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Table 2. Power Connections

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

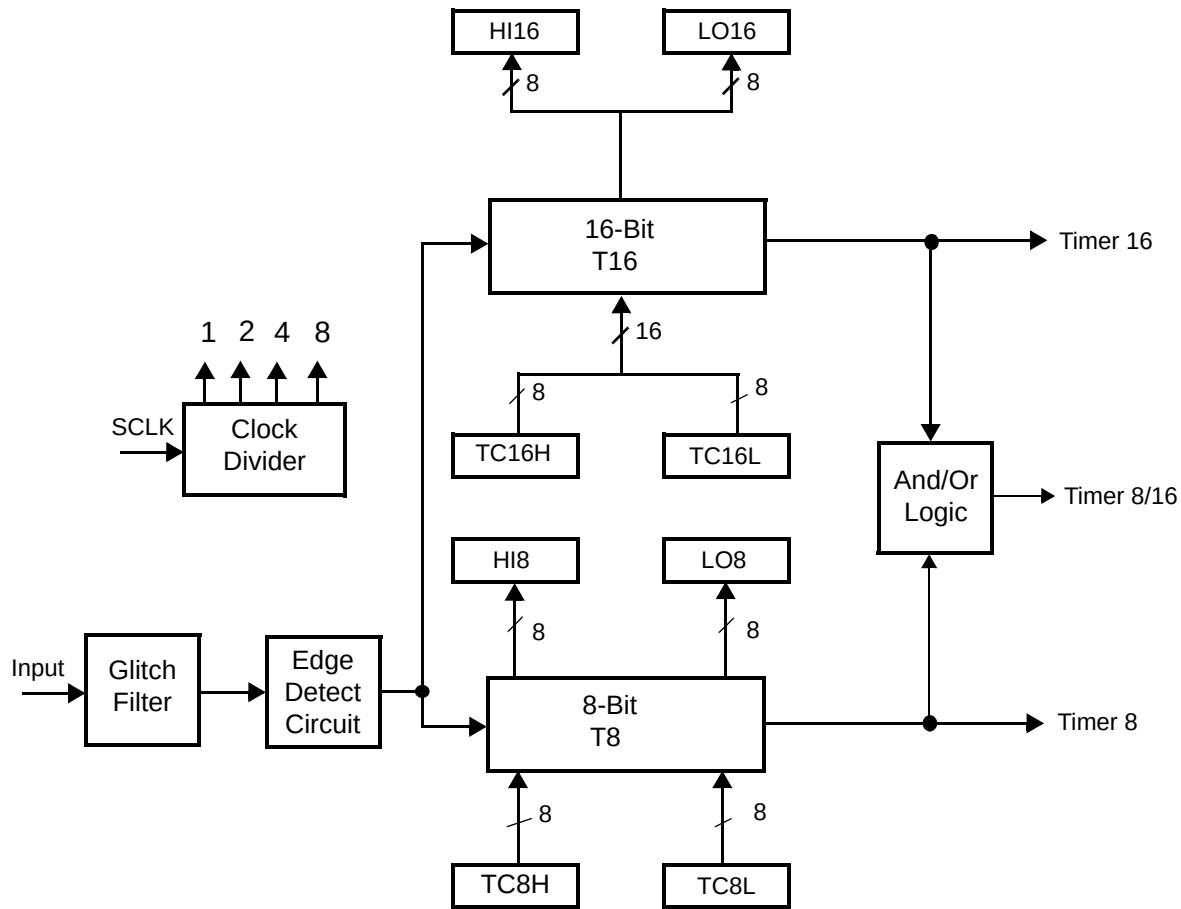


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 5.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZILOG does not recommend nor guarantee these packages for use in production.

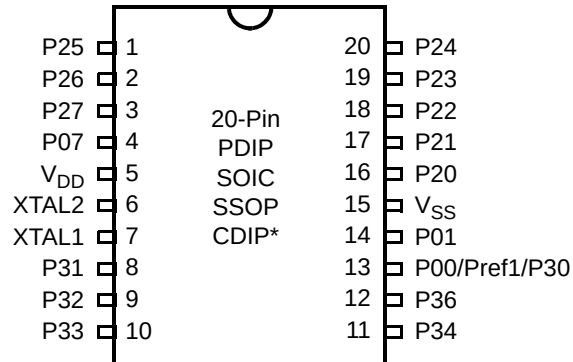


Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Table 8. DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C			Units	Conditions	Notes
			Min	Typ	Max			
I _{CC1}	Standby Current (HALT Mode)	2.0			3	mA	V _{IN} = 0V, V _{CC} at 8.0MHz	1, 2
		3.6			5		Same as above	1, 2
		2.0			2		Clock Divide-by-16 at 8.0MHz	1, 2
		3.6			4		Same as above	1, 2
I _{CC2}	Standby Current (Stop Mode)	2.0			8	μA	V _{IN} = 0 V, V _{CC} WDT is not Running	3
		3.6			10	μA	Same as above	3
		2.0			500	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6			800	μA	Same as above	3
I _{LV}	Standby Current (Low Voltage)				10	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection				2.0	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to the V_{DD} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.

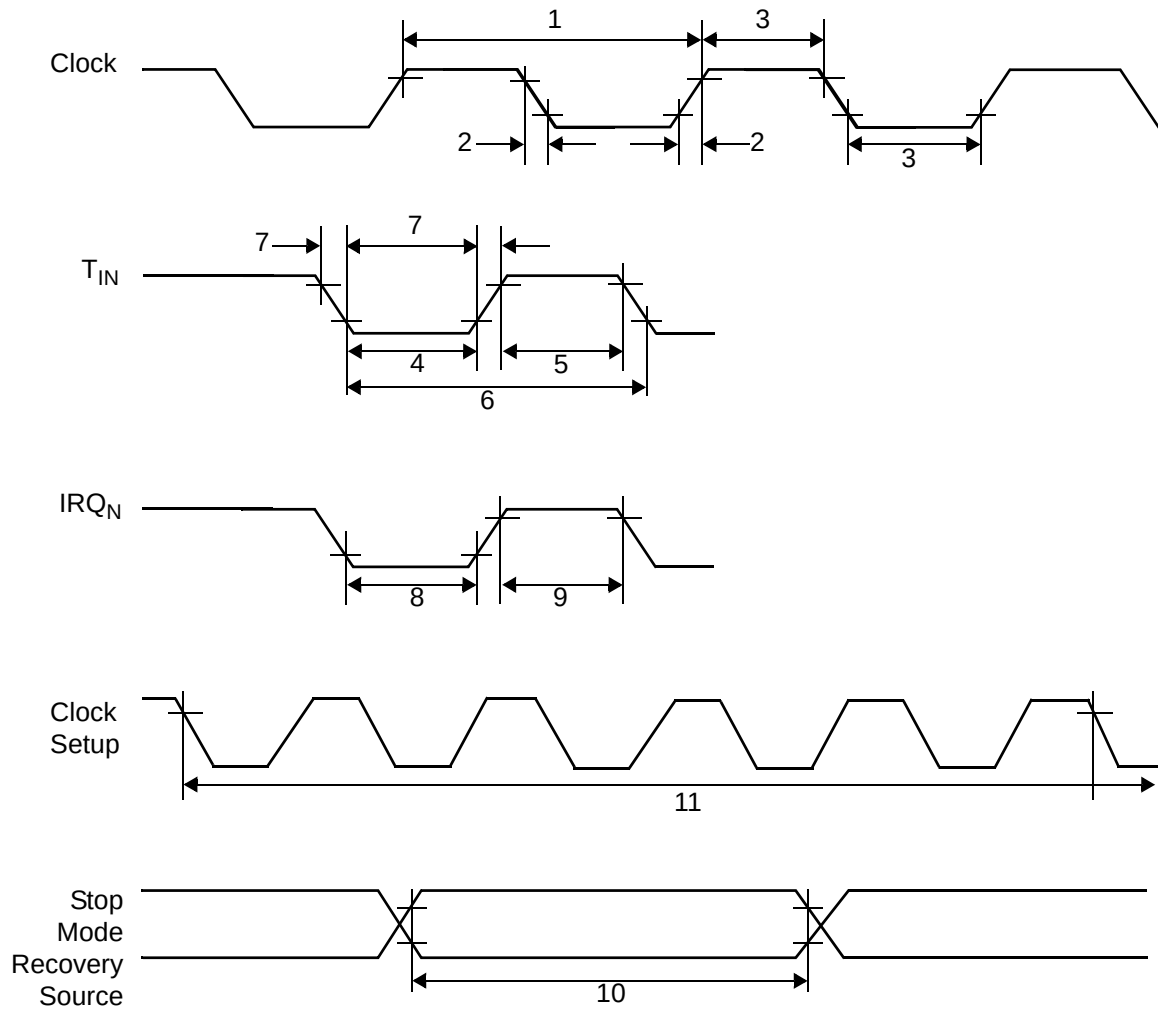


Figure 8. AC Timing Diagram

Table 10. AC Characteristics

				T _A =0°C to +70°C 8.0MHz			Watch-Dog Timer Mode Register (D1, D0)	
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes	
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1	
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms		

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

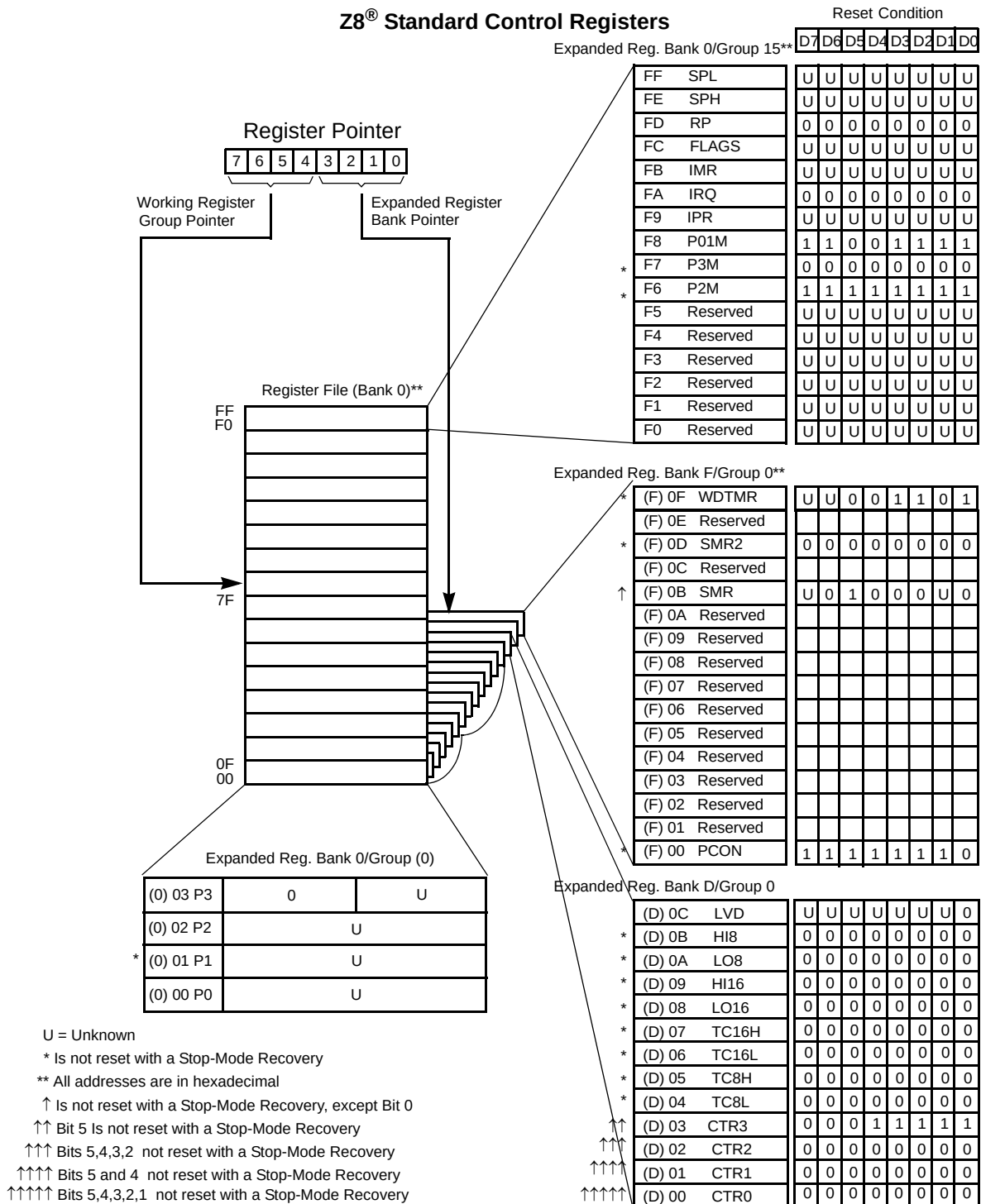


Figure 15. Expanded Register File Architecture

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

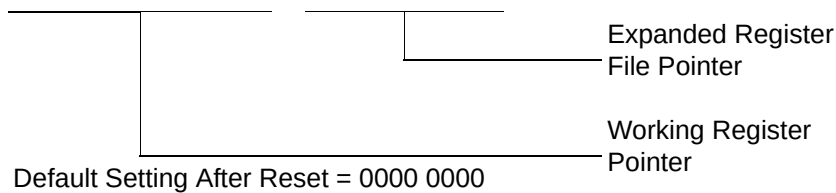


Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 26)

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTRL0

R1 = CTRL1

R2 = CTRL2

R3 = Reserved

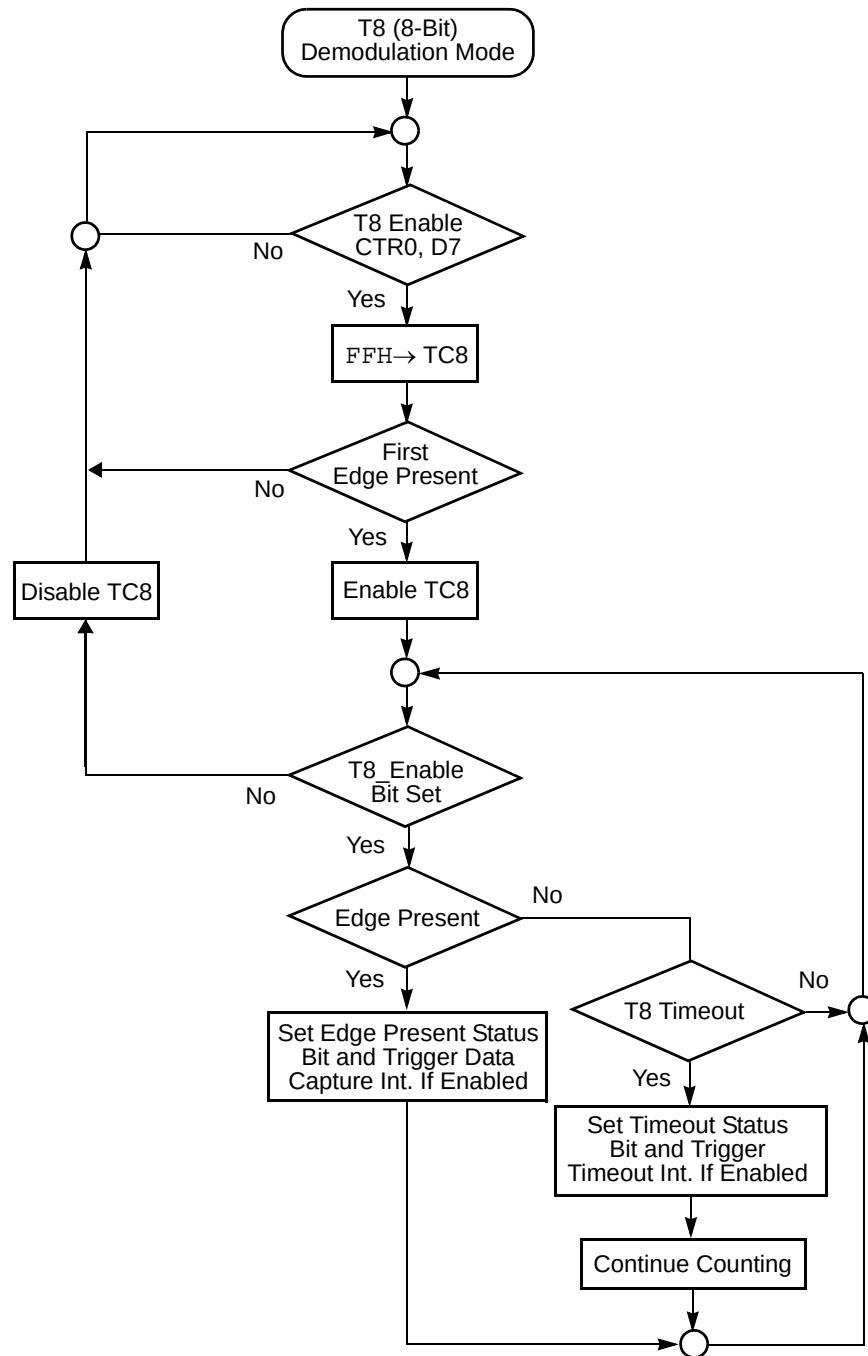


Figure 24. Demodulation Mode Flowchart



Caution:

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE_H. Transition from 0 to FFFF_H is not a timeout condition.

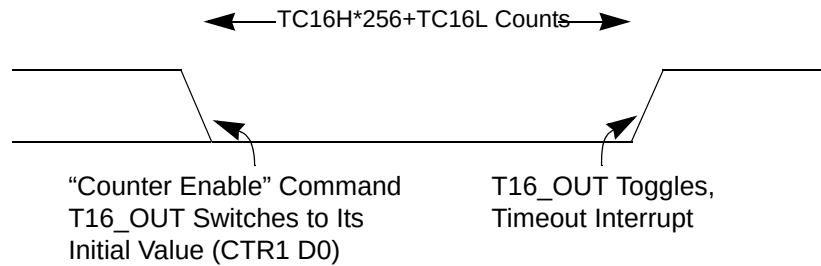


Figure 26. T16_OUT in Single-Pass Mode

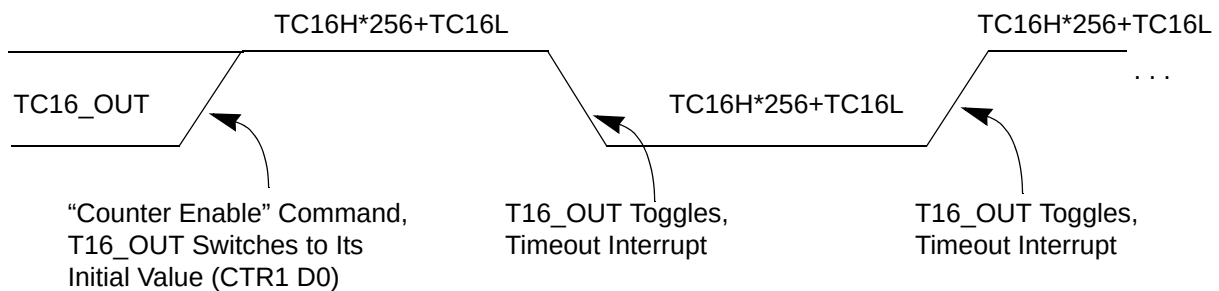


Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FF_H. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF_H and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

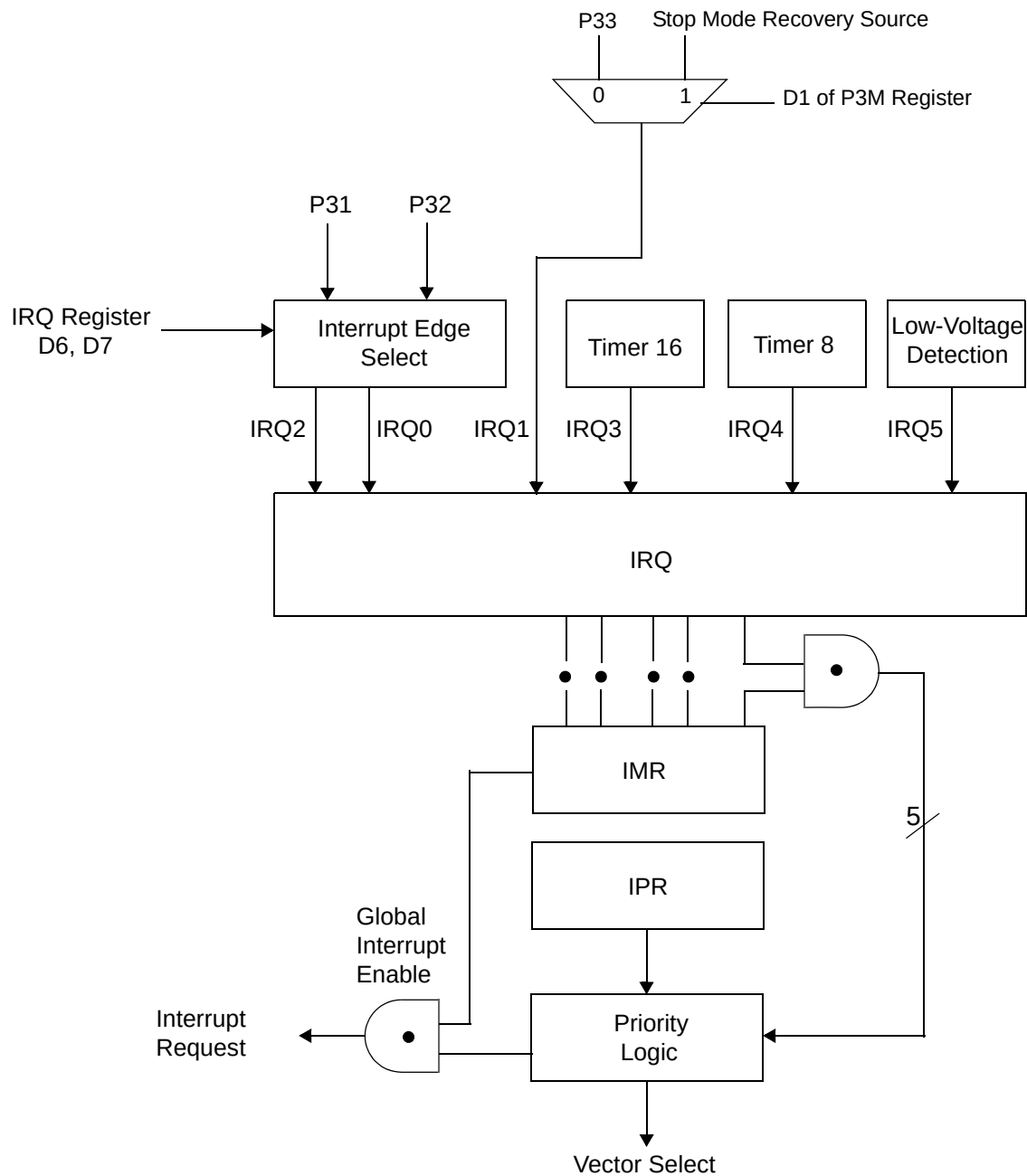


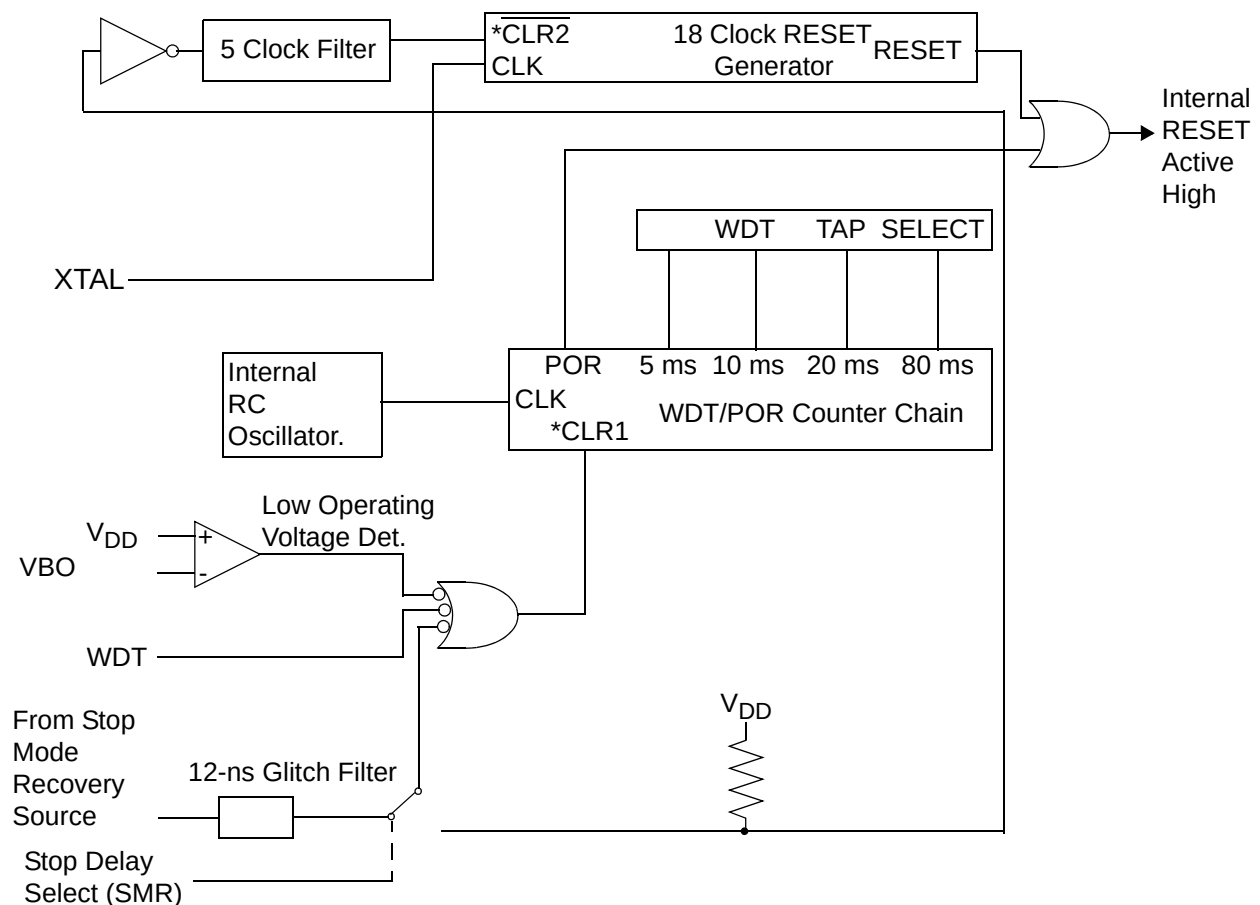
Figure 30. Interrupt Block Diagram

Table 20. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



* CLR1 and CLR2 enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

Figure 38. Resets and WDT

Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position	Description		
LVD	76543---	Reserved No Effect		
	----2--	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD
*Default after POR				

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

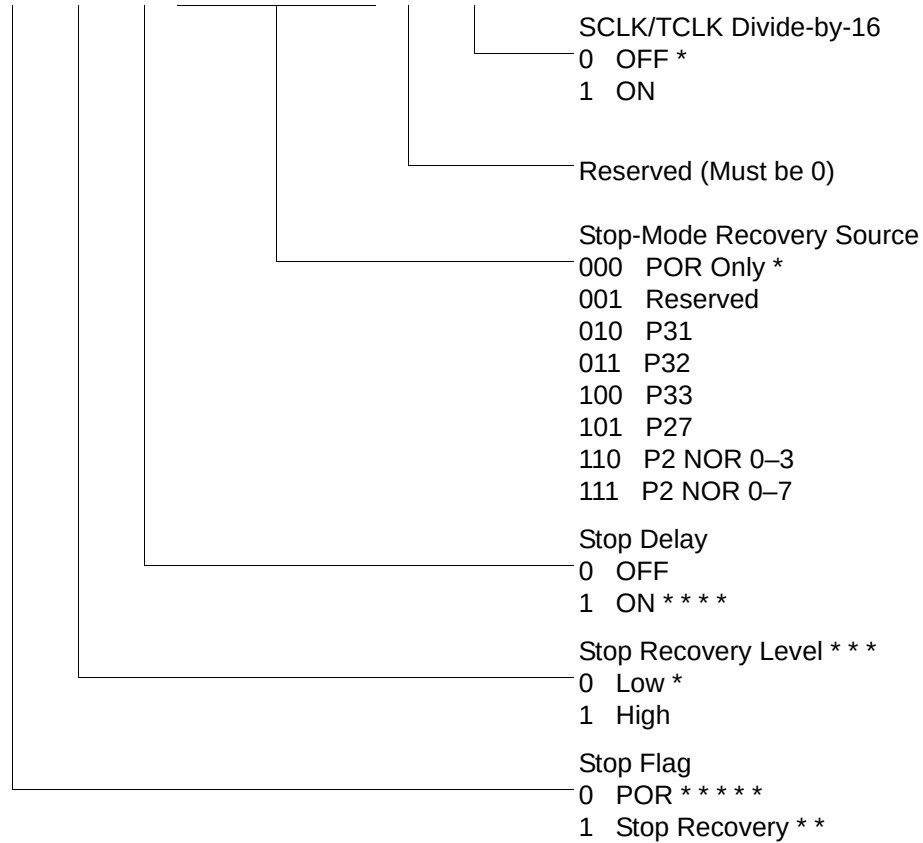
Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD} . The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD} . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after Reset

** Set after STOP Mode Recovery

*** At the XOR gate input

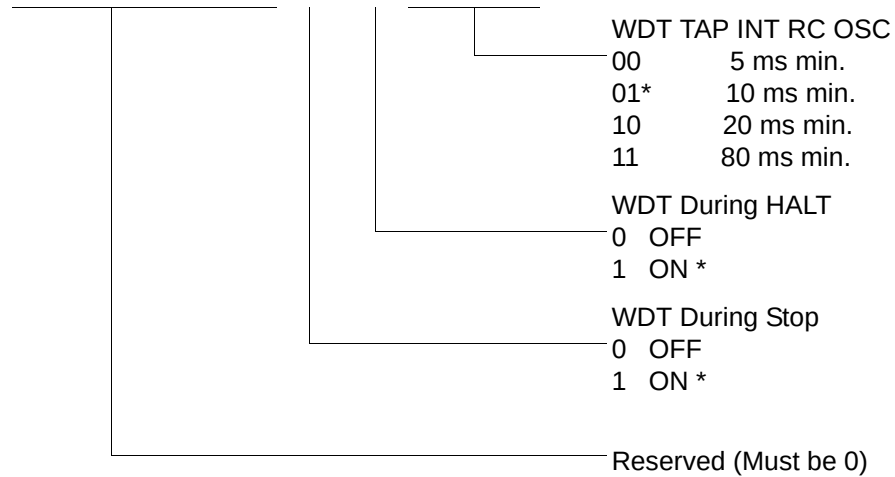
**** Default setting after Reset. Must be 1 if using a crystal or resonator clock source.

***** Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

WDTMR(0F)0FH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



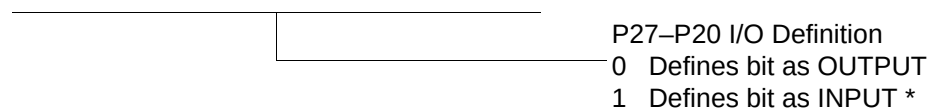
* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)

R252 Flags(FCH)

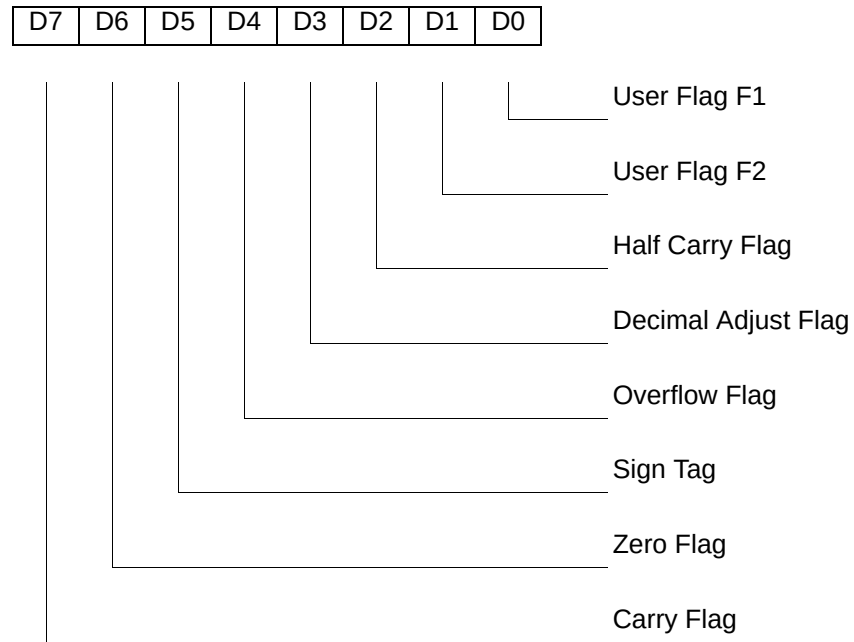
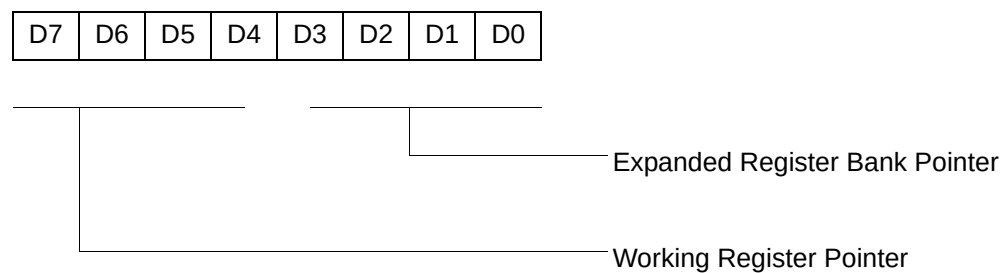


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)

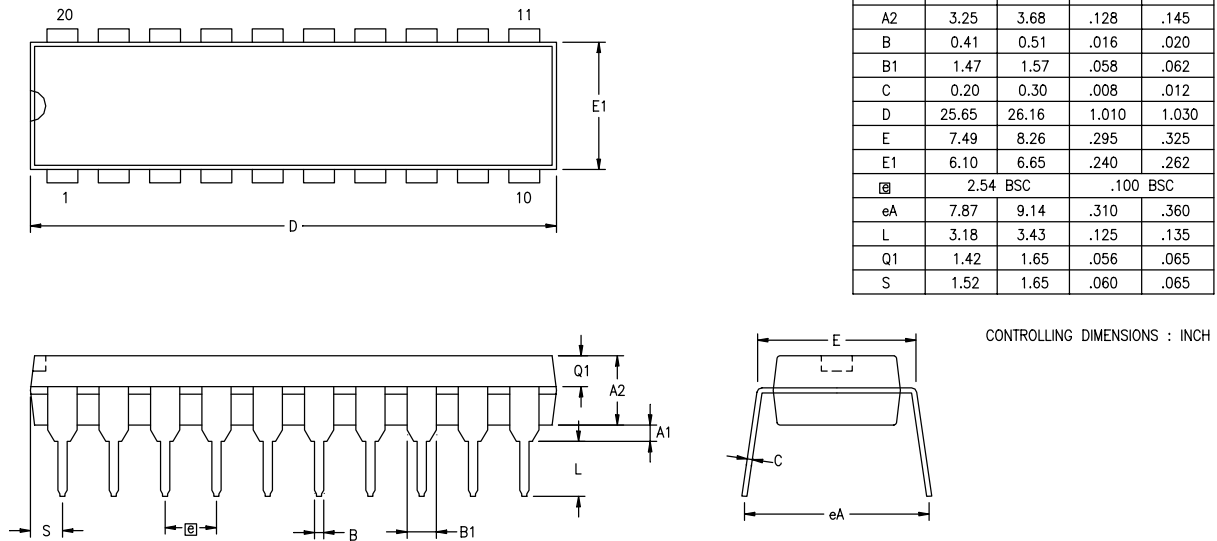


Figure 59. 20-Pin PDIP Package Diagram

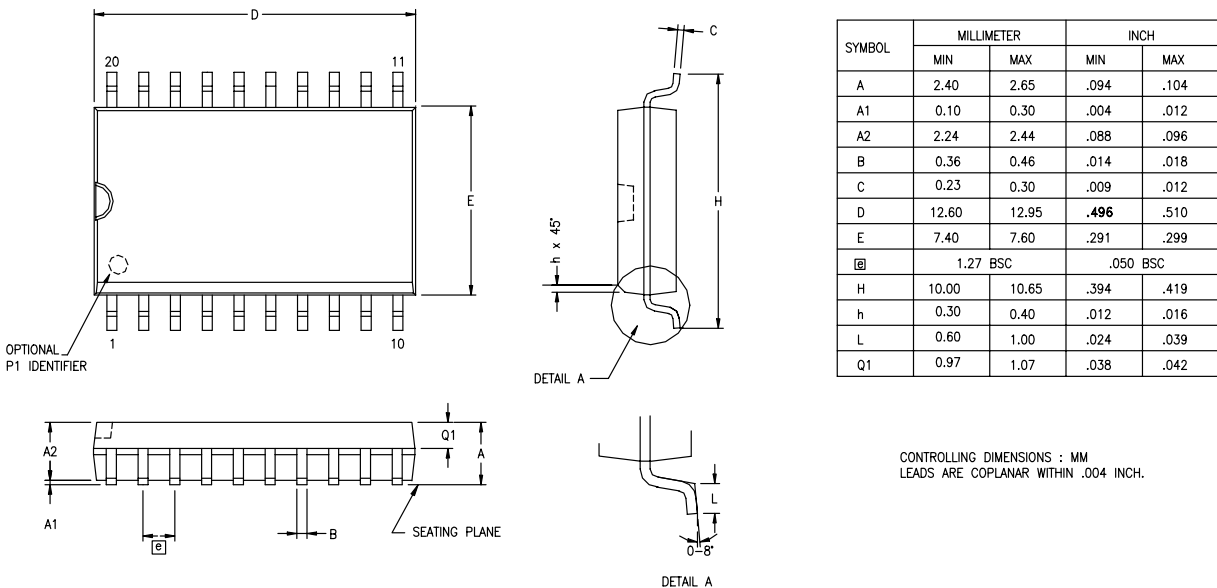


Figure 60. 20-Pin SOIC Package Diagram

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