Zilog - ZGP323LAH4816G Datasheet





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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K × 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lah4816g

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Figure 35. Stop Mode Recovery Source	57
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)	. 59
Figure 37. Watch-Dog Timer Mode Register (Write Only)	60
Figure 38. Resets and WDT	61
Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted	d) 64
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write) .	65
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)	. 67
Figure 42. T8/T16 Control Register (0D)03H: Read/Write	
(Except Where Noted)	68
Figure 43. Voltage Detection Register	69
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)	70
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)	71
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only	/) 72
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)	73
Figure 48. Port 2 Mode Register (F6H: Write Only)	73
Figure 49. Port 3 Mode Register (F7H: Write Only)	74
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)	75
Figure 51. Interrupt Priority Register (F9H: Write Only)	76
Figure 52. Interrupt Request Register (FAH: Read/Write)	77
Figure 53. Interrupt Mask Register (FBH: Read/Write)	77
Figure 54. Flag Register (FCH: Read/Write)	78
Figure 55. Register Pointer (FDH: Read/Write)	78
Figure 56. Stack Pointer High (FEH: Read/Write)	79
Figure 57. Stack Pointer Low (FFH: Read/Write)	79
Figure 58. 20-Pin CDIP Package	80
Figure 59. 20-Pin PDIP Package Diagram	81
Figure 60. 20-Pin SOIC Package Diagram	81
Figure 61. 20-Pin SSOP Package Diagram	82
Figure 62. 28-Pin CDIP Package	83
Figure 63. 28-Pin SOIC Package Diagram	84
Figure 64. 28-Pin PDIP Package Diagram	85
Figure 65. 28-Pin SSOP Package Diagram	86
Figure 66. 40-Pin CDIP Package	87
Figure 67. 40-Pin PDIP Package Diagram	87
Figure 68. 48-Pin SSOP Package Design	88



- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR
- **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K Ω ±50% at V_{CC}=3 V and 450 K Ω ±50% at $V_{CC}=2$ V.

General Description

The Z8 GPTM OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG[®]'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z8 GPTM OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to registermapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8[®] offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of userselectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: All signals with an overline, "", are active Low. For example, B/\overline{W} , in which WORD is active Low, and \overline{B}/W , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.



Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Port 0 (P07-P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

Notes: Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to be input following an SMR.



CTR1(0D)01H" on page 33). Other edge detect and IRQ modes are described in Table 11.

Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Table 11. Port 3 Pin Function Summary

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Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.







Figure 13. Port 3 Counter/Timer Output Configuration

Z8 GP[™] OTP MCU Family Product Specification



Z8 [®] Standard Control Registers				onc	litio	n	
Expanded Reg. Bank 0/Group 15*	* D7 D6	D5	D4	D3	D2	D1	D0
		1					
			0	0	0	0	0
		0	0	0	0	0	0
Register Pointer /	0 0	0	0	0	0	0	0
7 6 5 4 3 2 1 0	00	0	0	0	0	0	0
	00	U	U	U	U	U	U
Working Register Expanded Register	0 0	0	0	0	0	0	0
Group Pointer Bank Pointer F9 IPK		U	U	U	U	U	U
	1 1	0	0	1	1	1	1
* F7 P3M	0 0	0	0	0	0	0	0
* F6 P2M	1 1	1	1	1	1	1	1
F5 Reserved	UU	U	U	U	U	U	U
F4 Reserved	UU	U	U	U	U	U	U
F3 Reserved	UU	U	U	U	U	U	U
Register File (Bank 0)** / F2 Reserved	UU	U	U	U	U	U	U
FF F1 Reserved	UU	U	U	U	U	U	U
F0 Reserved	υυ	U	U	U	U	U	U
Expanded Reg. Bank F/Group 0**							
L (F) OF WDTMR		0	0	1	1	0	1
(F) OF Reserved	0 0	0	0	-	-	0	-
* (F) 0D_SMR2	0.0	0	0	0	0	0	0
(F) OC Reserved	00	-	0	-	•	•	0
		4	0	0	0		0
7F (F) 0A Reserved	0 0	-	0	0	0	0	0
		-		_	_	-	_
				_		_	
				_		_	
				-		_	
				-		_	
				-		_	
				_	-	-	_
				_	-	-	_
				_	-	-	_
			4	-	4	-	~
Expanded Reg. Bank 0/Group (0)	1 1		ſ	1	1	1	0
(0) 03 P3 0 U Hxpanded\Reg. Bank D/Group 0							_
(0) 02 P2 U (D) 0C LVD		U	U	U	U	U	0
* (0) 01 P1 U V * (D) 04 L 08	0 0	0	0	0	0	0	0
(0) 01 1 1 0 (D) 02 100 (D) 02 116	0 0	0	0	0	0	0	0
(0) 00 P0 U * (D) 08 LO16	0 0	0	0	0	0	0	0
U = Unknown	0 0	0	0	0	0	0	0
* Is not reset with a Stop-Mode Recovery	0 0	0	0	0	0	0	0
** All addresses are in hexadecimal	0 0	0	0	0	0	0	0
↑ Is not reset with a Stop-Mode Recovery, except Bit 0	0 0	0	0	0	0	0	0
↑↑ Bit 5 Is not reset with a Stop-Mode Recovery	0 0	0	1	1	1	1	1
↑↑↑ Bits 5.4.3.2 not reset with a Stop-Mode Recovery	0 0	0	0	0	0	0	0
↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery	0 0	0	0	0	0	0	0
1111 Dia 5 4 2 2 4 not react with a Stan Made Decouvery	0 0	0	0	0	0	0	0

Figure 15. Expanded Register File Architecture

27

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A $_{0\rm H}$ in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.





Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 26)

R253 RP = 00h R0 = Port 0 R1 = Port 1 R2 = Port 2 R3 = Port 3

But if:

R253 RP = 0Dh R0 = CTRL0 R1 = CTRL1 R2 = CTRL2R3 = Reserved



Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 13 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Mode	7	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/	-6	R/W		Transmit Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/	54	R/W		Transmit Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

Table 13. CTR1(0D)01H T8 and T16 Common Functions

34

Field	Bit Position		Value	Description
Transmit_Submode/	32	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Table 13. CTR1(0D)01H T8 and T16 Common Functions (Continued)

Note:

*Default at Power-On Reset.

**Default at Power-On Reset.Not reset with Stop Mode recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.



When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Ca

Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put



T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



Figure 25. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in "Interrupts" on page 48.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.





Figure 30. Interrupt Block Diagram





SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

- * * Set after STOP Mode Recovery
- * * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

Table 21. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.



LVD(0D)0CH



* Default

Figure 43. Voltage Detection Register

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



R247 P3M(F7H)



* Default setting after reset. Not reset with Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)



R250 IRQ(FAH)





Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset

* * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



Package Information

Package information for all versions of Z8 GPTM OTP MCU Family are depicted in Figures 58 through Figure 68.







Figure 58. 20-Pin CDIP Package

Z8 GP[™] OTP MCU Family Product Specification



T8 and T16 common control functions 65 T8/T16 control 68 TC16H(D)07h 30 TC16L(D)06h 31 TC8 control 64 TC8H(D)05h 31 TC8L(D)04h 31 voltage detection 69 watch-dog timer 73 register description Counter/Timer2 LS-Byte Hold 31 Counter/Timer2 MS-Byte Hold 30 Counter/Timer8 Control 31 Counter/Timer8 High Hold 31 Counter/Timer8 Low Hold 31 CTR2 Counter/Timer 16 Control 35 CTR3 T8/T16 Control 37 Stop Mode Recovery2 38 T16 Capture LO 30 T8 and T16 Common functions 33 T8_Capture_HI 30 T8 Capture LO 30 register file 28 expanded 24 register pointer 27 detail 29 reset pin function 23 resets and WDT 61

S

SCLK circuit 56 single-pass mode T16_OUT 45 T8_OUT 41 stack 29 standard test conditions 10 standby modes 1 stop instruction, counter/timer 52 stop mode recovery 2 register 59 source 57 stop mode recovery 2 59 stop mode recovery register 55

Т

T16 transmit mode 44 T16_Capture_HI 30 T8 transmit mode 38 T8_Capture_HI 30 test conditions, standard 10 test load diagram 10 timing diagram, AC 14 transmit mode flowchart 39

V

VCC 5 voltage brown-out/standby 62 detection and flags 63 voltage detection register 69

W

watch-dog timer mode registerwatch-dog timer mode register 60 time select 61

Χ

XTAL1 5 XTAL1 pin function 16 XTAL2 5 XTAL2 pin function 16