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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lap4004g

Table of Contents

```
P25 ▭ 1          28 ▭ P24
P26 ▭ 2          27 ▭ P23
P27 ▭ 3          26 ▭ P22
P04 ▭ 4          25 ▭ P21
P05 ▭ 5          24 ▭ P20
P06 ▭ 6   28-Pin 23 ▭ P03
P07 ▭ 7   PDIP   22 ▭ V_SS
V_DD ▭ 8  SOIC   21 ▭ P02
XTAL2 ▭ 9 SSOP   20 ▭ P01
XTAL1 ▭ 10 CDIP* 19 ▭ P00
P31 ▭ 11         18 ▭ Pref1/P30
P32 ▭ 12         17 ▭ P36
P33 ▭ 13         16 ▭ P37
P34 ▭ 14         15 ▭ P35
```
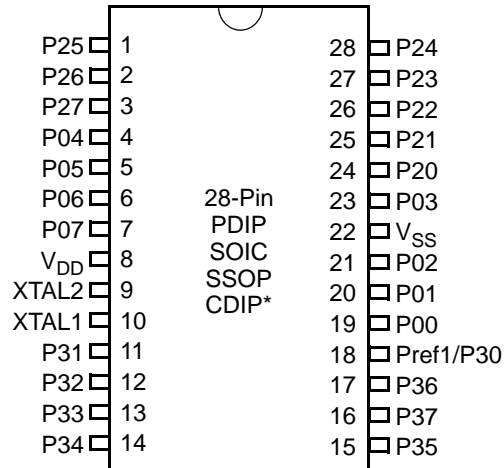
Figure 4.   28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4.   28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V_{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V_{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V_{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

▶ **Note:**   *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.
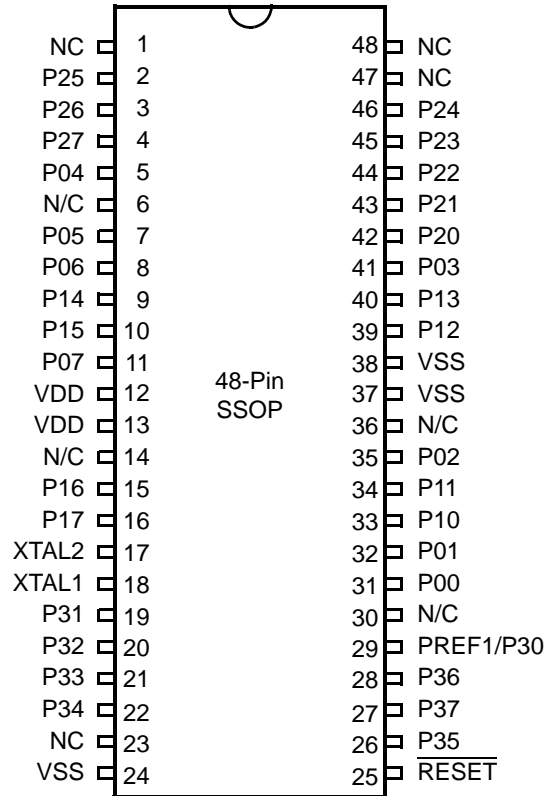
```
               ┌────────∪────────┐
       NC  ┌┤  1            48  ├┐  NC
      P25  ┌┤  2            47  ├┐  NC
      P26  ┌┤  3            46  ├┐  P24
      P27  ┌┤  4            45  ├┐  P23
      P04  ┌┤  5            44  ├┐  P22
      N/C  ┌┤  6            43  ├┐  P21
      P05  ┌┤  7            42  ├┐  P20
      P06  ┌┤  8            41  ├┐  P03
      P14  ┌┤  9            40  ├┐  P13
      P15  ┌┤ 10            39  ├┐  P12
      P07  ┌┤ 11     48-Pin 38  ├┐  VSS
      VDD  ┌┤ 12     SSOP   37  ├┐  VSS
      VDD  ┌┤ 13            36  ├┐  N/C
      N/C  ┌┤ 14            35  ├┐  P02
      P16  ┌┤ 15            34  ├┐  P11
      P17  ┌┤ 16            33  ├┐  P10
    XTAL2  ┌┤ 17            32  ├┐  P01
    XTAL1  ┌┤ 18            31  ├┐  P00
      P31  ┌┤ 19            30  ├┐  N/C
      P32  ┌┤ 20            29  ├┐  PREF1/P30
      P33  ┌┤ 21            28  ├┐  P36
      P34  ┌┤ 22            27  ├┐  P37
       NC  ┌┤ 23            26  ├┐  P35
      VSS  ┌┤ 24            25  ├┐  RESET
               └─────────────────┘
```

Figure 6.   48-Pin SSOP Pin Configuration

Table 5.   40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12

Table 8. DC Characteristics (Continued)

Symbol	Parameter	V_{CC}	T_A= 0°C to +70°C			Units	Conditions	Notes
			Min	Typ	Max			
I_{CC1}	Standby Current (HALT Mode)	2.0			3	mA	V_{IN} = 0V, V_{CC} at 8.0MHz	1, 2
		3.6			5		Same as above	1, 2
		2.0			2		Clock Divide-by-16 at 8.0MHz	1, 2
		3.6			4		Same as above	1, 2
I_{CC2}	Standby Current (Stop Mode)	2.0			8	µA	V_{IN} = 0 V, V_{CC} WDT is not Running	3
		3.6			10	µA	Same as above	3
		2.0			500	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6			800	µA	Same as above	3
I_{LV}	Standby Current (Low Voltage)				10	µA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection				2.0	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	Vcc Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes:
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 µF), physically close to the V_{DD} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.
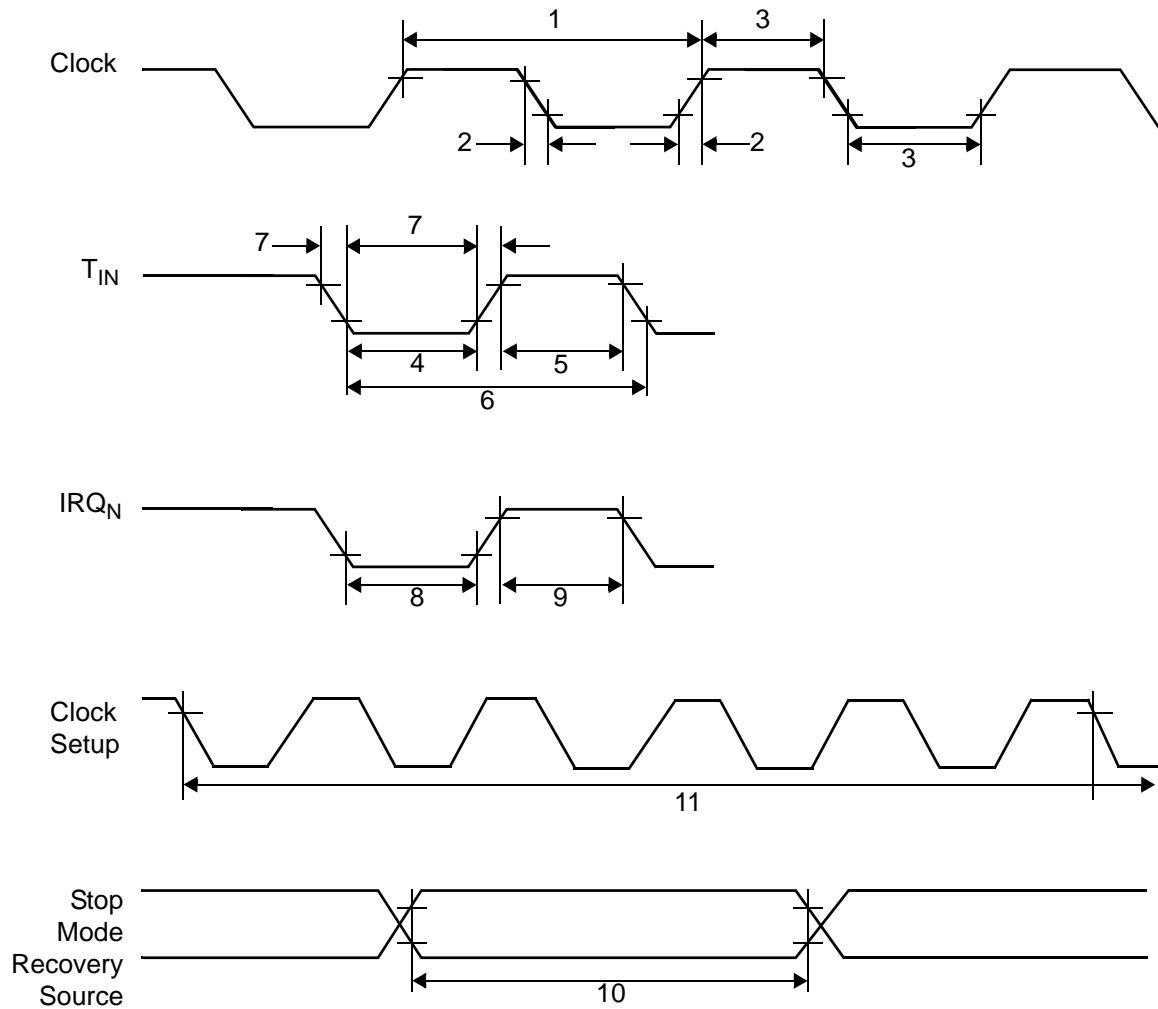
Figure 8.   AC Timing Diagram
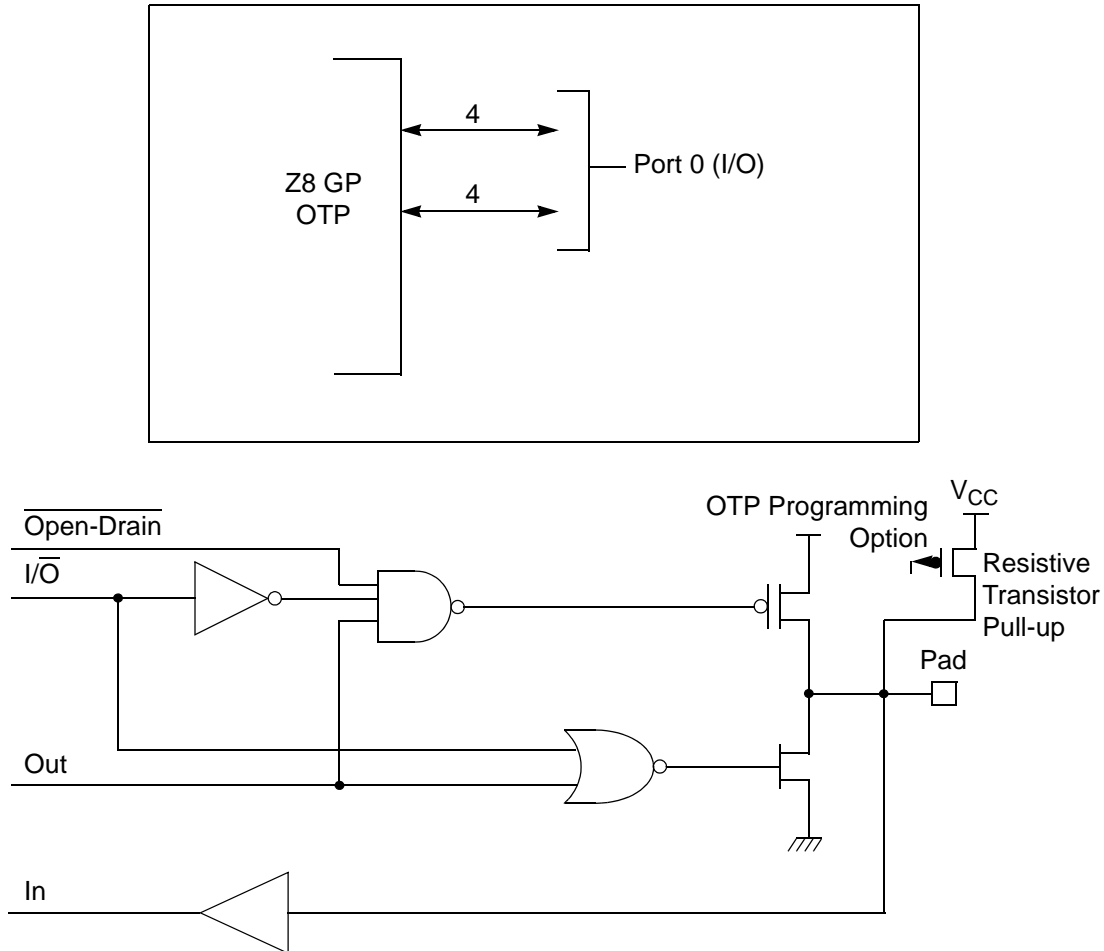
Figure 9.   Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

▶ **Note:** The Port 1 direction is reset to be input following an SMR.
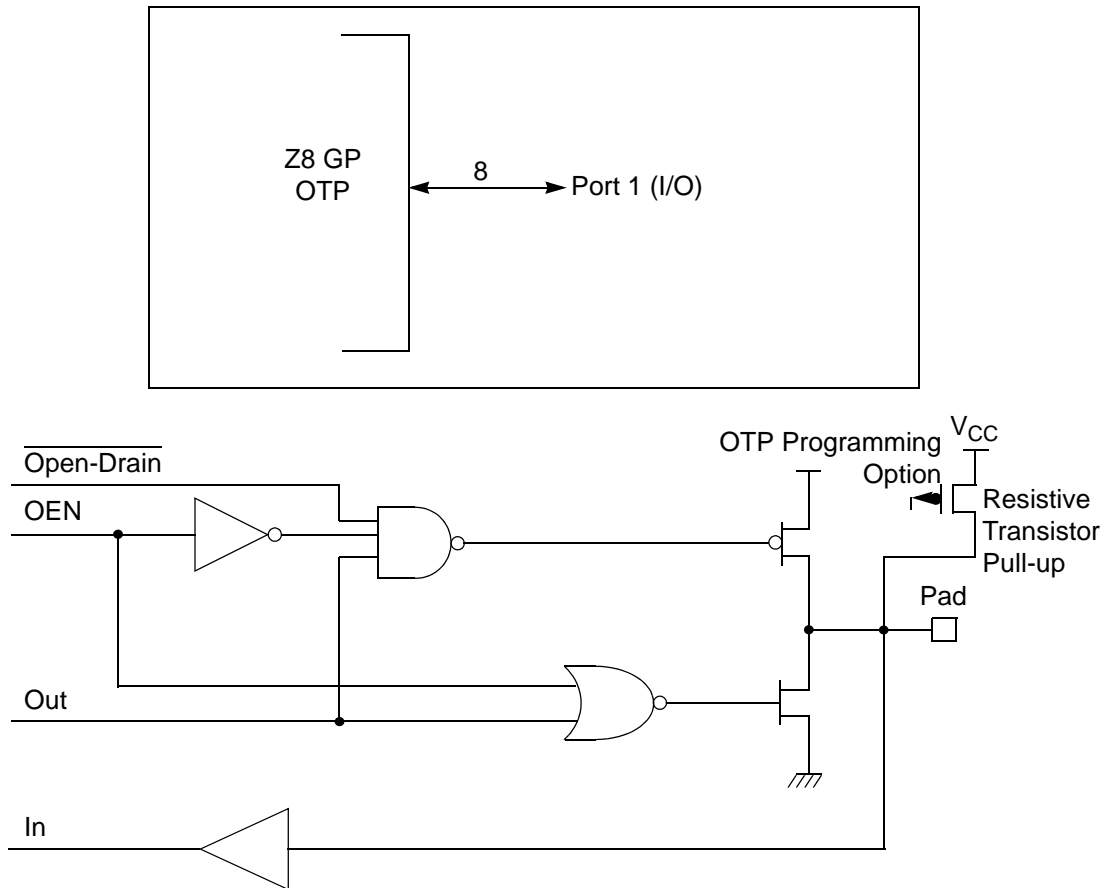
Figure 10. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.
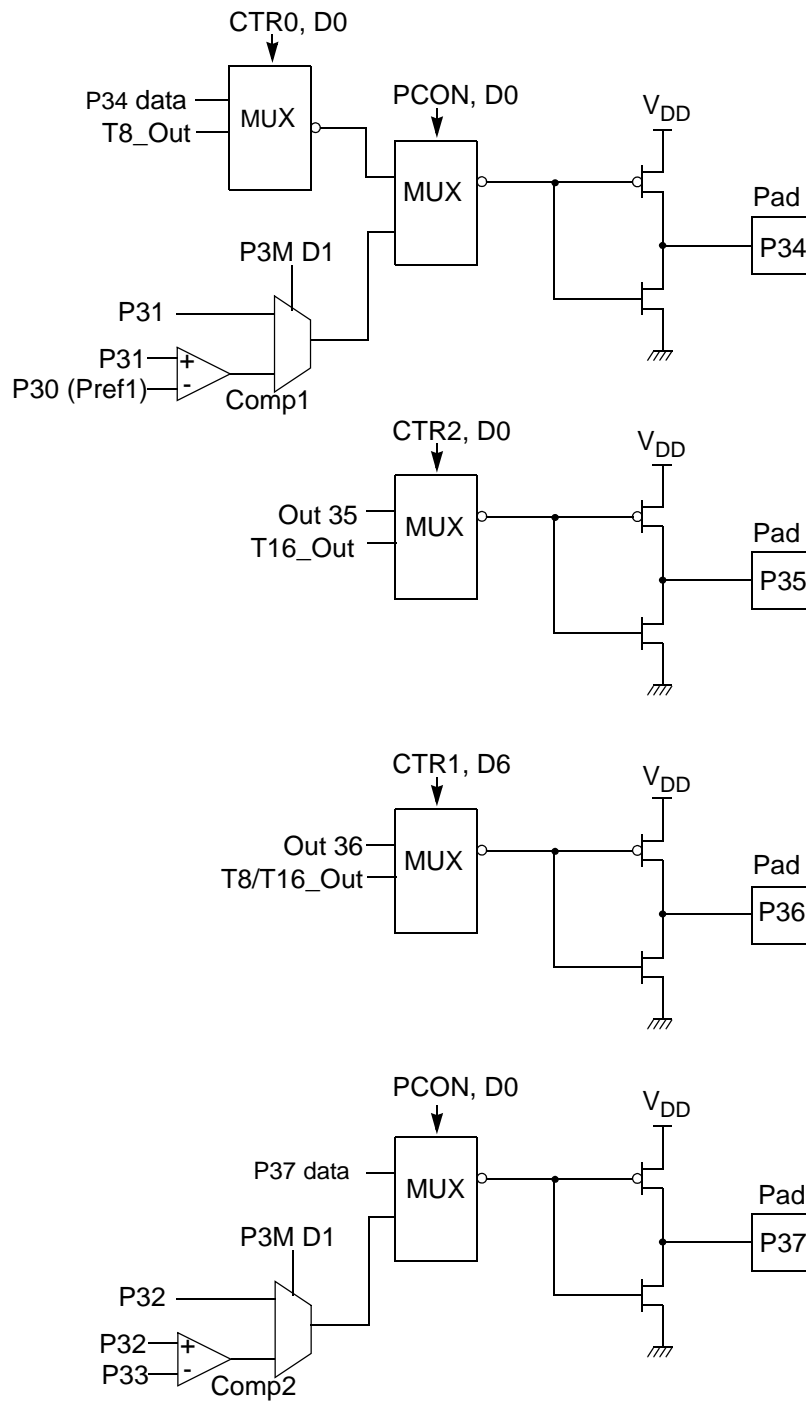
Figure 13. Port 3 Counter/Timer Output Configuration

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 12 lists and briefly describes the fields for this register.

Table 12. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R/W	0	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

Table 13. CTR1(0D)01H T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/	- - - - 3 2 - -	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	- - - - - - 1 -			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	- - - - - - - 0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default at Power-On Reset.
**Default at Power-On Reset.Not reset with Stop Mode recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to "NORMAL OPERATION Mode" terminates the "PING-PONG Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

> **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 14 lists and briefly describes the fields for this register.
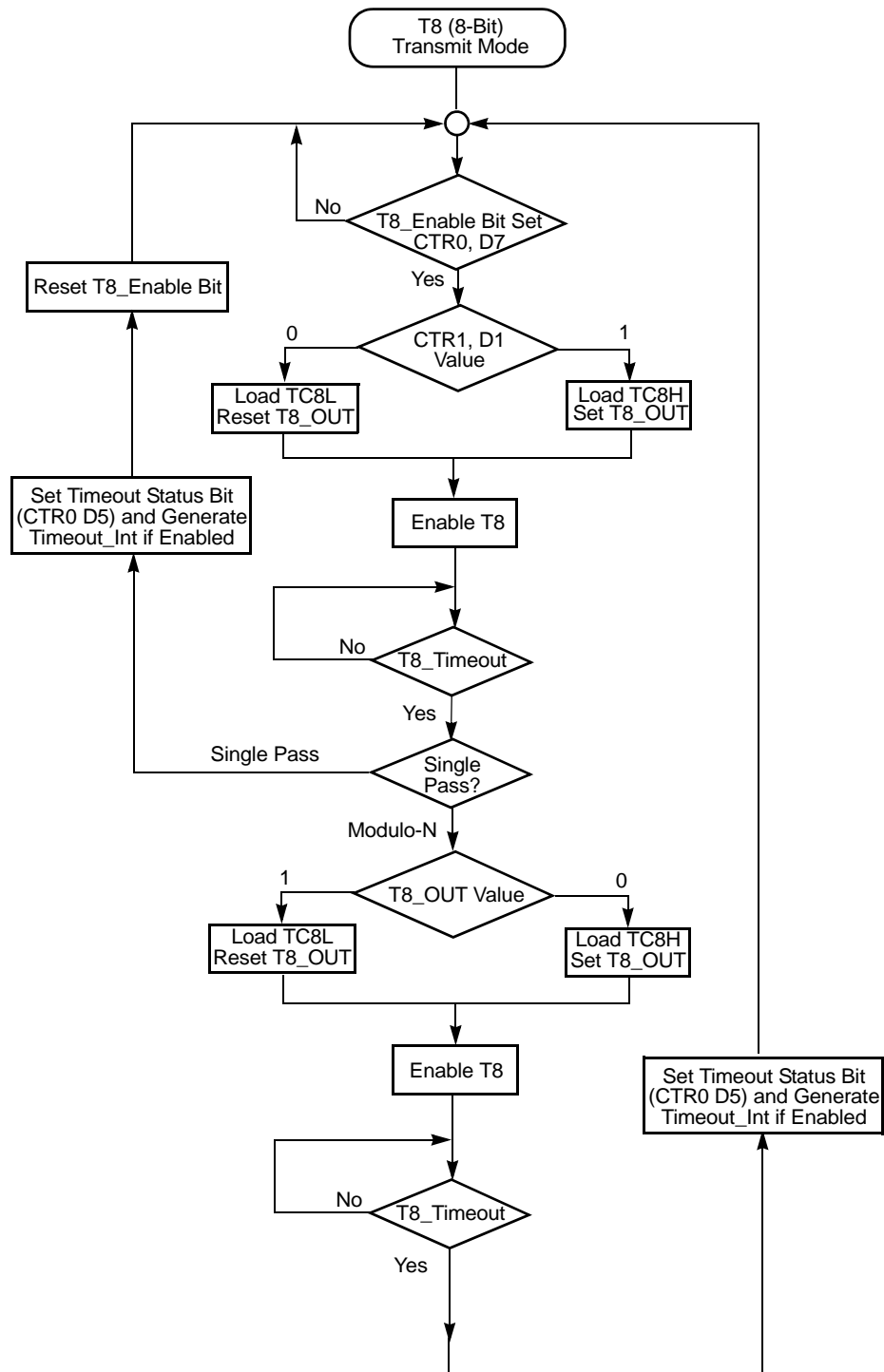
Figure 19. Transmit Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.
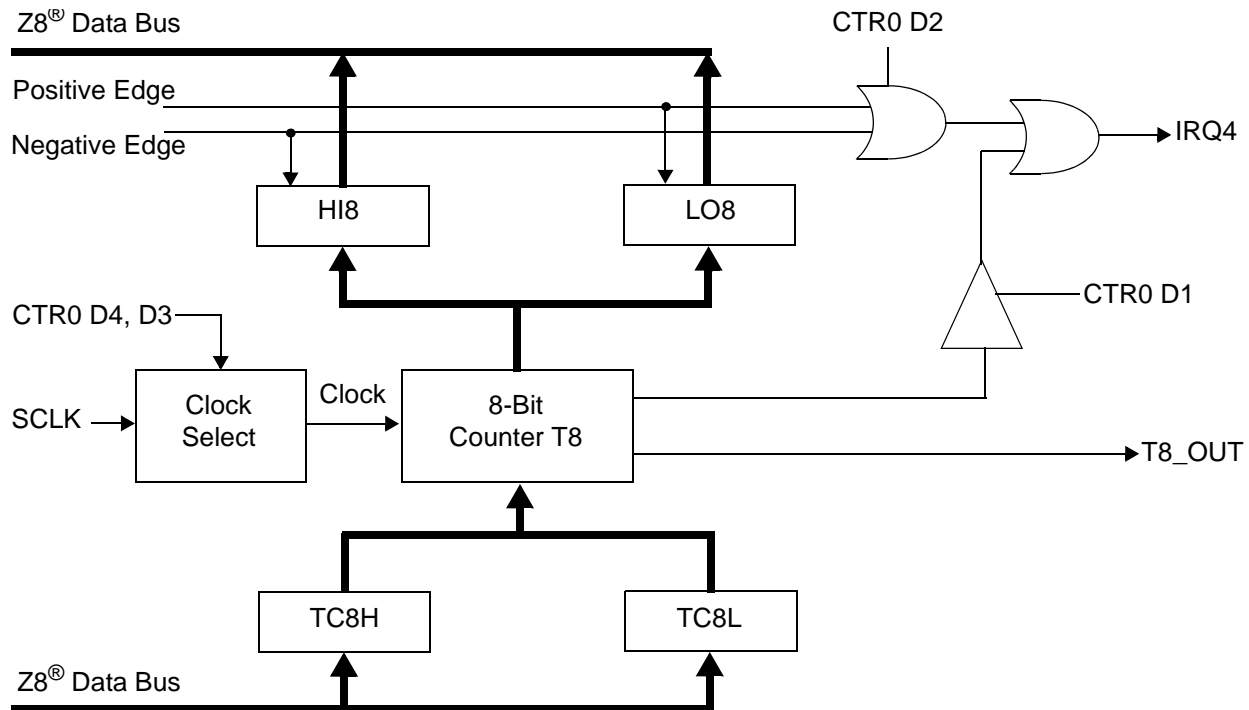
Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

⚠ **Caution:**   To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is illustrated in Figure 29. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

Interrupts

The Z8 GP[TM] OTP MCU Family features six different interrupts (Table 16). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 16) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 57.
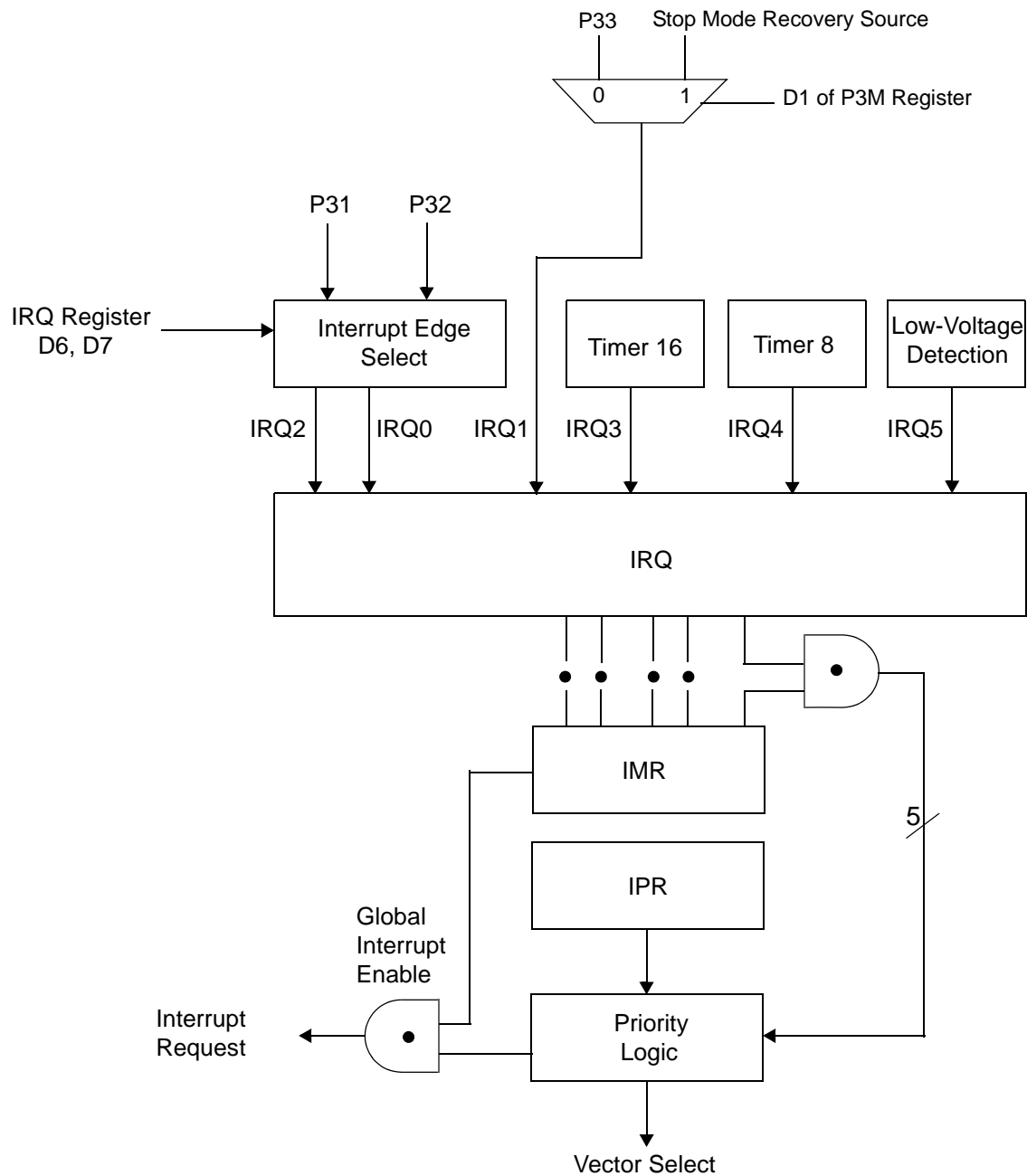
Figure 30. Interrupt Block Diagram

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.

Crystal
C1, C2 = 33pF TYP *
f = 8 MHz

External Clock

* Preliminary value including pin parasitics

Ceramic Resonator f = 8MHz
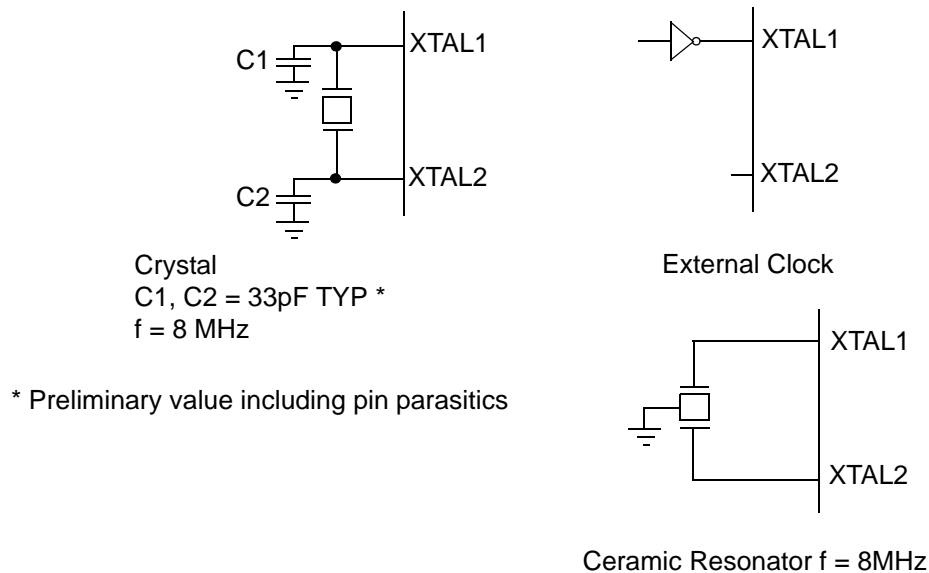
Figure 31. Oscillator Configuration

SMR2(0F)0DH

D7	D6	D5	D4	D3	D2	D1	D0

Reserved (Must be 0)

Reserved (Must be 0)

Stop-Mode Recovery Source 2
000 POR Only *
001 NAND P20, P21, P22, P23
010 NAND P20, P21, P22, P23, P24, P25, P26, P27
011 NOR P31, P32, P33
100 NAND P31, P32, P33
101 NOR P31, P32, P33, P00, P07
110 NAND P31, P32, P33, P00, P07
111 NAND P31, P32, P33, P20, P21, P22

Reserved (Must be 0)

Recovery Level * *
0 Low
1 High

Reserved (Must be 0)
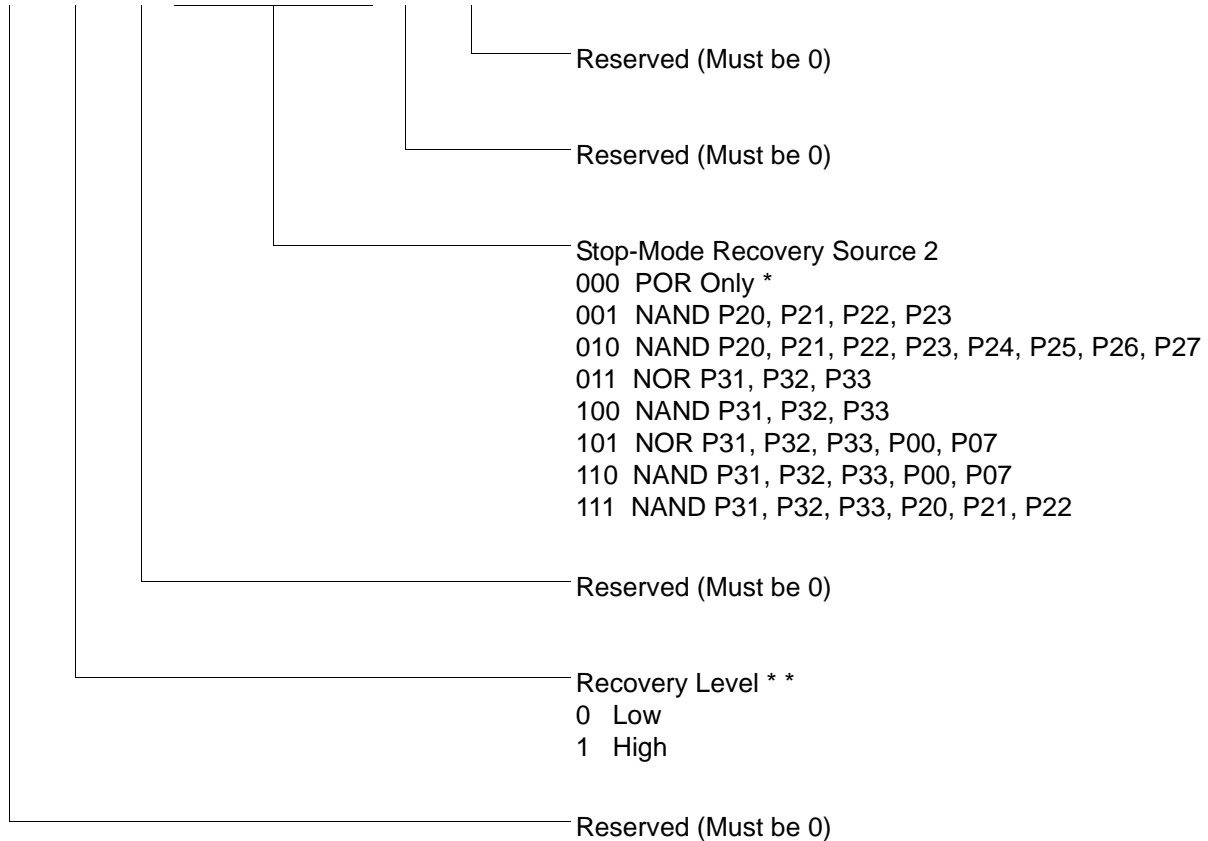
Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.
* Default setting after reset
* * At the XOR gate input

Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)
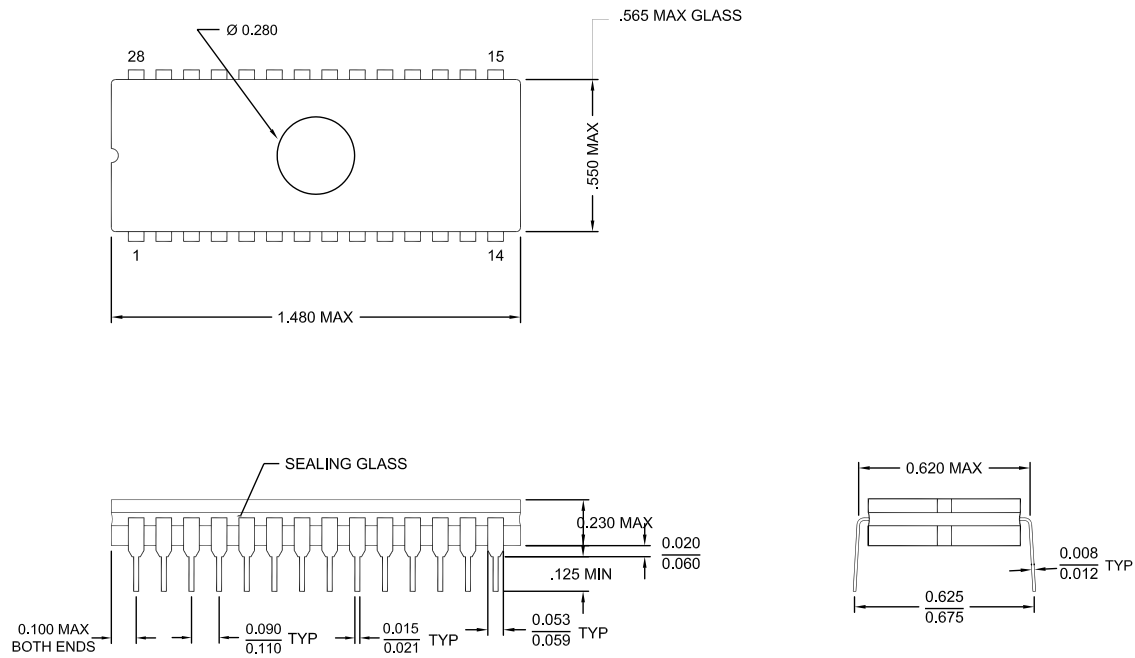
Figure 62. 28-Pin CDIP Package

Index