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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lap4008c

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Table 2. Power Connections

Connection	Circuit	Device	
Power	V _{CC}	V _{DD}	
Ground	GND	V _{SS}	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram





	Г				
NC		1	$\overline{}$	40	⊐ NC
P25		2		39	⊐ P24
P26		3		38	⊐ P23
P27		4		37	⊐ P22
P04		5		36	🗆 P21
P05	d	6	40-Pir	35	⊐ P20
P06		7	PDIP	34	⊐ P03
P14		8	CDIP'	. 33	🗖 P13
P15		9	•	32	⊐ P12
P07	d	10		31	⊐ VSS
VDD		11		30	⊐ P02
P16	d	12		39	🗆 P11
P17	d	13		28	⊐ P10
XTAL2	d	14		27	⊐ P01
XTAL1	d	15		26	⊐ P00
P31	d	16		25	□ Pref1/P30
P32	d	17		24	⊐ P36
P33	þ	18		23	⊐ P37
P34	d	19		22	□ <u>P35</u>
NC		20		21	RESET

Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

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	1		1 7			
NC		1	\bigcirc	18	_	NC
DOF		2		40		NC
P20		2		47		NC DO4
P26		3		40		P24
P27		4		45		P23
P04	E	5		44		P22
N/C		6		43		P21
P05		7		42		P20
P06		8		41		P03
P14		9		40		P13
P15		10		39		P12
P07	E	11	40 D'	38		VSS
VDD	E	12	48-PIN	37		VSS
VDD		13	330P	36		N/C
N/C	C	14		35		P02
P16		15		34		P11
P17		16		33		P10
XTAL2		17		32		P01
XTAL1		18		31		P00
P31		19		30		N/C
P32		20		29		PREF1/P30
P33		21		28		P36
P34		22		27		P37
NC		23		26	_	P35
VSS	H	20		20	_	RESET
.00	_	24		20		

Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12





Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.



Note: The Port 1 direction is reset to be input following an SMR.

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Location of 32	768	Not Accessible
first Byte of		On-Chip
executed		ROW
after RESET	12	Reset Start Address
	11	IRQ5
	10	IRQ5
	9	IRQ4
	8	IRQ4
Interrupt Vector	7	IRQ3
(Lower Byte)	6	IRQ3
	5	► IRQ2
Interrupt Vector	4	┍ IRQ2
(Upper Byte)	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0

Figure 14. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The $Z8^{\ensuremath{\mathbb{R}}}$ register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTRL0
LD	1, #xx	;	load CTRL1
LD	R1, 2	;	$CTRL2 \rightarrow CTRL1$
LD	RP. #0Dh	;	Select ERF D
for access to bank D	,	,	
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 \rightarrow register 71h			
LD	R1, 2		
; CTRL2 \rightarrow register 71h			

Register File

>

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.









* RP = 00: Selects Register Bank 0, Working Register Group 0

Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.







Figure 19. Transmit Mode Flowchart



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.



Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

Table 16. Interrupt Types, Sources, and Vectors

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z8 GPTM OTP MCU Family interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 17.

l	RQ	Interrupt Edge			
D7	D6	IRQ2 (P31)	IRQ0 (P32)		
0	0	F	F		
0	1	F	R		
1	0	R	F		
1	1	R/F	R/F		
Note: F = Falling Edge; R = Rising Edge					

Table 17. IRQ Register



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line
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Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H



* Default setting after reset

Figure 32. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.







Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 19).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 18 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Reserved	7		0	Reserved (Must be 0)
Recovery Level	-6	W	0 [†]	Low
-			1	High
Reserved	5		0	Reserved (Must be 0)
Source	432	W	000†	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	10		00	Reserved (Must be 0)

Table 18. SMR2(F)0DH:Stop Mode Recovery Register 2*

Notes:

* Port pins configured as outputs are ignored as a SMR recovery source. † Indicates the value upon Power-On Reset

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Figure 35. Stop Mode Recovery Source

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CTR1(0D)01H D7 D6 D5 D3 D1 D0 D4 D2 Transmit Mode* R/W 0 T16_OUT is 0 initially* 1 T16_OUT is 1 initially **Demodulation Mode** R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially **Demodulation Mode** R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 **Demodulation Mode** 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 1 Reserved Transmit Mode/T8/T16 Logic 0 0 AND** 0 1 OR 1 0 NOR 1 1 NAND **Demodulation Mode** 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 1 Reserved Transmit Mode 0 P36 as Port Output * 1 P36 as T8/T16_OUT **Demodulation Mode** 0 P31 as Demodulator Input 1 P20 as Demodulator Input Transmit/Demodulation Mode 0 Transmit Mode * * Default setting after reset **Default setting after reset. Not reset with Stop Mode 1 Demodulation Mode recovery







Notes: Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



CTR2(0D)02H



Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)





CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved No effect when written Always reads 11111
								Sync Mode 0* Disable Sync Mode** 1 Enable Sync Mode
								T ₈ Enable R 0* T ₈ Disabled R 1 T ₈ Enabled W0 Stop T ₈ W1 Enable T ₈
								T ₁₆ Enable R 0* T ₁₆ Disabled R 1 T ₁₆ Enabled W 0 Stop T ₁₆ W 1 Enable T ₁₆

* Default setting after reset. ** Default setting after reset. Not reset with Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.



Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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