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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lap4008g

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### **Development Features**

Table 1 lists the features of  $ZiLOG^{(R)}$ 's Z8  $GP^{TM}$  OTP MCU Family family members.

#### Table 1. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323L OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V-3.6V

- Low power consumption–6mW (typical)
- T = Temperature
  - S = Standard 0° to +70°C
  - $E = Extended 40^{\circ} to + 105^{\circ}C$
  - A = Automotive  $-40^{\circ}$  to  $+125^{\circ}$ C
- Three standby modes:
  - STOP-2µA (typical)
  - HALT-0.8mA (typical)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors



#### Table 2. Power Connections

Connection	Circuit	Device	
Power	V <sub>CC</sub>	V <sub>DD</sub>	
Ground	GND	V <sub>SS</sub>	



Note: Refer to the specific package for available pins.

#### Figure 1. Functional Block Diagram





#### Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 3.	20-Pin PDIP/SOIC/SSOP/CDIP*	Pin	Identification
			achthoution

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20-P24	Port 2, Bits 0,1,2,3,4	Input/Output

**Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

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	1		1 7			
NC		1	$\bigcirc$	18	_	NC
DOF		2		40		NC
P20		2		47		NC DO4
P26		3		40		P24
P27		4		45		P23
P04	E	5		44		P22
N/C		6		43		P21
P05		7		42		P20
P06		8		41		P03
P14		9		40		P13
P15		10		39		P12
P07	E	11		38		VSS
VDD	E	12	48-PIN	37		VSS
VDD		13	330P	36		N/C
N/C	C	14		35		P02
P16		15		34		P11
P17		16		33		P10
XTAL2		17		32		P01
XTAL1		18		31		P00
P31		19		30		N/C
P32		20		29		PREF1/P30
P33		21		28		P36
P34		22		27		P37
NC		23		26	_	P35
VSS	H	20		20	_	RESET
.00	_	24		20		

Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V <sub>DD</sub>
31	24, 37, 38	V <sub>SS</sub>
25	29	Pref1/P30
	48	NC

#### Table 5. 40- and 48-Pin Configuration (Continued)



### **Absolute Maximum Ratings**

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

#### Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximu	m Units	Notes
Ambient temperature under bias	0	+70	С	
Storage temperature	-65	+150	С	
Voltage on any pin with respect to V <sub>SS</sub>	-0.3	+5.5	V	1
Voltage on $V_{DD}$ pin with respect to $V_{SS}$	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into $V_{DD}$ or out of $V_{SS}$		75	mA	
Notes:				

This voltage applies to all pins except the following: V<sub>DD</sub>, P32, P33 and RESET.

### **Standard Test Conditions**

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).



Figure 7. Test Load Diagram





Figure 10. Port 1 Configuration

#### Port 2 (P27-P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

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**Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTRL0
LD	1, #xx	;	load CTRL1
LD	R1, 2	;	$CTRL2 \rightarrow CTRL1$
LD	RP. #0Dh	;	Select ERF D
for access to bank D	,	,	
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 $\rightarrow$ register 71h			
LD	R1, 2		
; CTRL2 $\rightarrow$ register 71h			

#### **Register File**

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The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.









\* RP = 00: Selects Register Bank 0, Working Register Group 0

Figure 17. Register Pointer—Detail

#### Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



#### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

#### **Ping-Pong Mode**

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1, D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16\_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

**Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.



#### Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

#### Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 57) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address <code>0BH</code>.



#### Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH

D7	D6	D5	D4	D3	D2	D1	D0	]
								Reserved (Must be 0)   Reserved (Must be 0)   Stop-Mode Recovery Source 2   000 POR Only *   001 NAND P20, P21, P22, P23   010 NAND P20, P21, P22, P23, P24, P25, P26, P27   011 NOR P31, P32, P33   100 NAND P31, P32, P33   101 NOR P31, P32, P33, P00, P07   110 NAND P31, P32, P33, P00, P07
								Reserved (Must be 0) Recovery Level * * 0 Low * 1 High
								Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset

\* \* At the XOR gate input

#### Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.



**Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.



#### LVD(0D)0CH



\* Default

Figure 43. Voltage Detection Register

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### **Expanded Register File Control Registers (0F)**

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.





Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset

\* \* At the XOR gate input





#### R247 P3M(F7H)



\* Default setting after reset. Not reset with Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

INCH

NOM

0.073

0.005

0.068

0.006

0.402

0.209

0.307

0.030

0.0256 TYP



MAX

0.078

0.008

0.070

0.015

0.008

0.407

0.212

0.311

0.037





(	
	0-8

DETAIL 'A'

SYMBOL

А

A1

A2

В

С

D

Е

е

Н

L

MIN

1.73

0.05

1.68

0.25

0.09

10.07

5.20

7.65

0.63

CONTROLLING DIMENSIONS: MM LEADS ARE COPLANAR WITHIN .004 INCHES.

MILLIMETER

NOM

1.86

0.13

1.73

\_

10.20

5.30

0.65 TYP

7.80

0.75

MAX

1.99

0.21

1.78

0.38

0.20

10.33

5.38

7.90

0.95

MIN

0.068

0.002

0.066

0.010

0.004

0.397

0.205

0.301

0.025

Figure 65. 28-Pin SSOP Package Diagram



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