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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323las2016c00tr

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Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}
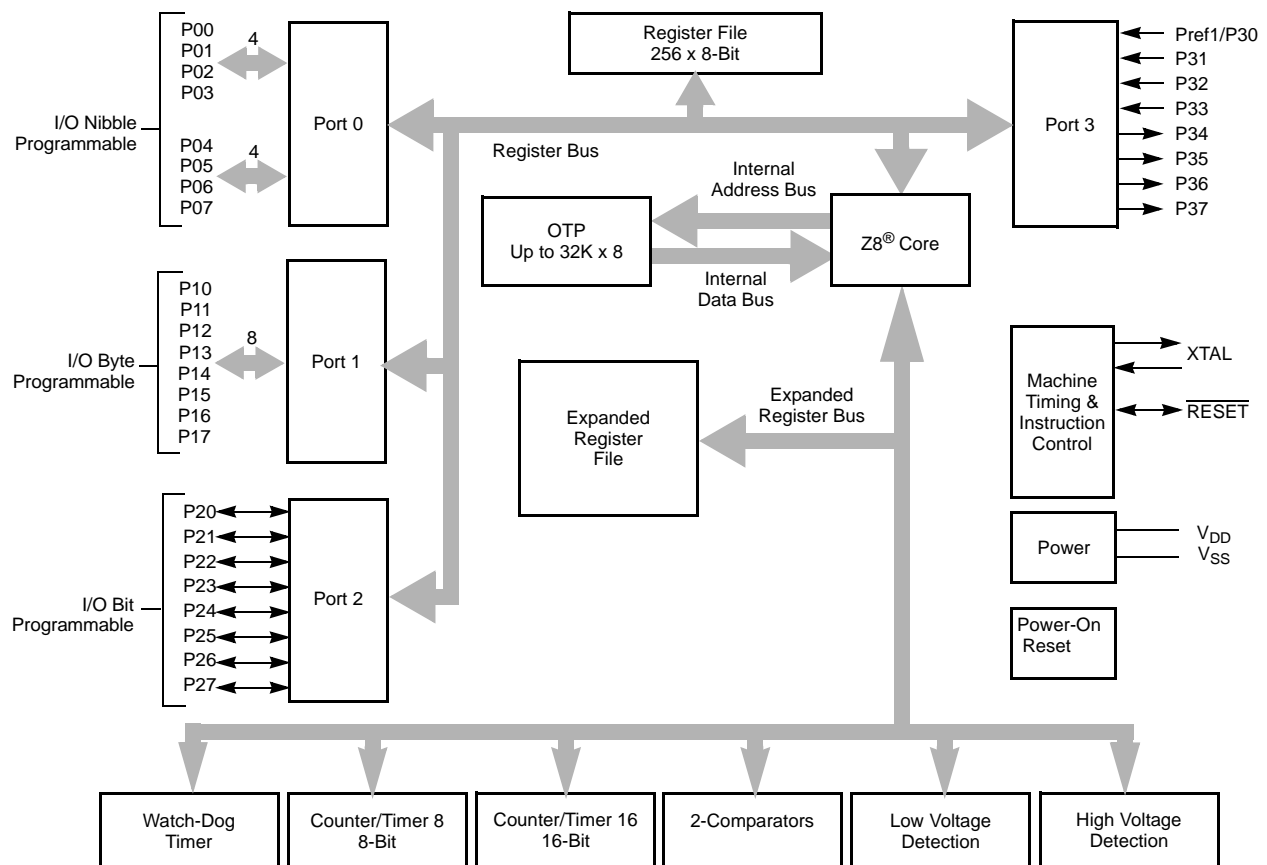
Note: Refer to the specific package for available pins.

Figure 1.   Functional Block Diagram

```
         ┌─────────⌣─────────┐
  NC  ◻  1                 48  ◻  NC
  P25 ◻  2                 47  ◻  NC
  P26 ◻  3                 46  ◻  P24
  P27 ◻  4                 45  ◻  P23
  P04 ◻  5                 44  ◻  P22
  N/C ◻  6                 43  ◻  P21
  P05 ◻  7                 42  ◻  P20
  P06 ◻  8                 41  ◻  P03
  P14 ◻  9                 40  ◻  P13
  P15 ◻ 10                 39  ◻  P12
  P07 ◻ 11     48-Pin      38  ◻  VSS
  VDD ◻ 12     SSOP        37  ◻  VSS
  VDD ◻ 13                 36  ◻  N/C
  N/C ◻ 14                 35  ◻  P02
  P16 ◻ 15                 34  ◻  P11
  P17 ◻ 16                 33  ◻  P10
 XTAL2◻ 17                 32  ◻  P01
 XTAL1◻ 18                 31  ◻  P00
  P31 ◻ 19                 30  ◻  N/C
  P32 ◻ 20                 29  ◻  PREF1/P30
  P33 ◻ 21                 28  ◻  P36
  P34 ◻ 22                 27  ◻  P37
  NC  ◻ 23                 26  ◻  P35
  VSS ◻ 24                 25  ◻  RESET
         └───────────────────┘
```
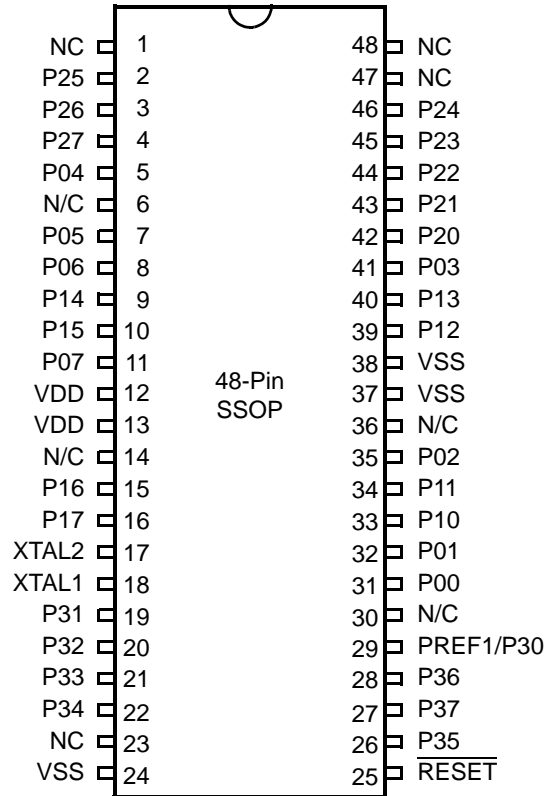
Figure 6.   48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12

Capacitance

Table 7 lists the capacitances.

Table 7. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF

Note: T_A = 25° C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND

DC Characteristics

Table 8. DC Characteristics

Symbol	Parameter	V_{CC}	T_A= 0°C to +70°C Min	Typ	Max	Units	Conditions	Notes
V_{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-3.6	0.8		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-3.6	V_{CC}–0.4			V	I_{OH} = −0.5mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V_{CC}–0.8			V	I_{OH} = −7mA	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	I_{OL} = 1.0mA I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{DD}-1.75	V		
I_{IL}	Input Leakage	2.0-3.6	−1		1	µA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
I_{OL}	Output Leakage	2.0-3.6	−1		1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0			10	mA	at 8.0 MHz	1, 2
		3.6			15	mA	at 8.0 MHz	1, 2

AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.
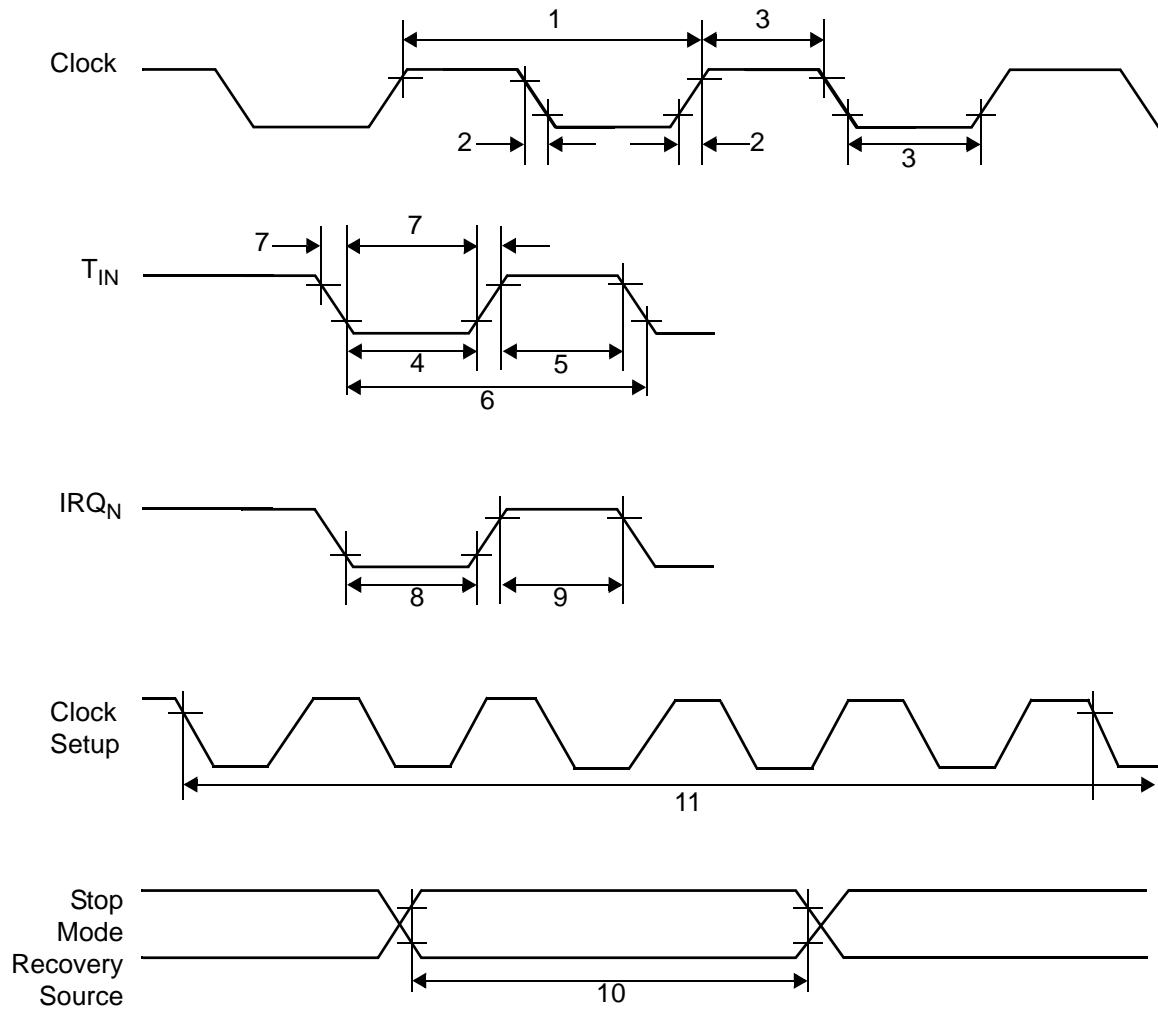

Figure 8.   AC Timing Diagram

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

> **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.
>
> The Port 0 direction is reset to be input following an SMR.

CTR1(0D)01H" on page 33). Other edge detect and IRQ modes are described in Table 11.

▶ **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Table 11. Port 3 Pin Function Summary

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

▶ **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

$\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP™ asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP™ does not assert the $\overline{\text{RESET}}$ pin when under VBO.

▶ **Note:** The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8®' functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0

Expanded Register
File Pointer

Working Register
Pointer

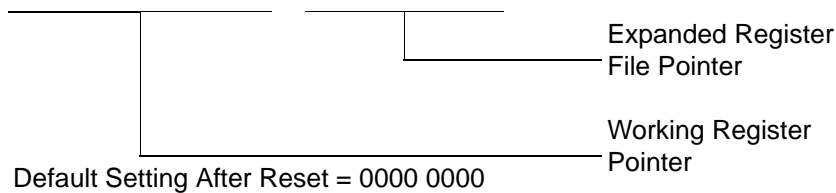Default Setting After Reset = 0000 0000

Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 26)

R253 RP = 00h
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0Dh
R0 = CTRL0
R1 = CTRL1
R2 = CTRL2
R3 = Reserved

Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.

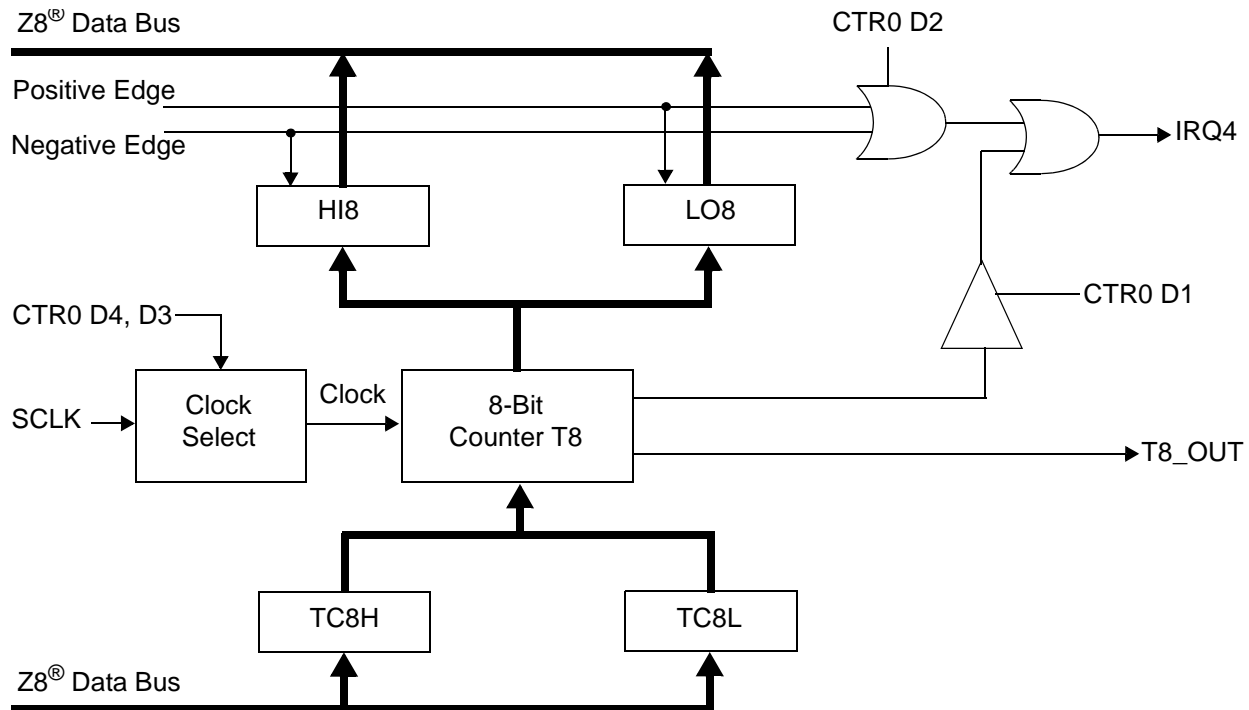**Figure 20. 8-Bit Counter/Timer Circuits**

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

⚠️ **Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is illustrated in Figure 29. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

Interrupts

The Z8 GP^{TM} OTP MCU Family features six different interrupts (Table 16). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 16) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 57.

LVD(0D)0CH

D7	D6	D5	D4	D3	D2	D1	D0

Voltage Detection
0: Disable *
1: Enable

LVD Flag (Read only)
0: LVD flag reset *
1: LVD flag set

HVD Flag (Read only)
0: HVD flag reset *
1: HVD flag set

Reserved (Must be 0)
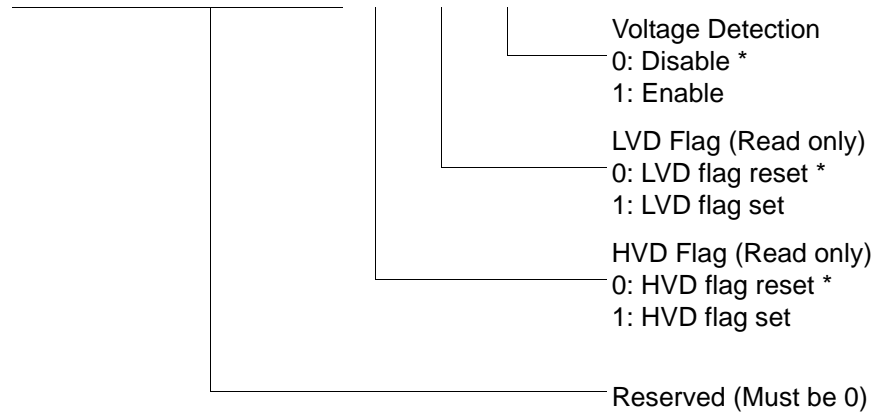
 * Default

Figure 43. Voltage Detection Register

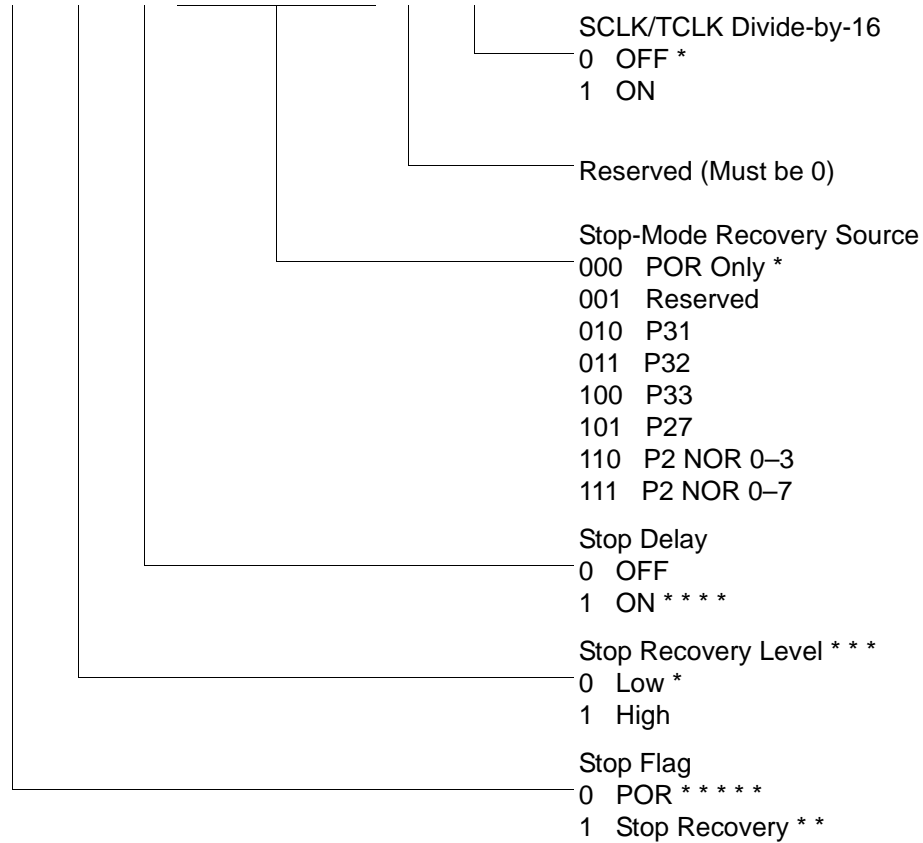▶ **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0

SCLK/TCLK Divide-by-16
0   OFF *
1   ON

Reserved (Must be 0)

Stop-Mode Recovery Source
000   POR Only *
001   Reserved
010   P31
011   P32
100   P33
101   P27
110   P2 NOR 0–3
111   P2 NOR 0–7

Stop Delay
0   OFF
1   ON * * * *

Stop Recovery Level * * *
0   Low *
1   High

Stop Flag
0   POR * * * * *
1   Stop Recovery * *

* Default setting after Reset
* * Set after STOP Mode Recovery
* * * At the XOR gate input
* * * * Default setting after Reset. Must be 1 if using a crystal or resonator clock source.
* * * * * Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

0= P31, P32 Digital Mode*
1= P31, P32 Analog Mode

Reserved (Must be 0)
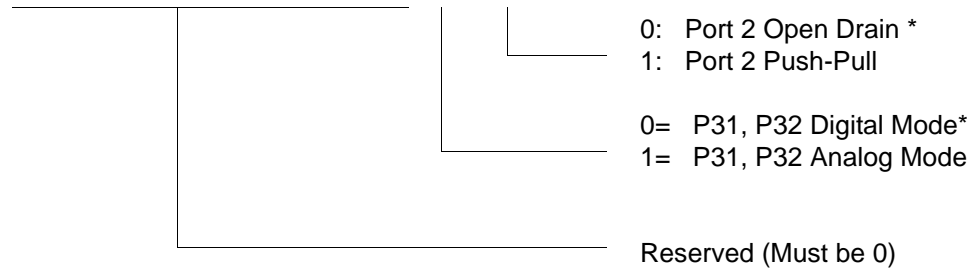
 * Default setting after reset. Not reset with Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

R250 IRQ(FAH)

D7	D6	D5	D4	D3	D2	D1	D0

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = T16
IRQ4 = T8
IRQ5 = LVD

Inter Edge
P31↓   P32↓ = 00
P31↓   P32↑ = 01
P31↑   P32↓ = 10
P31↑↓   P32↑↓ = 11
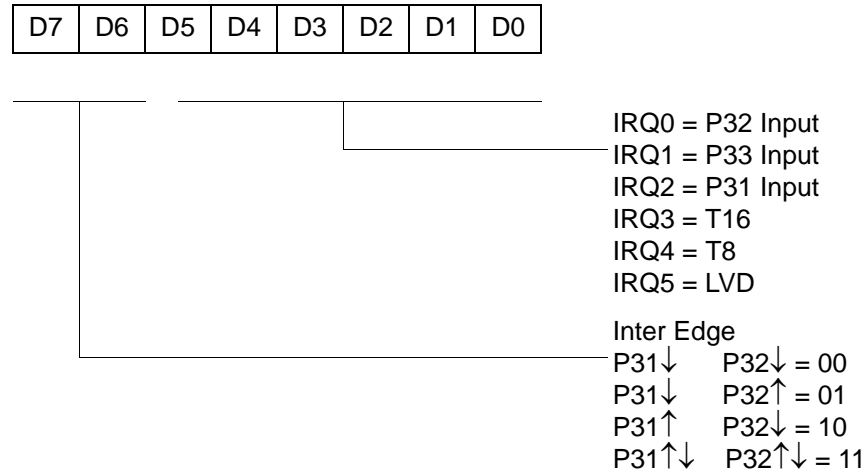
Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)

D7	D6	D5	D4	D3	D2	D1	D0

1 Enables IRQ5–IRQ0
   (D0 = IRQ0)

Reserved (Must be 0)

0   Master Interrupt Disable *
1   Master Interrupt Enable * *
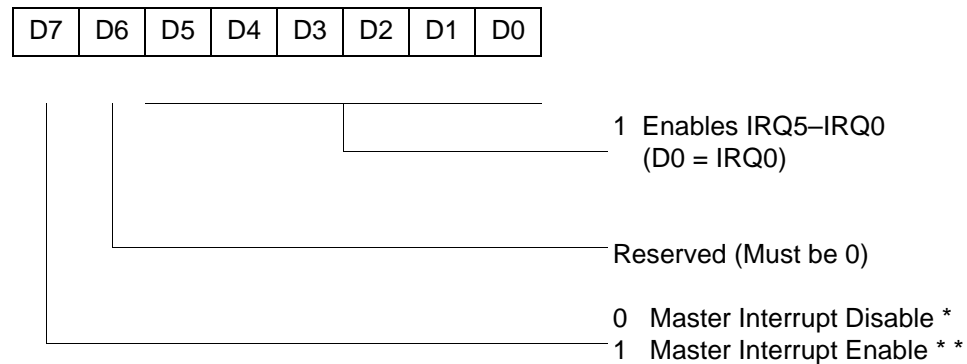
 * Default setting after reset
 * * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram

Figure 66. 40-Pin CDIP Package

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

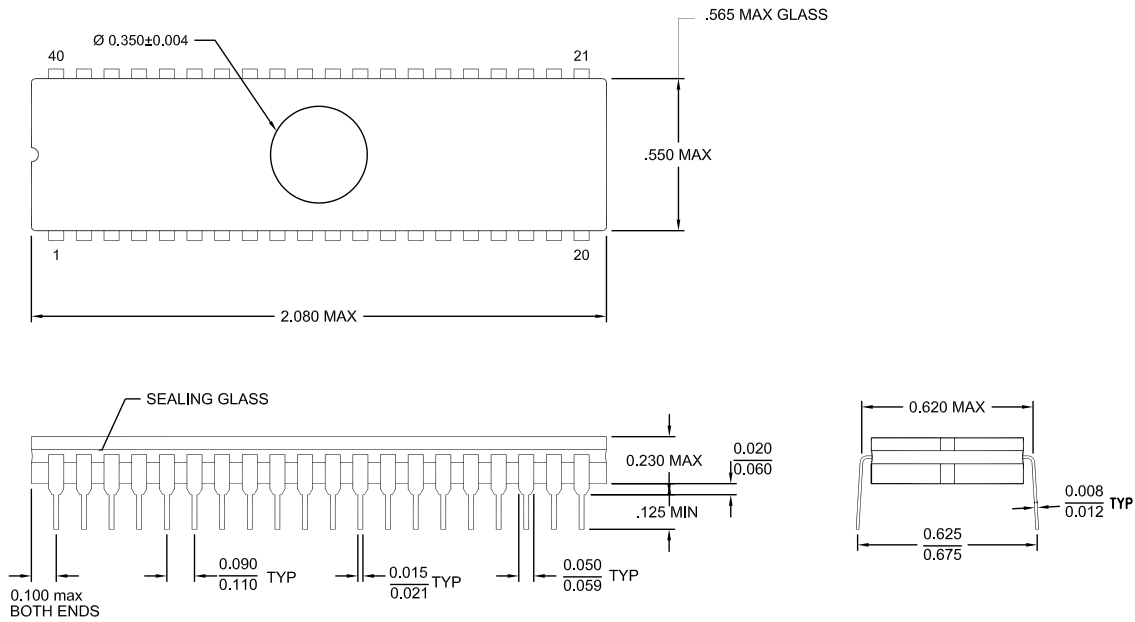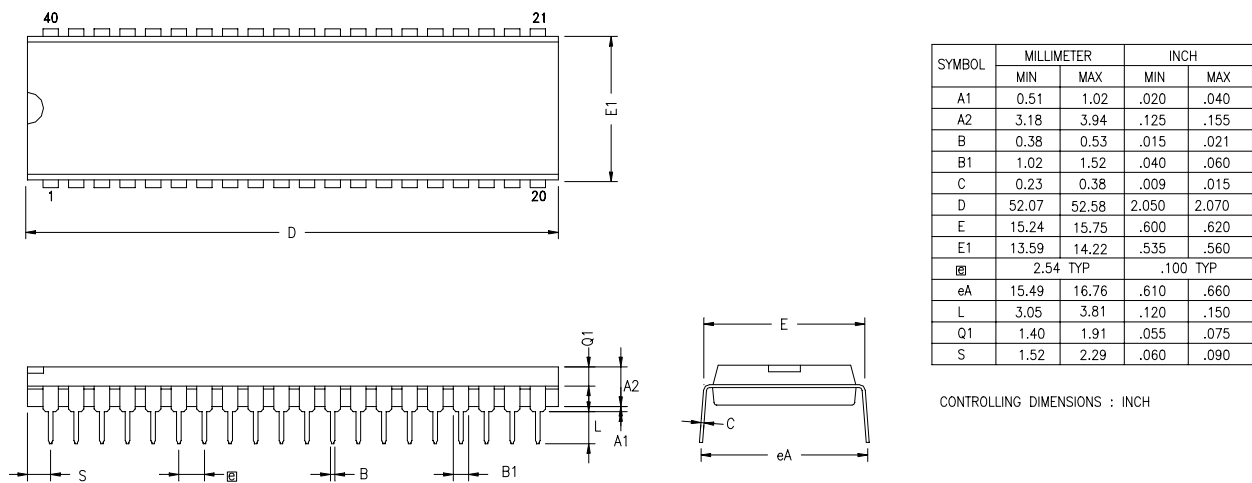CONTROLLING DIMENSIONS : INCH

Figure 67. 40-Pin PDIP Package Diagram

Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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