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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323las2032g



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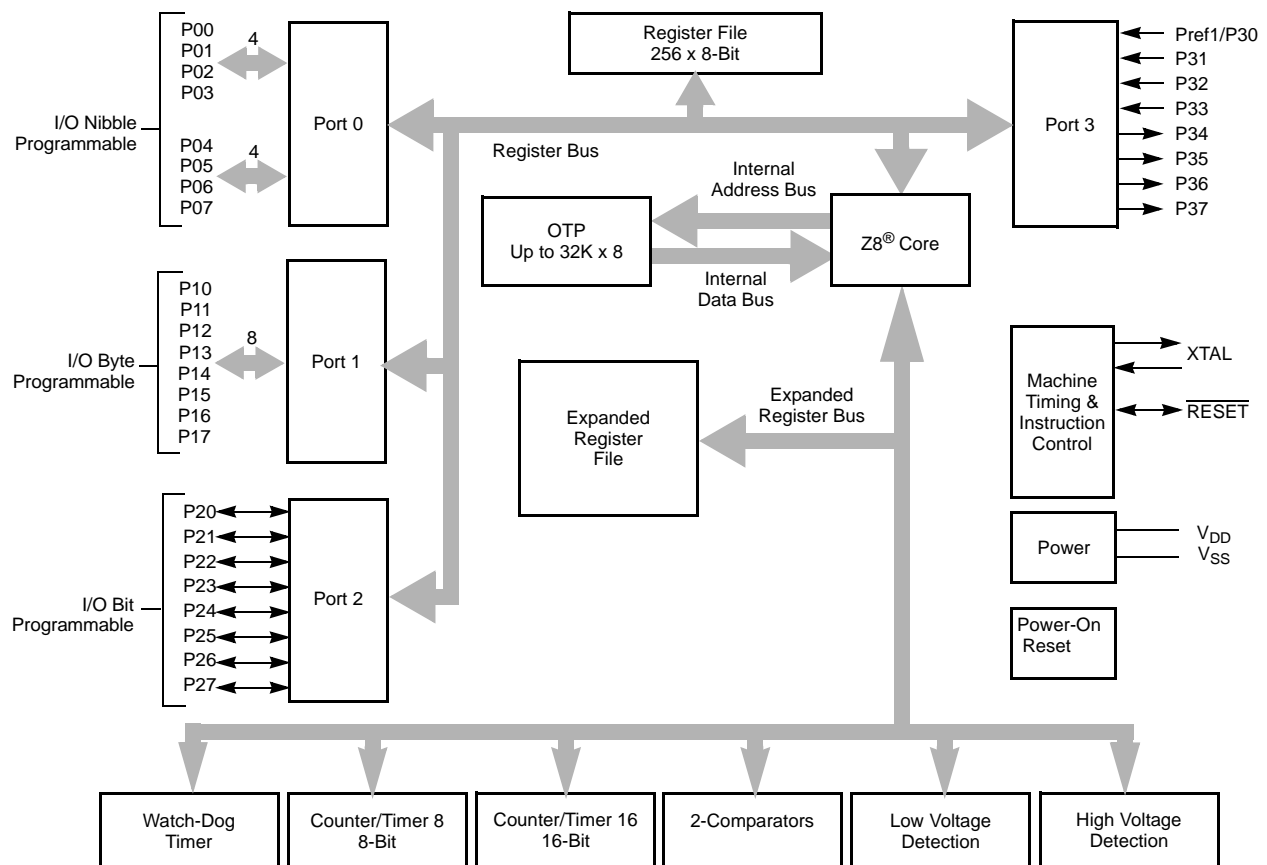


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Table 2. Power Connections

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

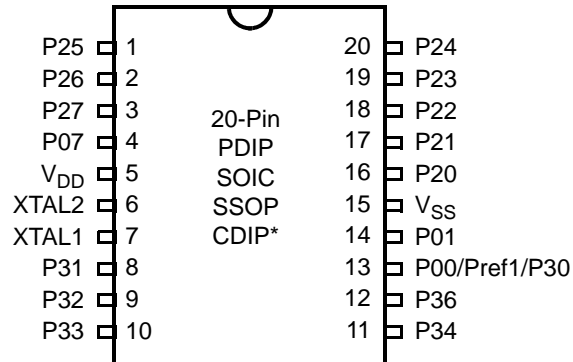


Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Absolute Maximum Ratings

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+70	C	
Storage temperature	-65	+150	C	
Voltage on any pin with respect to V_{SS}	-0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μ A	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Notes:
This voltage applies to all pins except the following: V_{DD} , P32, P33 and $\overline{\text{RESET}}$.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

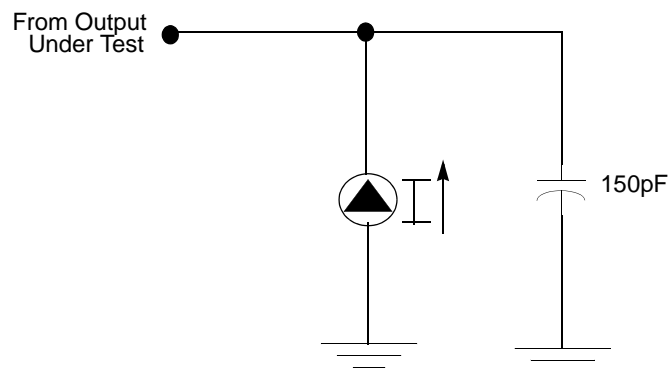


Figure 7. Test Load Diagram

Table 8. DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C			Units	Conditions	Notes
			Min	Typ	Max			
I _{CC1}	Standby Current (HALT Mode)	2.0			3	mA	V _{IN} = 0V, V _{CC} at 8.0MHz	1, 2
		3.6			5		Same as above	1, 2
		2.0			2		Clock Divide-by-16 at 8.0MHz	1, 2
		3.6			4		Same as above	1, 2
I _{CC2}	Standby Current (Stop Mode)	2.0			8	μA	V _{IN} = 0 V, V _{CC} WDT is not Running	3
		3.6			10	μA	Same as above	3
		2.0			500	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6			800	μA	Same as above	3
I _{LV}	Standby Current (Low Voltage)				10	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection				2.0	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to the V_{DD} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.

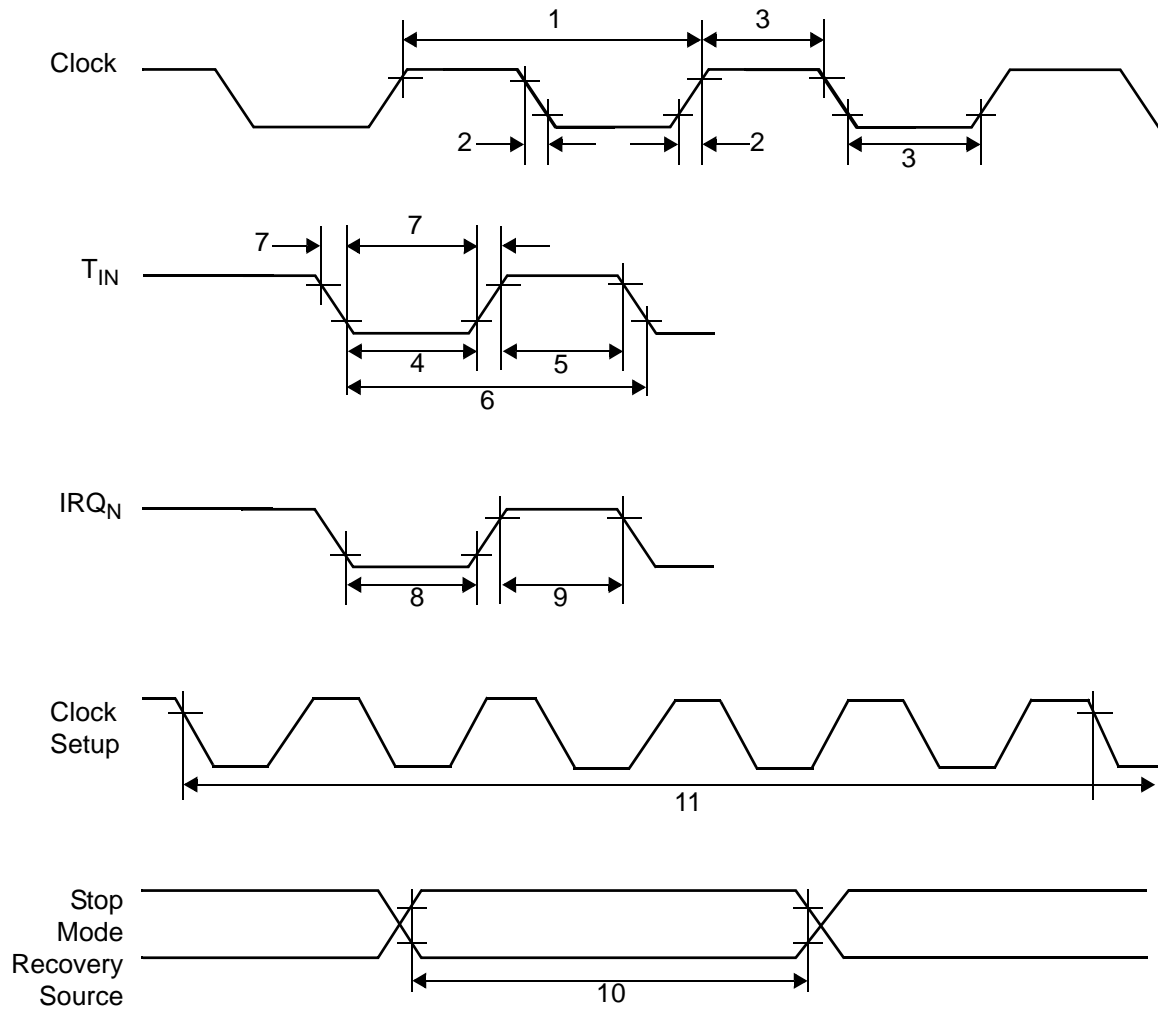


Figure 8. AC Timing Diagram

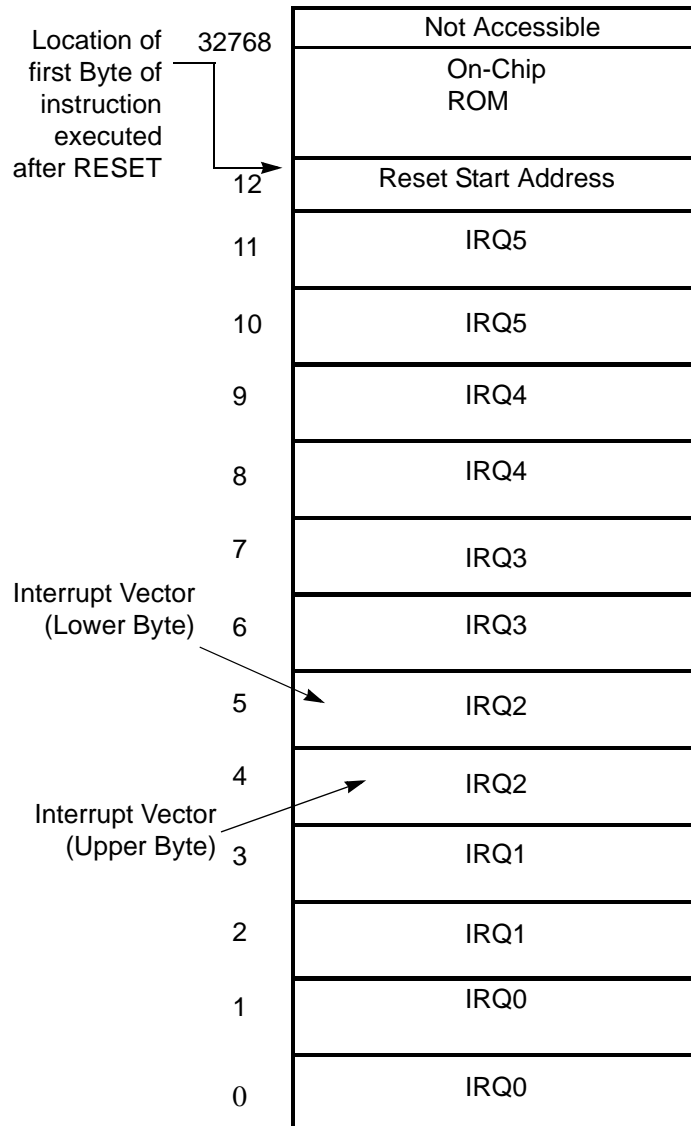


Figure 14. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8® register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the

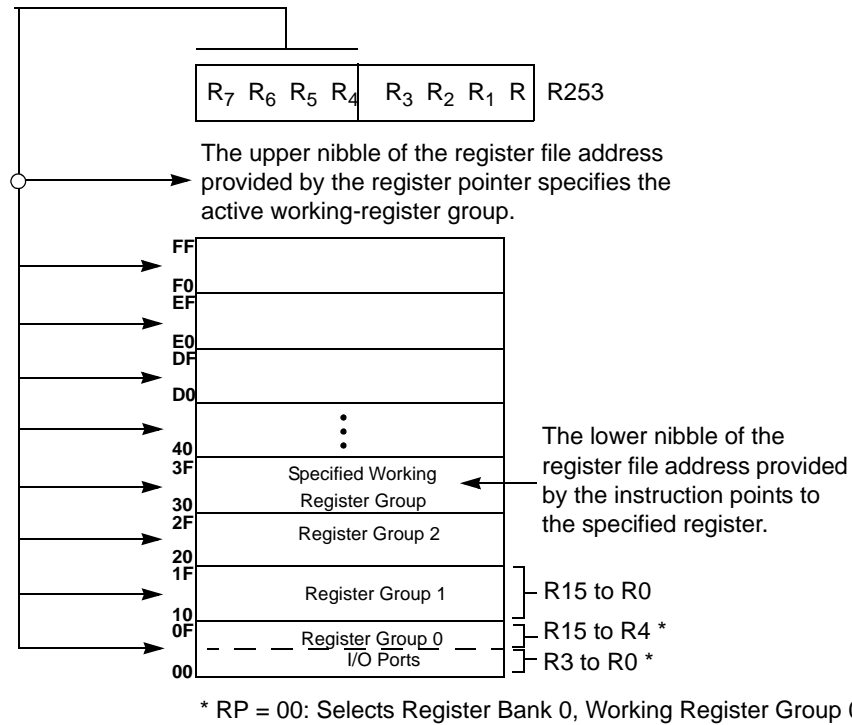


Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Table 12. CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	-----1-	R/W	0	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-----0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:

*Indicates the value upon Power-On Reset.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.



Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

This bit defines the frequency of the input signal to T8.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.

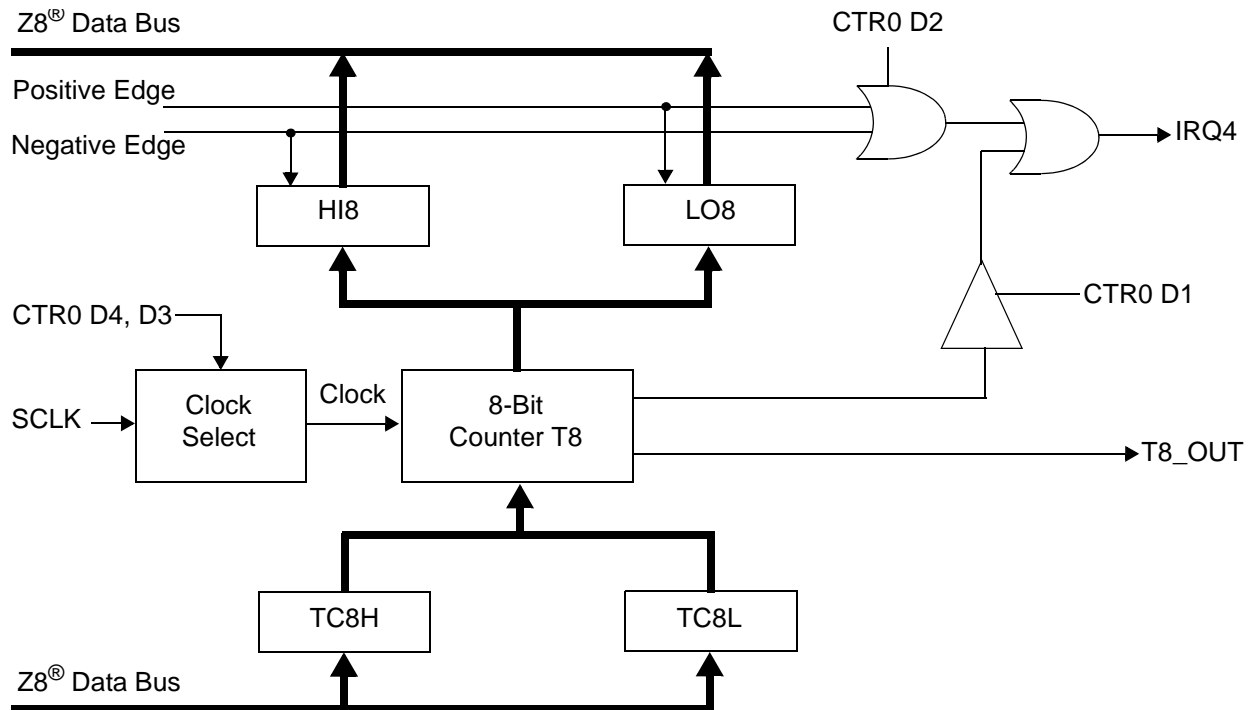


Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.*

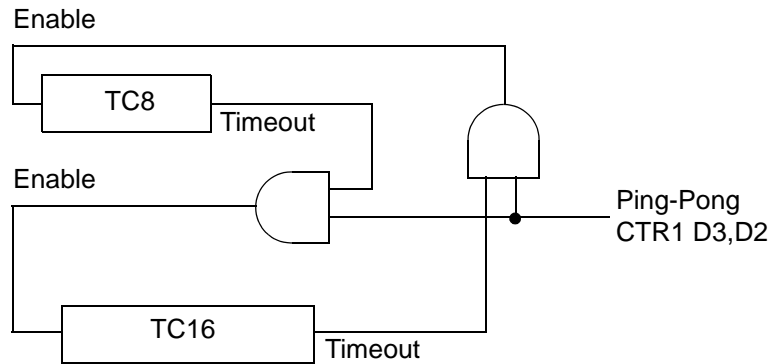


Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

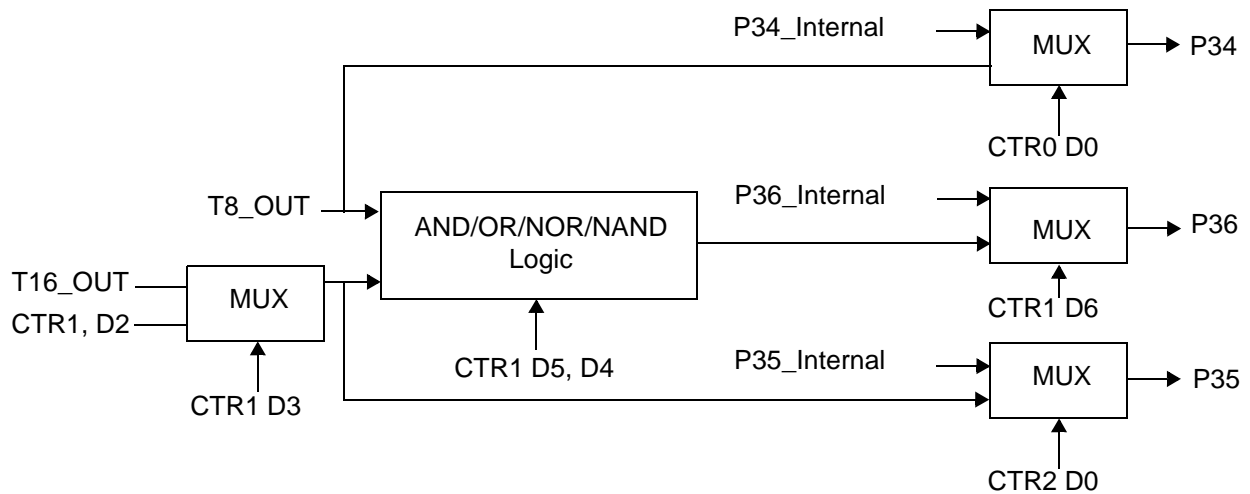


Figure 29. Output Circuit

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.

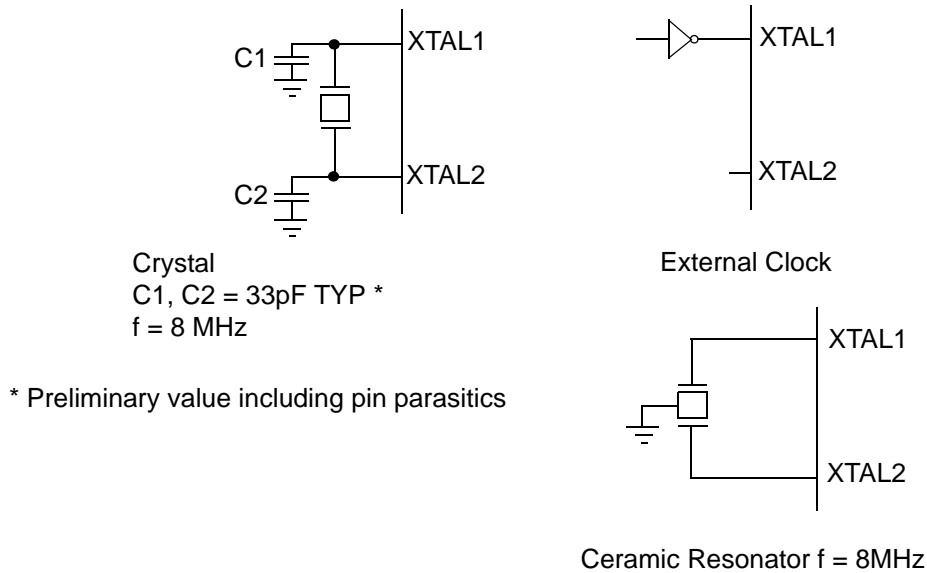


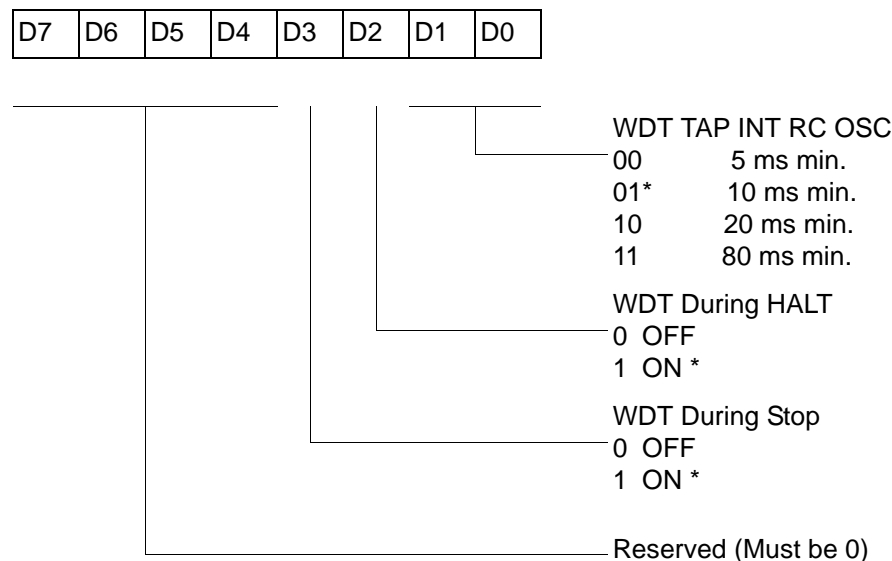
Figure 31. Oscillator Configuration

Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8® CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

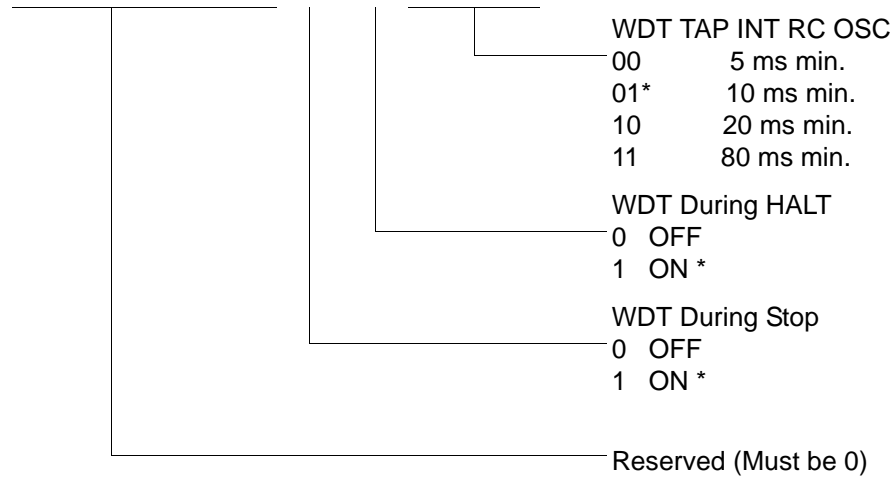
Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 20.

WDTMR(0F)0FH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



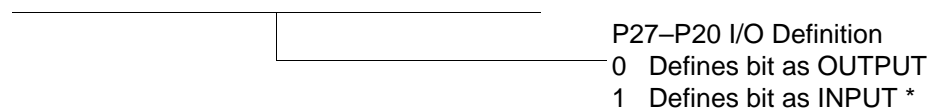
* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)

R249 IPR(F9H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

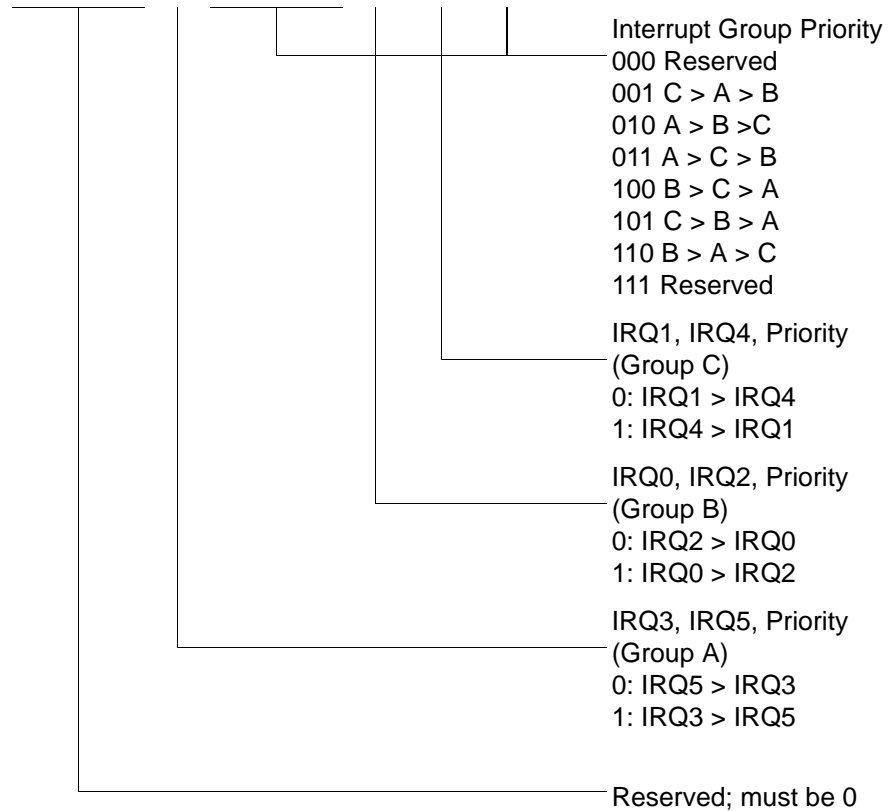


Figure 51. Interrupt Priority Register (F9H: Write Only)

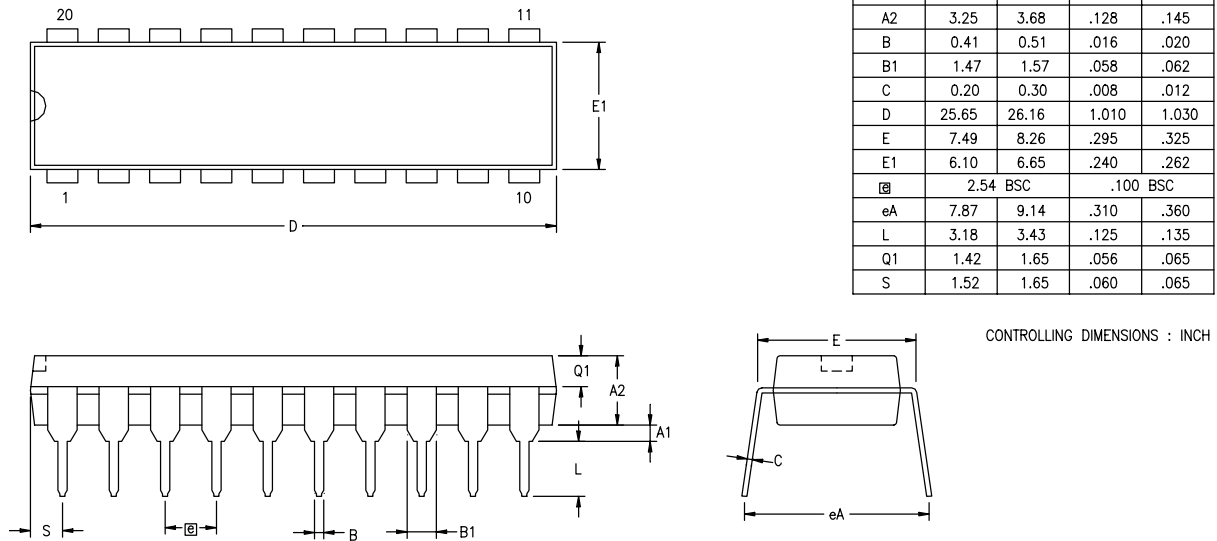


Figure 59. 20-Pin PDIP Package Diagram

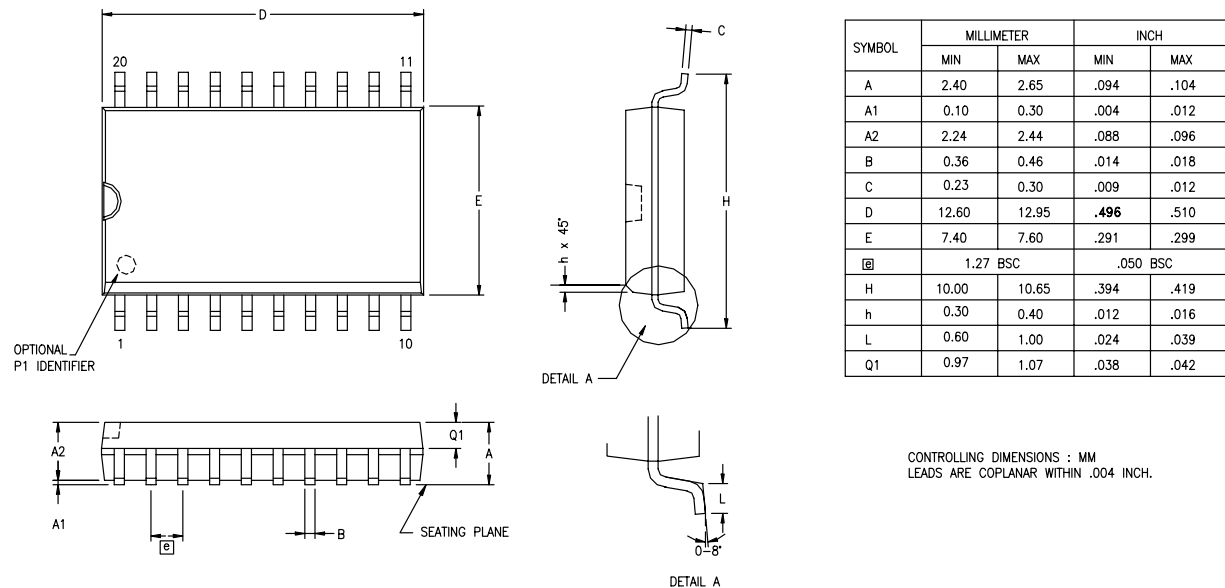
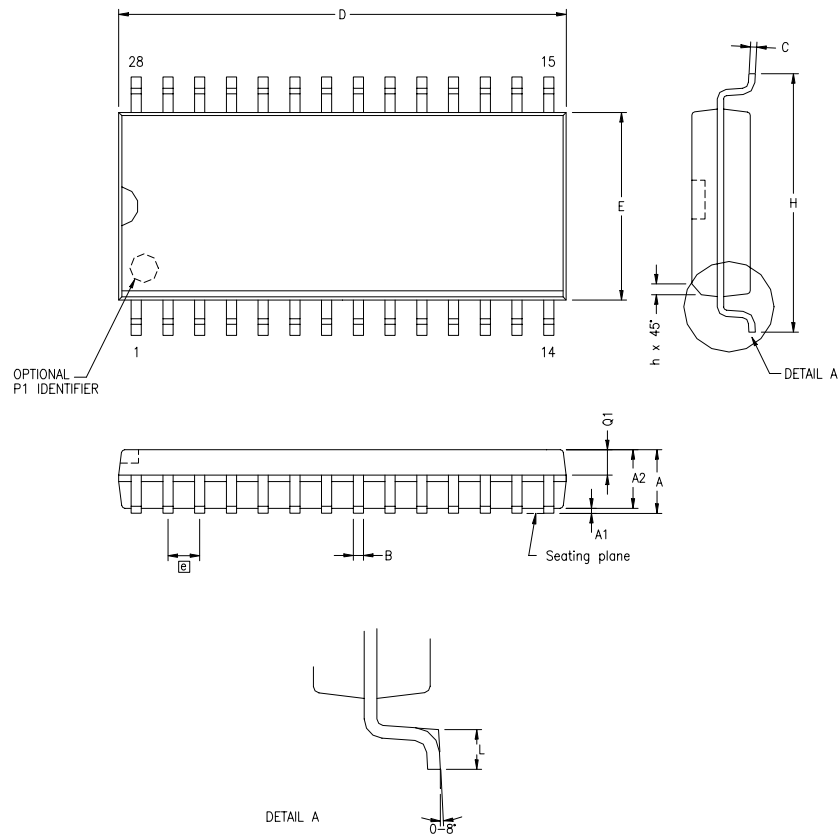


Figure 60. 20-Pin SOIC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
ⓐ	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
 LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 63. 28-Pin SOIC Package Diagram

Ordering Information

32KB Standard Temperature: 0° to +70°C			
Part Number	Description	Part Number	Description
ZGP323LSH4832C	48-pin SSOP 32K OTP	ZGP323LSS2832C	28-pin SOIC 32K OTP
ZGP323LSP4032C	40-pin PDIP 32K OTP	ZGP323LSH2032C	20-pin SSOP 32K OTP
ZGP323LSH2832C	28-pin SSOP 32K OTP	ZGP323LSP2032C	20-pin PDIP 32K OTP
ZGP323LSP2832C	28-pin PDIP 32K OTP	ZGP323LSS2032C	20-pin SOIC 32K OTP
ZGP323LSK2032E	20-pin CDIP 32K OTP	ZGP323LSK4032E	40-pin CDIP 32K OTP
		ZGP323LSK2832E	28-pin CDIP 32K OTP
32KB Extended Temperature: -40° to +105°C			
Part Number	Description	Part Number	Description
ZGP323LEH4832C	48-pin SSOP 32K OTP	ZGP323LES2832C	28-pin SOIC 32K OTP
ZGP323LEP4032C	40-pin PDIP 32K OTP	ZGP323LEH2032C	20-pin SSOP 32K OTP
ZGP323LEH2832C	28-pin SSOP 32K OTP	ZGP323LEP2032C	20-pin PDIP 32K OTP
ZGP323LEP2832C	28-pin PDIP 32K OTP	ZGP323LES2032C	20-pin SOIC 32K OTP
32KB Automotive Temperature: -40° to +125°C			
Part Number	Description	Part Number	Description
ZGP323LAH4832C	48-pin SSOP 32K OTP	ZGP323LAS2832C	28-pin SOIC 32K OTP
ZGP323LAP4032C	40-pin PDIP 32K OTP	ZGP323LAH2032C	20-pin SSOP 32K OTP
ZGP323LAH2832C	28-pin SSOP 32K OTP	ZGP323LAP2032C	20-pin PDIP 32K OTP
ZGP323LAP2832C	28-pin PDIP 32K OTP	ZGP323LAS2032C	20-pin SOIC 32K OTP
Note: Replace C with G for Lead-Free Packaging			

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