# Zilog - ZGP323LAS2804C00TR Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323las2804c00tr |

- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

**Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 KΩ ±50% at $V_{CC}$=3 V and 450 KΩ ±50% at $V_{CC}$=2 V.

## General Description

The Z8 GP™ OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z8 GP™ OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

**Note:** All signals with an overline, "$\overline{\ }$", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.

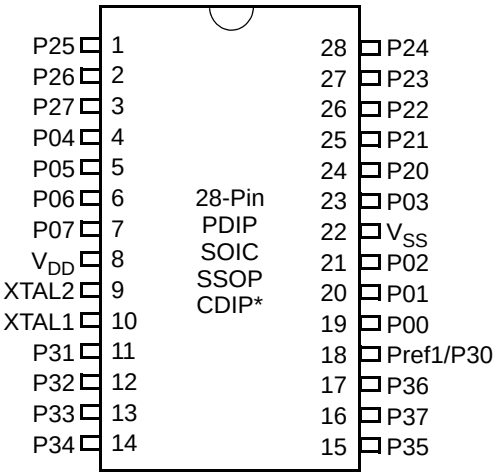



**Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration**

**Table 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification**

| Pin | Symbol | Direction | Description |
|---|---|---|---|
| 1-3 | P25-P27 | Input/Output | Port 2, Bits 5,6,7 |
| 4-7 | P04-P07 | Input/Output | Port 0, Bits 4,5,6,7 |
| 8 | $V_{DD}$ | | Power supply |
| 9 | XTAL2 | Output | Crystal, oscillator clock |
| 10 | XTAL1 | Input | Crystal, oscillator clock |
| 11-13 | P31-P33 | Input | Port 3, Bits 1,2,3 |
| 14 | P34 | Output | Port 3, Bit 4 |
| 15 | P35 | Output | Port 3, Bit 5 |
| 16 | P37 | Output | Port 3, Bit 7 |
| 17 | P36 | Output | Port 3, Bit 6 |
| 18 | Pref1/P30<br>Port 3 Bit 0 | Input | Analog ref input; connect to $V_{CC}$ if not used<br>Input for Pref1/P30 |
| 19-21 | P00-P02 | Input/Output | Port 0, Bits 0,1,2 |
| 22 | $V_{SS}$ | | Ground |
| 23 | P03 | Input/Output | Port 0, Bit 3 |
| 24-28 | P20-P24 | Input/Output | Port 2, Bits 0-4 |

**Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

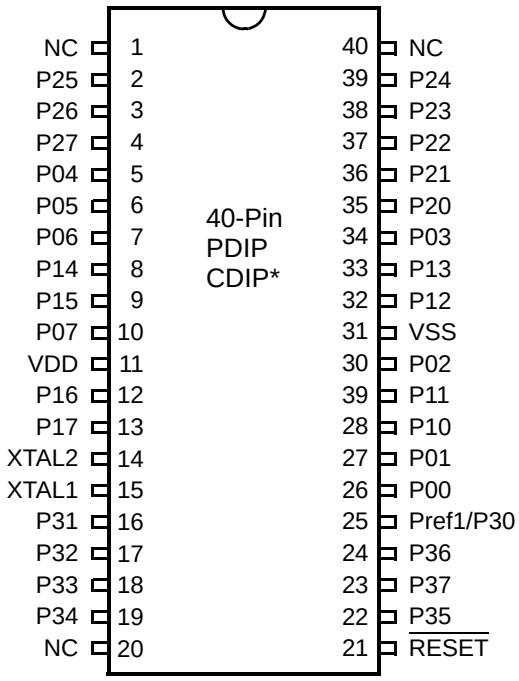



**Figure 5. 40-Pin PDIP/CDIP* Pin Configuration**

**Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

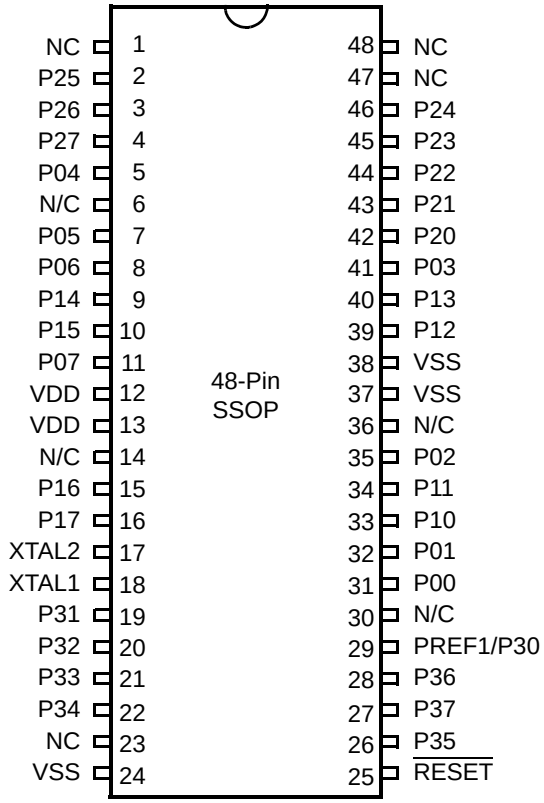



**Figure 6. 48-Pin SSOP Pin Configuration**

**Table 5. 40- and 48-Pin Configuration**

| 40-Pin PDIP/CDIP* # | 48-Pin SSOP # | Symbol |
|---|---|---|
| 26 | 31 | P00 |
| 27 | 32 | P01 |
| 30 | 35 | P02 |
| 34 | 41 | P03 |
| 5 | 5 | P04 |
| 6 | 7 | P05 |
| 7 | 8 | P06 |
| 10 | 11 | P07 |
| 28 | 33 | P10 |
| 29 | 34 | P11 |
| 32 | 39 | P12 |

# Capacitance

Table 7 lists the capacitances.

**Table 7. Capacitance**

| Parameter | Maximum |
|---|---|
| Input capacitance | 12pF |
| Output capacitance | 12pF |
| I/O capacitance | 12pF |
| Note: $T_A$ = 25° C, $V_{CC}$ = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND | |

# DC Characteristics

**Table 8. DC Characteristics**

| | | | $T_A$= 0°C to +70°C | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | **Notes** |
| $V_{CC}$ | Supply Voltage | | 2.0 | | 3.6 | V | See Note 5 | 5 |
| $V_{CH}$ | Clock Input High Voltage | 2.0-3.6 | 0.8 | | $V_{CC}$+0.3 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 2.0-3.6 | $V_{SS}$–0.3 | | 0.5 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 2.0-3.6 | 0.7 $V_{CC}$ | | $V_{CC}$+0.3 | V | | |
| $V_{IL}$ | Input Low Voltage | 2.0-3.6 | $V_{SS}$–0.3 | | 0.2 $V_{CC}$ | V | | |
| $V_{OH1}$ | Output High Voltage | 2.0-3.6 | $V_{CC}$–0.4 | | | V | $I_{OH}$ = –0.5mA | |
| $V_{OH2}$ | Output High Voltage (P36, P37, P00, P01) | 2.0-3.6 | $V_{CC}$–0.8 | | | V | $I_{OH}$ = –7mA | |
| $V_{OL1}$ | Output Low Voltage | 2.0-3.6 | | | 0.4 | V | $I_{OL}$ = 1.0mA<br>$I_{OL}$ = 4.0mA | |
| $V_{OL2}$ | Output Low Voltage (P00, P01, P36, P37) | 2.0-3.6 | | | 0.8 | V | $I_{OL}$ = 10mA | |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 2.0-3.6 | | | 25 | mV | | |
| $V_{REF}$ | Comparator Reference Voltage | 2.0-3.6 | 0 | | $V_{DD}$ -1.75 | V | | |
| $I_{IL}$ | Input Leakage | 2.0-3.6 | –1 | | 1 | µA | $V_{IN}$ = 0V, $V_{CC}$<br>Pull-ups disabled | |
| $I_{OL}$ | Output Leakage | 2.0-3.6 | –1 | | 1 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{CC}$ | Supply Current | 2.0<br>3.6 | | | 10<br>15 | mA<br>mA | at 8.0 MHz<br>at 8.0 MHz | 1, 2<br>1, 2 |

### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## $\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP™ asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP™ does not assert the $\overline{\text{RESET}}$ pin when under VBO.

**Note:** The external Reset does not initiate an exit from STOP mode.

# Functional Description

This device incorporates special functions to enhance the Z8®, functionality in consumer and battery-operated applications.

## Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

## RAM

This device features 256B of RAM. See Figure 14.

**Table 12. CTR0(D)00H Counter/Timer8 Control Register (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Counter_INT_Mask | ------1- | R/W | 0<br>1 | Disable Time-Out Interrupt<br>Enable Time-Out Interrupt |
| P34_Out | -------0 | R/W | 0*<br>1 | P34 as Port Output<br>T8 Output on P34 |

**Note:**
*Indicates the value upon Power-On Reset.

### T8 Enable

This field enables T8 when set (written) to 1.

### Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

### Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.

**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

**Note:** Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

### T8 Clock

This bit defines the frequency of the input signal to T8.

### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows $V_{DD}$ and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from $V_{BO}$ Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

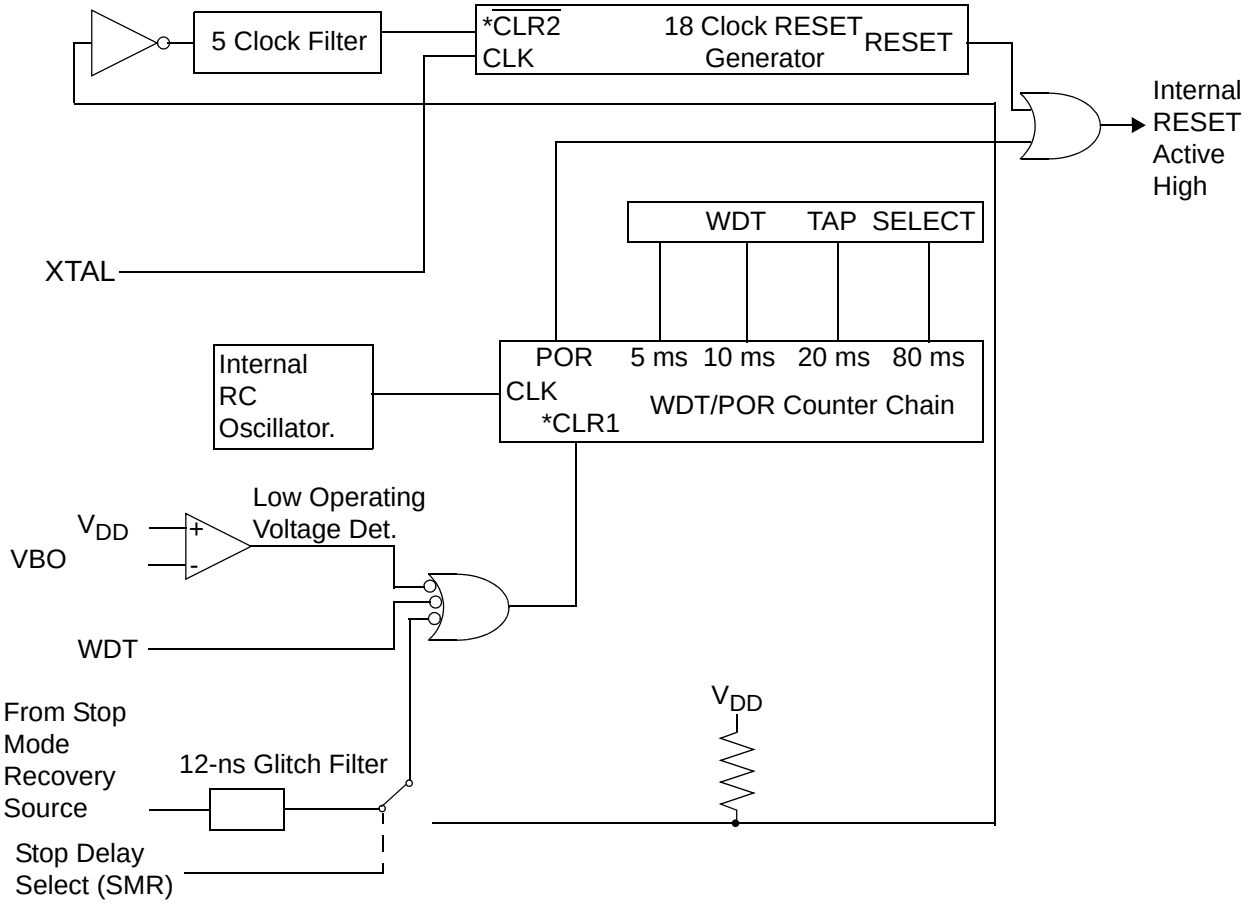
This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μA or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

**Table 20. Watch-Dog Timer Time Select**

| D1 | D0 | Timeout of Internal RC-Oscillator |
|---|---|---|
| 0 | 0 | 5ms min. |
| 0 | 1 | 10ms min. |
| 1 | 0 | 20ms min. |
| 1 | 1 | 80ms min. |

### WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.




* CLR1 and $\overline{CLR2}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

**Figure 38. Resets and WDT**

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

**Table 21. EPROM Selectable Options**

| | |
|---|---|
| Port 00–03 Pull-Ups | On/Off |
| Port 04–07 Pull-Ups | On/Off |
| Port 10–13 Pull-Ups | On/Off |
| Port 14–17 Pull-Ups | On/Off |
| Port 20–27 Pull-Ups | On/Off |
| EPROM Protection | On/Off |
| Watch-Dog Timer at Power-On Reset | On/Off |

### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the $V_{DD}$ is at the required level for correct operation of the device. Reset is globally driven when $V_{DD}$ falls below $V_{BO}$. A small drop in $V_{DD}$ causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the $V_{DD}$ is allowed to stay above $V_{RAM}$, the RAM content is preserved. When the power level is returned to above $V_{BO}$, the device performs a POR and functions normally.

CTR1(0D)01H

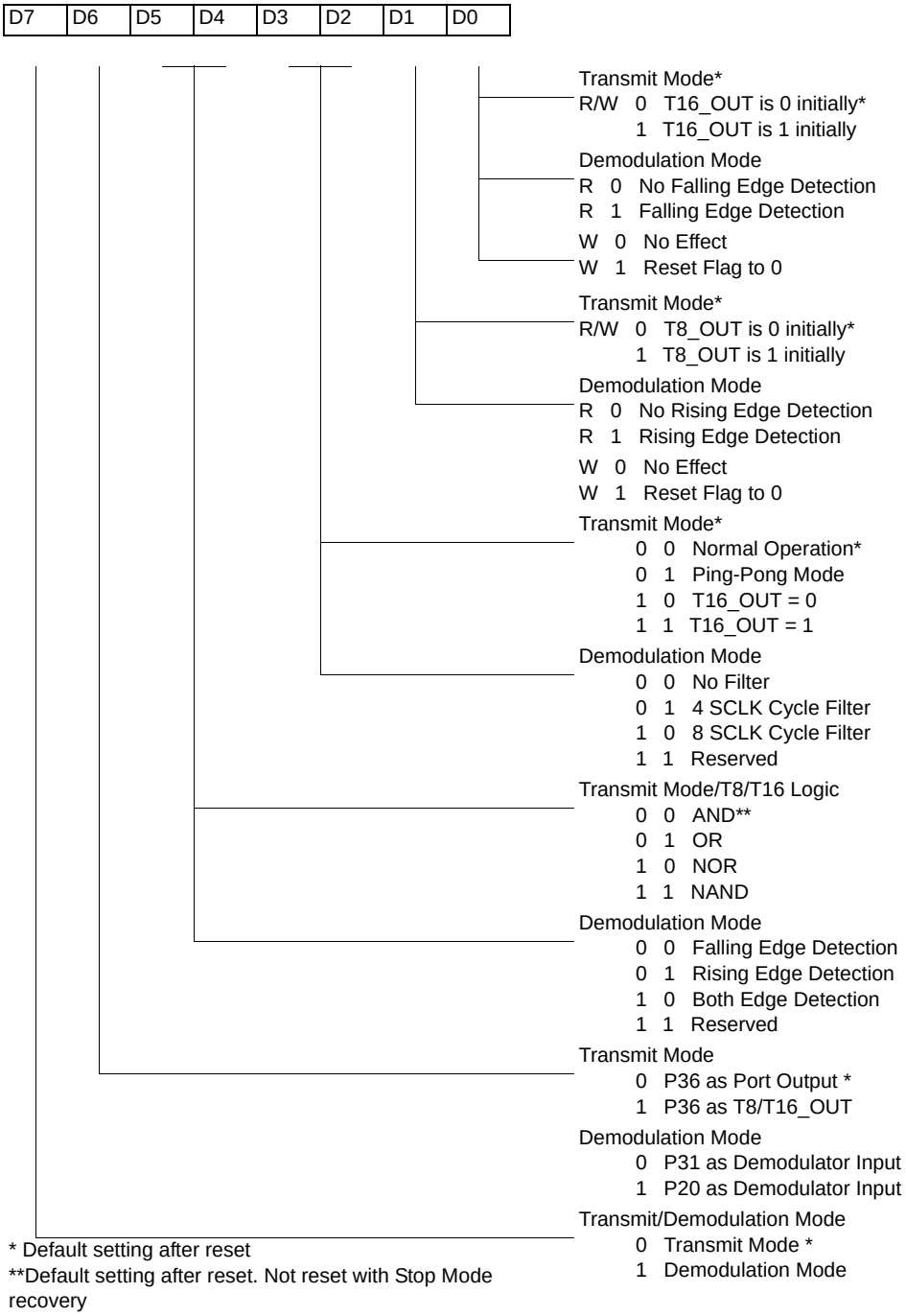



**Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)**

CTR2(0D)02H

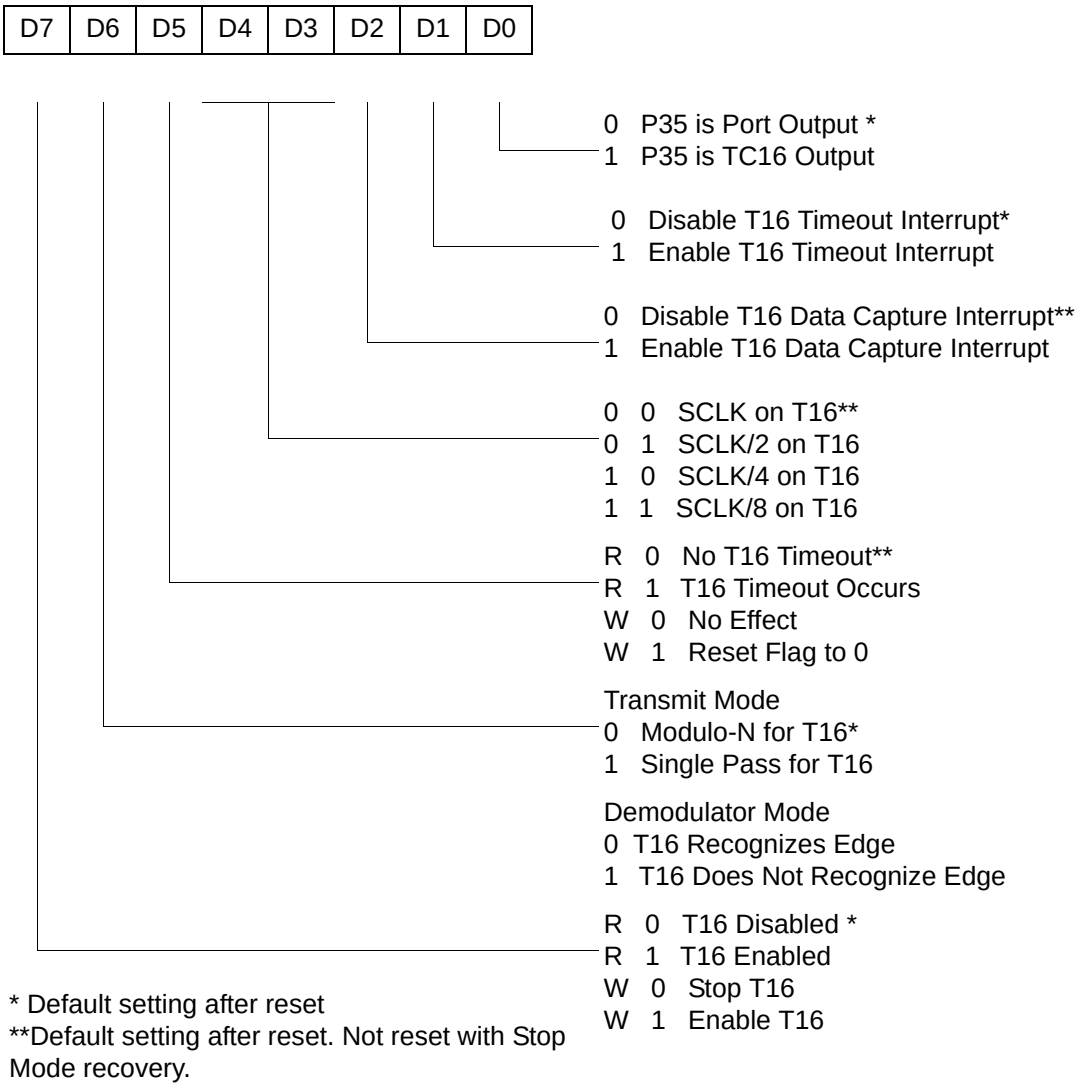
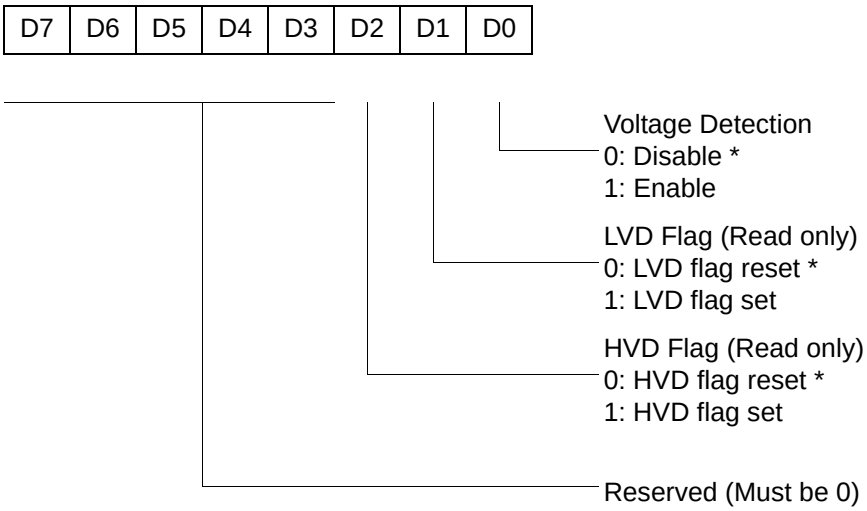



**Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

LVD(0D)0CH




* Default

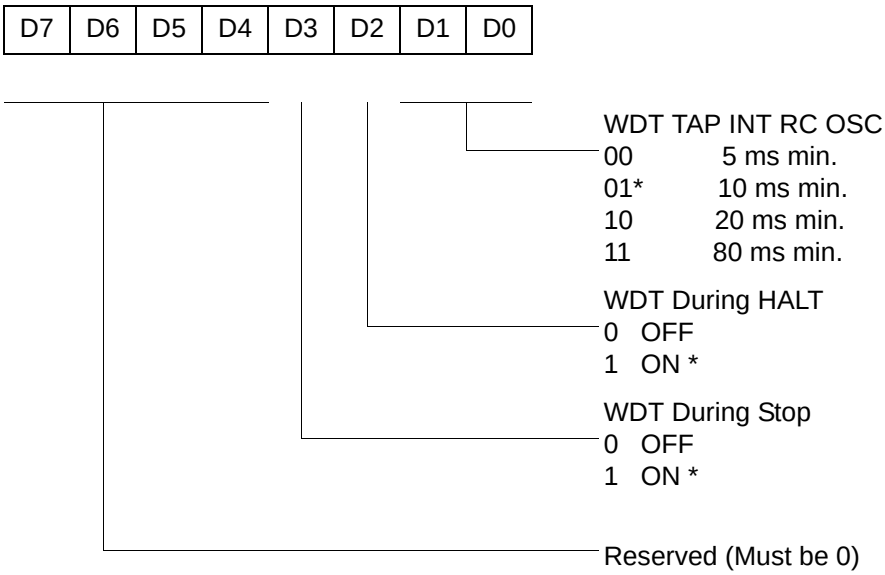
**Figure 43. Voltage Detection Register**

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

## Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.

WDTMR(0F)0FH

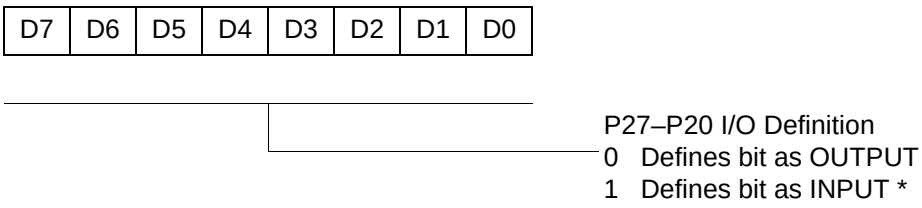



* Default setting after reset

**Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)**

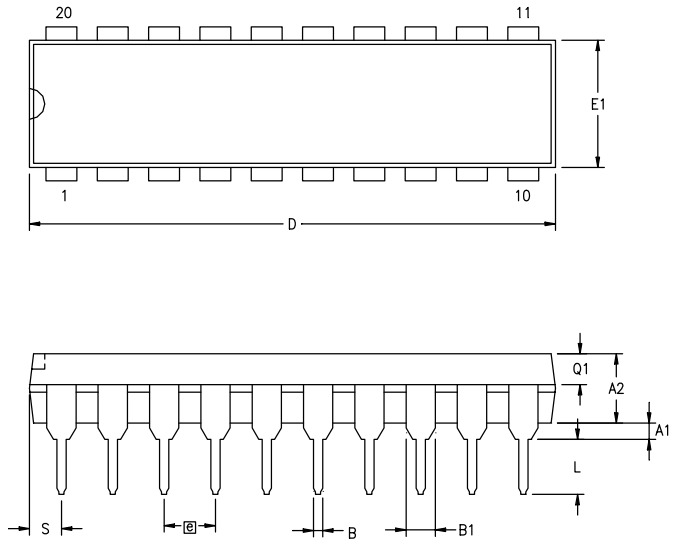
# Standard Control Registers

R246 P2M(F6H)




* Default setting after reset

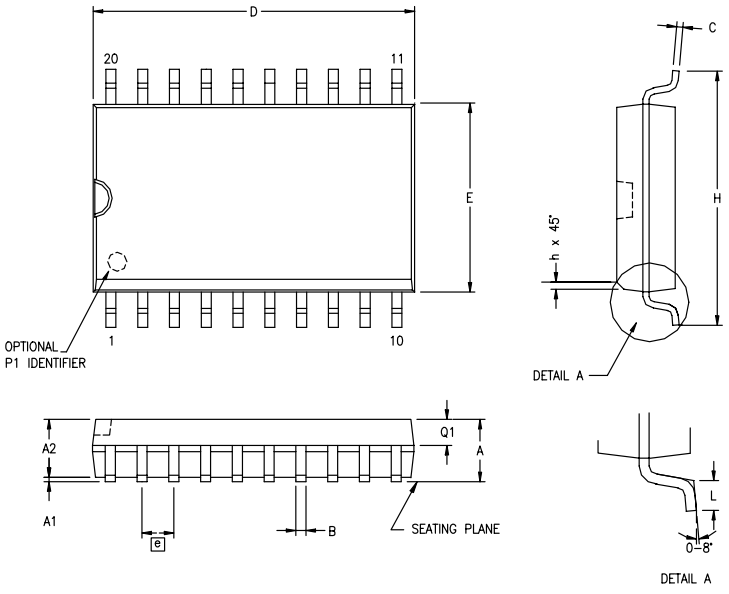
**Figure 48. Port 2 Mode Register (F6H: Write Only)**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.38 | 0.81 | .015 | .032 |
| A2 | 3.25 | 3.68 | .128 | .145 |
| B | 0.41 | 0.51 | .016 | .020 |
| B1 | 1.47 | 1.57 | .058 | .062 |
| C | 0.20 | 0.30 | .008 | .012 |
| D | 25.65 | 26.16 | 1.010 | 1.030 |
| E | 7.49 | 8.26 | .295 | .325 |
| E1 | 6.10 | 6.65 | .240 | .262 |
| e | 2.54 BSC | | .100 BSC | |
| eA | 7.87 | 9.14 | .310 | .360 |
| L | 3.18 | 3.43 | .125 | .135 |
| Q1 | 1.42 | 1.65 | .056 | .065 |
| S | 1.52 | 1.65 | .060 | .065 |

CONTROLLING DIMENSIONS : INCH

**Figure 59. 20-Pin PDIP Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.65 | .094 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.24 | 2.44 | .088 | .096 |
| B | 0.36 | 0.46 | .014 | .018 |
| C | 0.23 | 0.30 | .009 | .012 |
| D | 12.60 | 12.95 | **.496** | .510 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 BSC | | .050 BSC | |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.30 | 0.40 | .012 | .016 |
| L | 0.60 | 1.00 | .024 | .039 |
| Q1 | 0.97 | 1.07 | .038 | .042 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 60. 20-Pin SOIC Package Diagram**

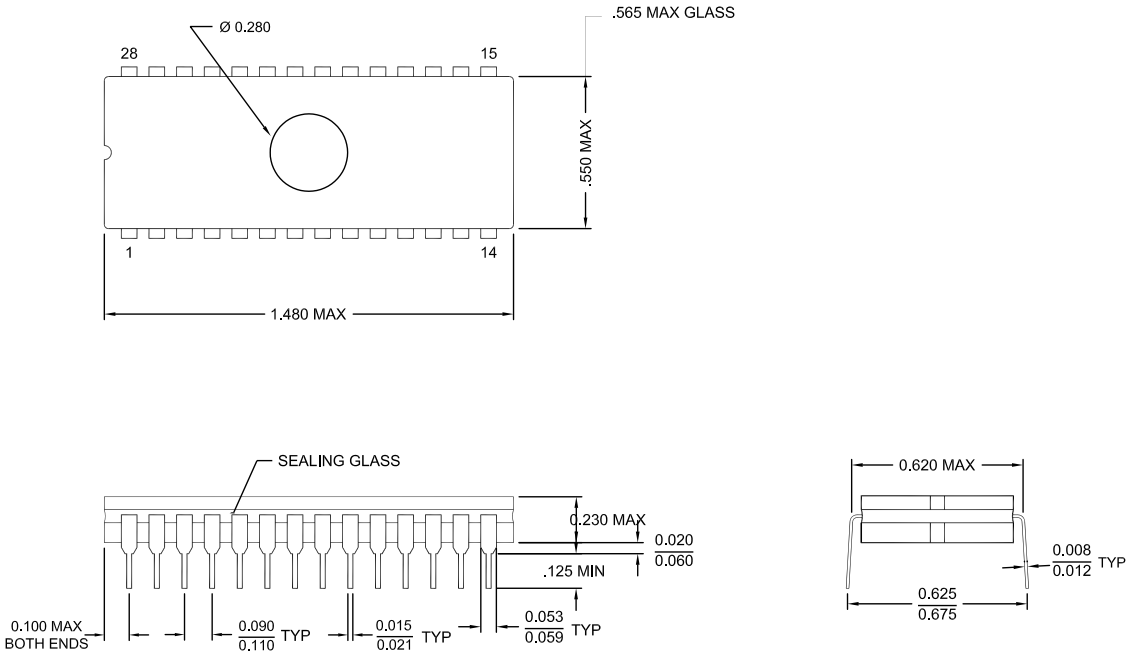



**Figure 62. 28-Pin CDIP Package**

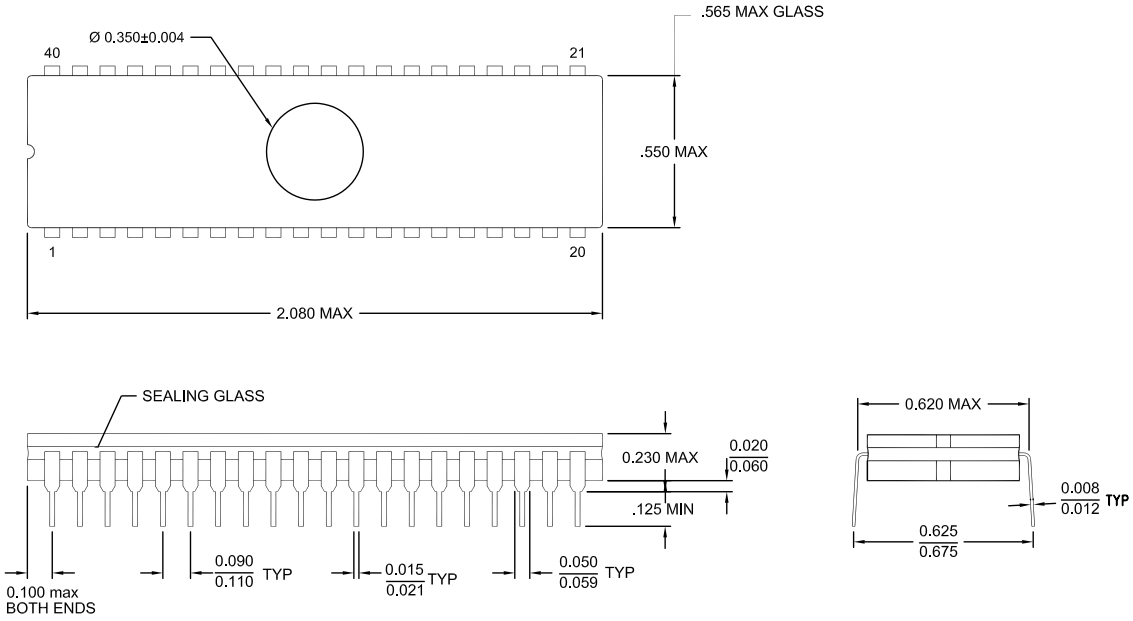
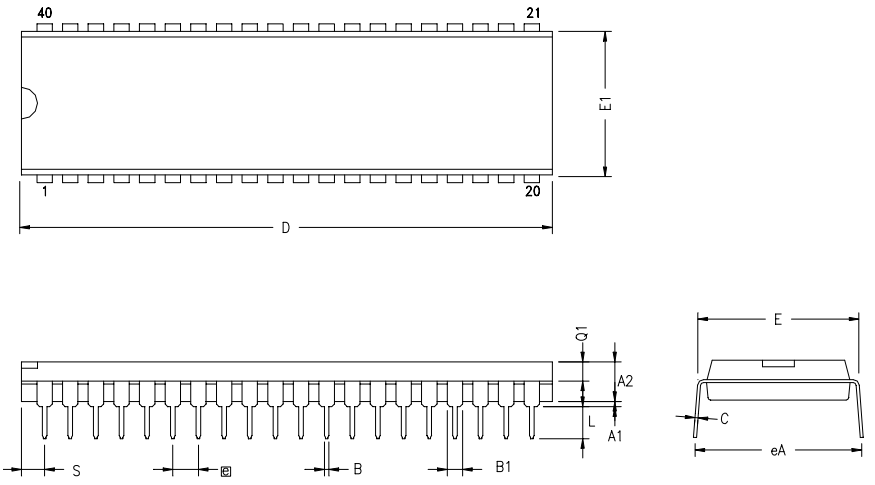



**Figure 66. 40-Pin CDIP Package**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 1.02 | .020 | .040 |
| A2 | 3.18 | 3.94 | .125 | .155 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.02 | 1.52 | .040 | .060 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 52.07 | 52.58 | 2.050 | 2.070 |
| E | 15.24 | 15.75 | .600 | .620 |
| E1 | 13.59 | 14.22 | .535 | .560 |
| e | 2.54 TYP | | .100 TYP | |
| eA | 15.49 | 16.76 | .610 | .660 |
| L | 3.05 | 3.81 | .120 | .150 |
| Q1 | 1.40 | 1.91 | .055 | .075 |
| S | 1.52 | 2.29 | .060 | .090 |

CONTROLLING DIMENSIONS : INCH

**Figure 67. 40-Pin PDIP Package Diagram**

# Ordering Information

| 32KB Standard Temperature: 0° to +70°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LSH4832C | 48-pin SSOP 32K OTP | ZGP323LSS2832C | 28-pin SOIC 32K OTP |
| ZGP323LSP4032C | 40-pin PDIP 32K OTP | ZGP323LSH2032C | 20-pin SSOP 32K OTP |
| ZGP323LSH2832C | 28-pin SSOP 32K OTP | ZGP323LSP2032C | 20-pin PDIP 32K OTP |
| ZGP323LSP2832C | 28-pin PDIP 32K OTP | ZGP323LSS2032C | 20-pin SOIC 32K OTP |
| ZGP323LSK2032E | 20-pin CDIP 32K OTP | ZGP323LSK4032E | 40-pin CDIP 32K OTP |
| | | ZGP323LSK2832E | 28-pin CDIP 32K OTP |

| 32KB Extended Temperature: -40° to +105°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LEH4832C | 48-pin SSOP 32K OTP | ZGP323LES2832C | 28-pin SOIC 32K OTP |
| ZGP323LEP4032C | 40-pin PDIP 32K OTP | ZGP323LEH2032C | 20-pin SSOP 32K OTP |
| ZGP323LEH2832C | 28-pin SSOP 32K OTP | ZGP323LEP2032C | 20-pin PDIP 32K OTP |
| ZGP323LEP2832C | 28-pin PDIP 32K OTP | ZGP323LES2032C | 20-pin SOIC 32K OTP |

| 32KB Automotive Temperature: -40° to +125°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LAH4832C | 48-pin SSOP 32K OTP | ZGP323LAS2832C | 28-pin SOIC 32K OTP |
| ZGP323LAP4032C | 40-pin PDIP 32K OTP | ZGP323LAH2032C | 20-pin SSOP 32K OTP |
| ZGP323LAH2832C | 28-pin SSOP 32K OTP | ZGP323LAP2032C | 20-pin PDIP 32K OTP |
| ZGP323LAP2832C | 28-pin PDIP 32K OTP | ZGP323LAS2032C | 20-pin SOIC 32K OTP |
| | | | |

Note: Replace C with G for Lead-Free Packaging

| 4KB Standard Temperature: 0° to +70°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LSH4804C | 48-pin SSOP 4K OTP | ZGP323LSS2804C | 28-pin SOIC 4K OTP |
| ZGP323LSP4004C | 40-pin PDIP 4K OTP | ZGP323LSH2004C | 20-pin SSOP 4K OTP |
| ZGP323LSH2804C | 28-pin SSOP 4K OTP | ZGP323LSP2004C | 20-pin PDIP 4K OTP |
| ZGP323LSP2804C | 28-pin PDIP 4K OTP | ZGP323LSS2004C | 20-pin SOIC 4K OTP |

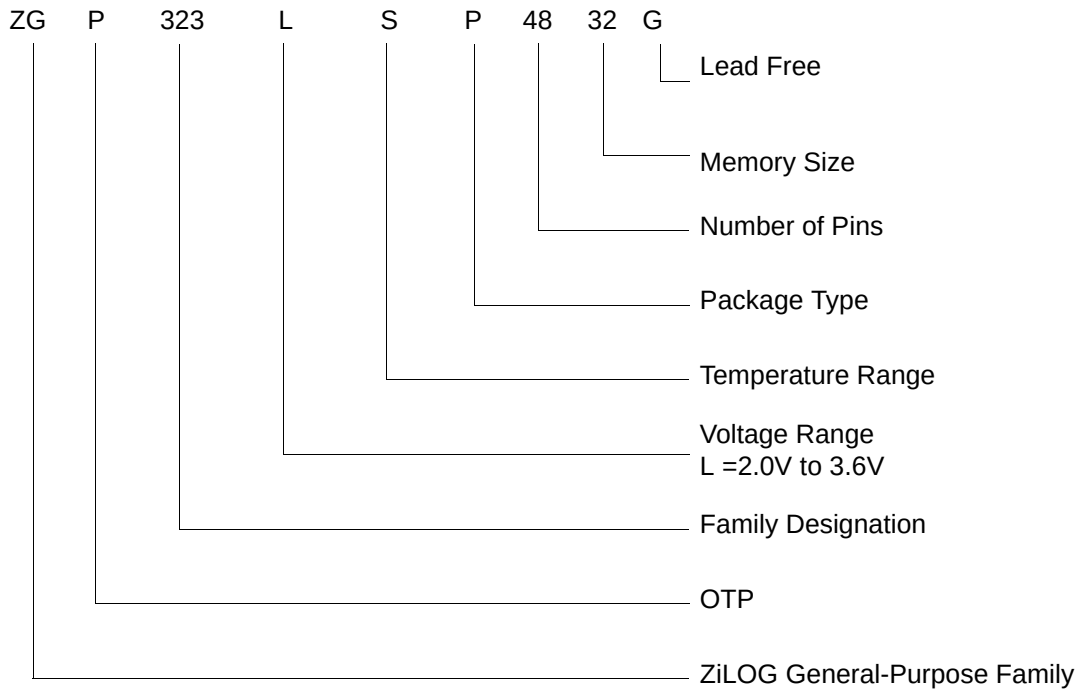
| 4KB Extended Temperature: -40° to +105°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LEH4804C | 48-pin SSOP 4K OTP | ZGP323LES2804C | 28-pin SOIC 4K OTP |
| ZGP323LEP4004C | 40-pin PDIP 4K OTP | ZGP323LEH2004C | 20-pin SSOP 4K OTP |
| ZGP323LEH2804C | 28-pin SSOP 4K OTP | ZGP323LEP2004C | 20-pin PDIP 4K OTP |
| ZGP323LEP2804C | 28-pin PDIP 4K OTP | ZGP323LES2004C | 20-pin SOIC 4K OTP |

| 4KB Automotive Temperature: -40° to +125°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LAH4804C | 48-pin SSOP 4K OTP | ZGP323LAS2804C | 28-pin SOIC 4K OTP |
| ZGP323LAP4004C | 40-pin PDIP 4K OTP | ZGP323LAH2004C | 20-pin SSOP 4K OTP |
| ZGP323LAH2804C | 28-pin SSOP 4K OTP | ZGP323LAP2004C | 20-pin PDIP 4K OTP |
| ZGP323LAP2804C | 28-pin PDIP 4K OTP | ZGP323LAS2004C | 20-pin SOIC 4K OTP |

Note: Replace C with G for Lead-Free Packaging

| Additional Components | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323ICE01ZEM | Emulator/programmer | ZGP32300100ZPR | Programming System |

**Example**


ZG
P
323
L
S
P
48
32
G
Lead Free
Memory Size
Number of Pins
Package Type
Temperature Range
Voltage Range
L =2.0V to 3.6V
Family Designation
OTP
ZiLOG General-Purpose Family