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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323las2816c">https://www.e-xfl.com/product-detail/zilog/zgp323las2816c</a>



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- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

► **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K $\Omega$   $\pm$ 50% at  $V_{CC}$ =3 V and 450 K $\Omega$   $\pm$ 50% at  $V_{CC}$ =2 V.

## General Description

The Z8 GP™ OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

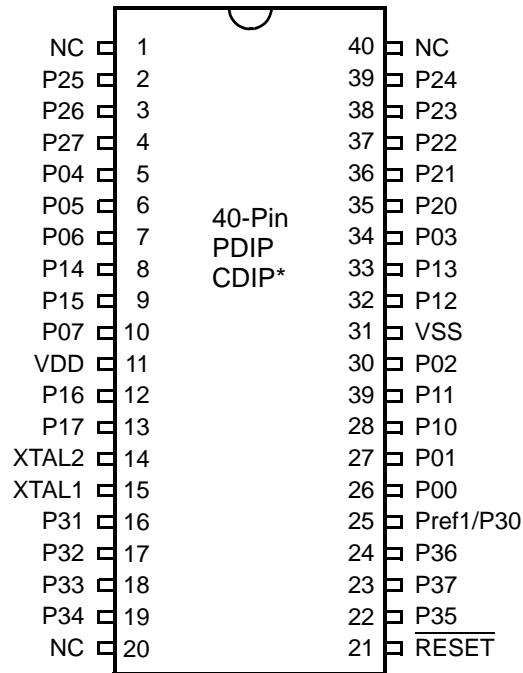
The Z8 GP™ OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, " $\overline{\phantom{x}}$ ", are active Low. For example,  $\overline{B/W}$ , in which WORD is active Low, and  $\overline{B/W}$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.



**Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration**

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

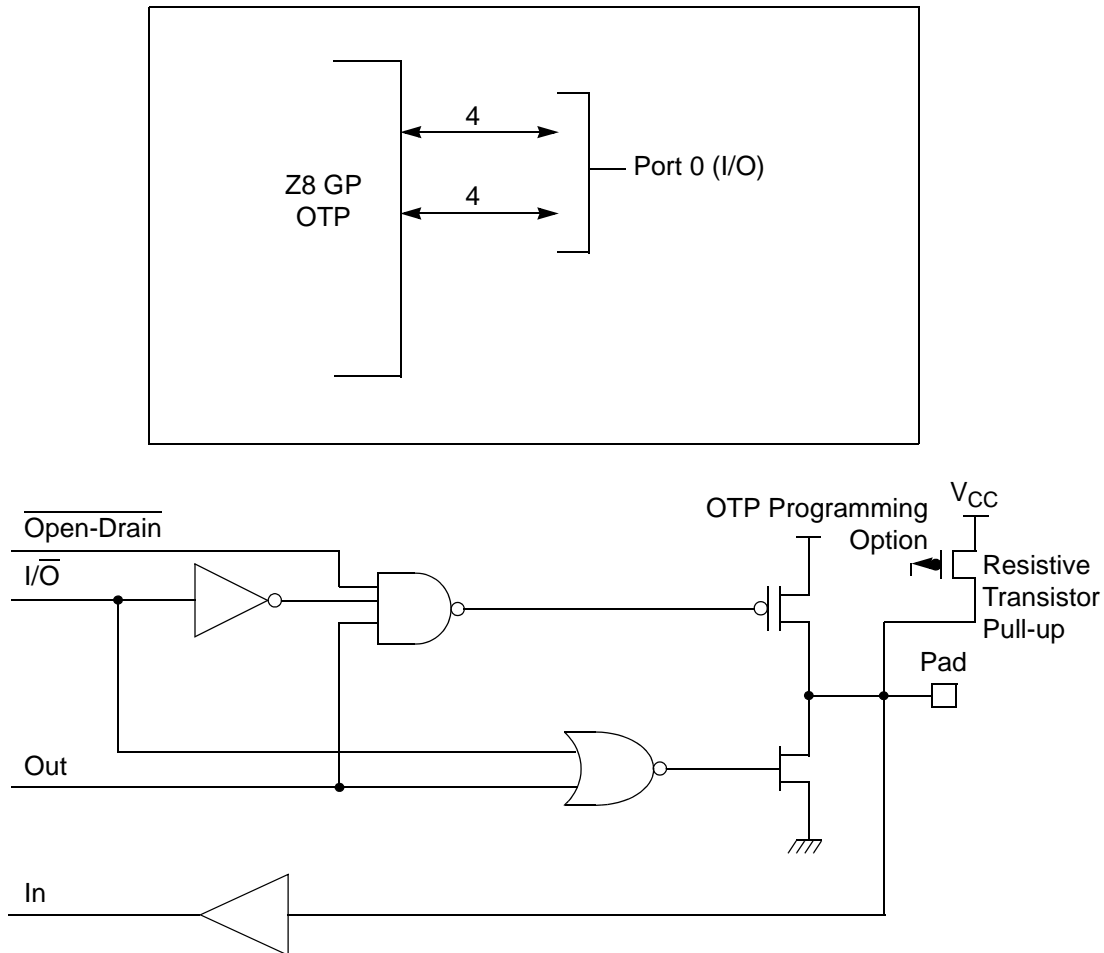
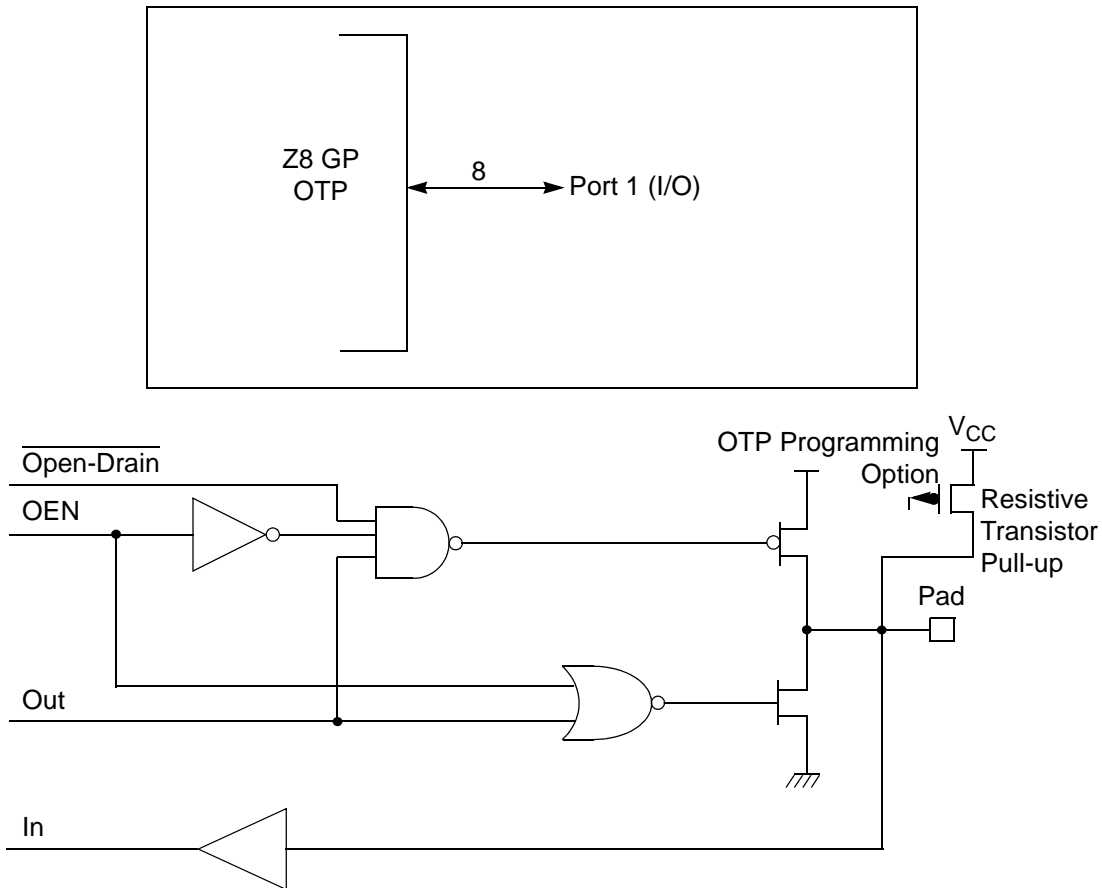


Figure 9. Port 0 Configuration

### Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to be input following an SMR.



**Figure 10. Port 1 Configuration**

## Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).

### T8/T16\_Logic/Edge \_Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

### Transmit\_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

### Initial\_T8\_Out/Rising\_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

### Initial\_T16 Out/Falling \_Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16\_OUT.

### CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 14 lists and briefly describes the fields for this register.

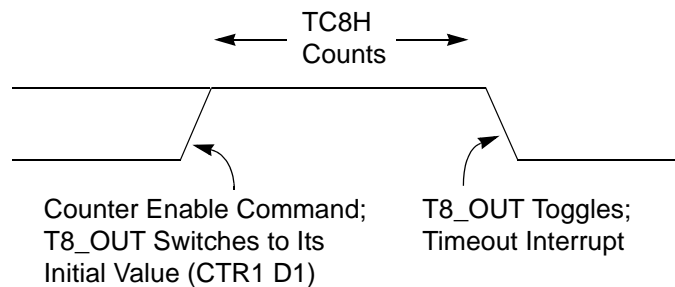
► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF<sub>h</sub> is not a timeout condition.

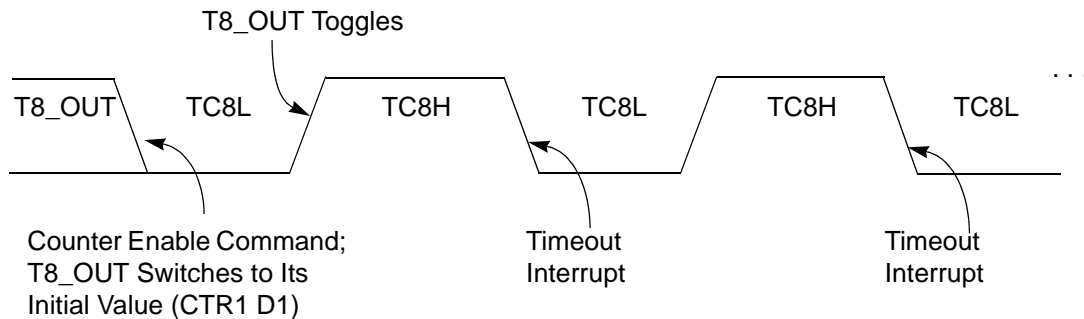


**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.



**Figure 21. T8\_OUT in Single-Pass Mode**



**Figure 22. T8\_OUT in Modulo-N Mode**

### T8 Demodulation Mode

The user must program TC8L and TC8H to FF<sub>h</sub>. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

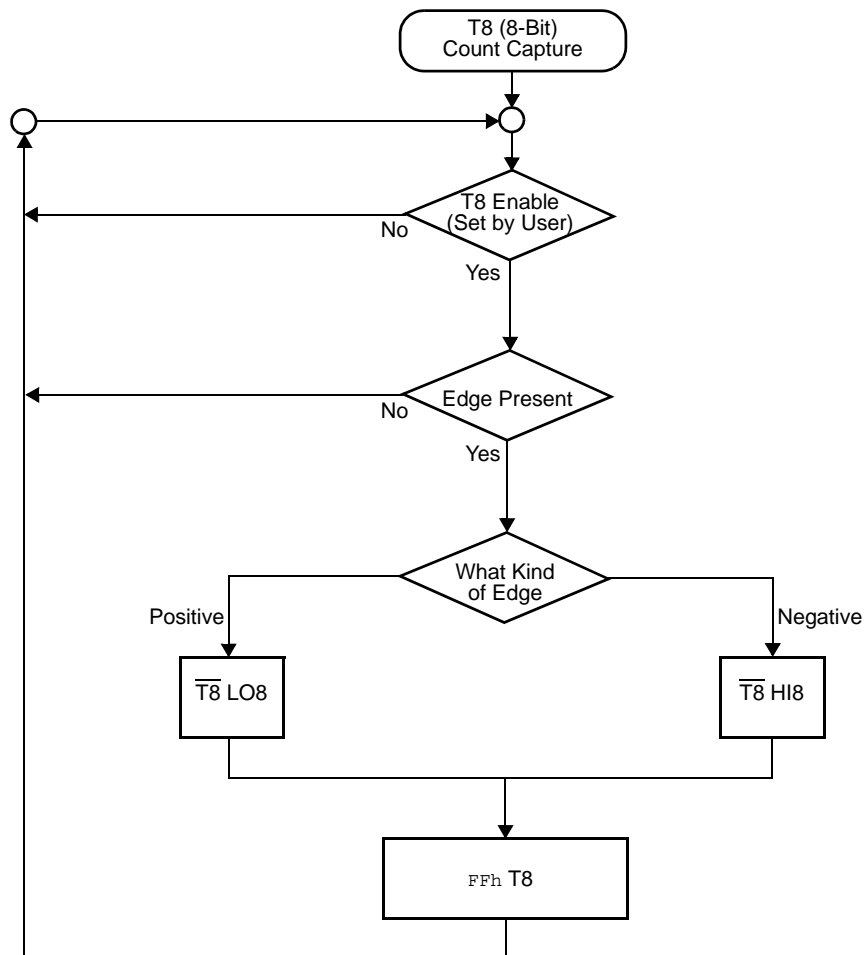


Figure 23. Demodulation Mode Count Capture Flowchart

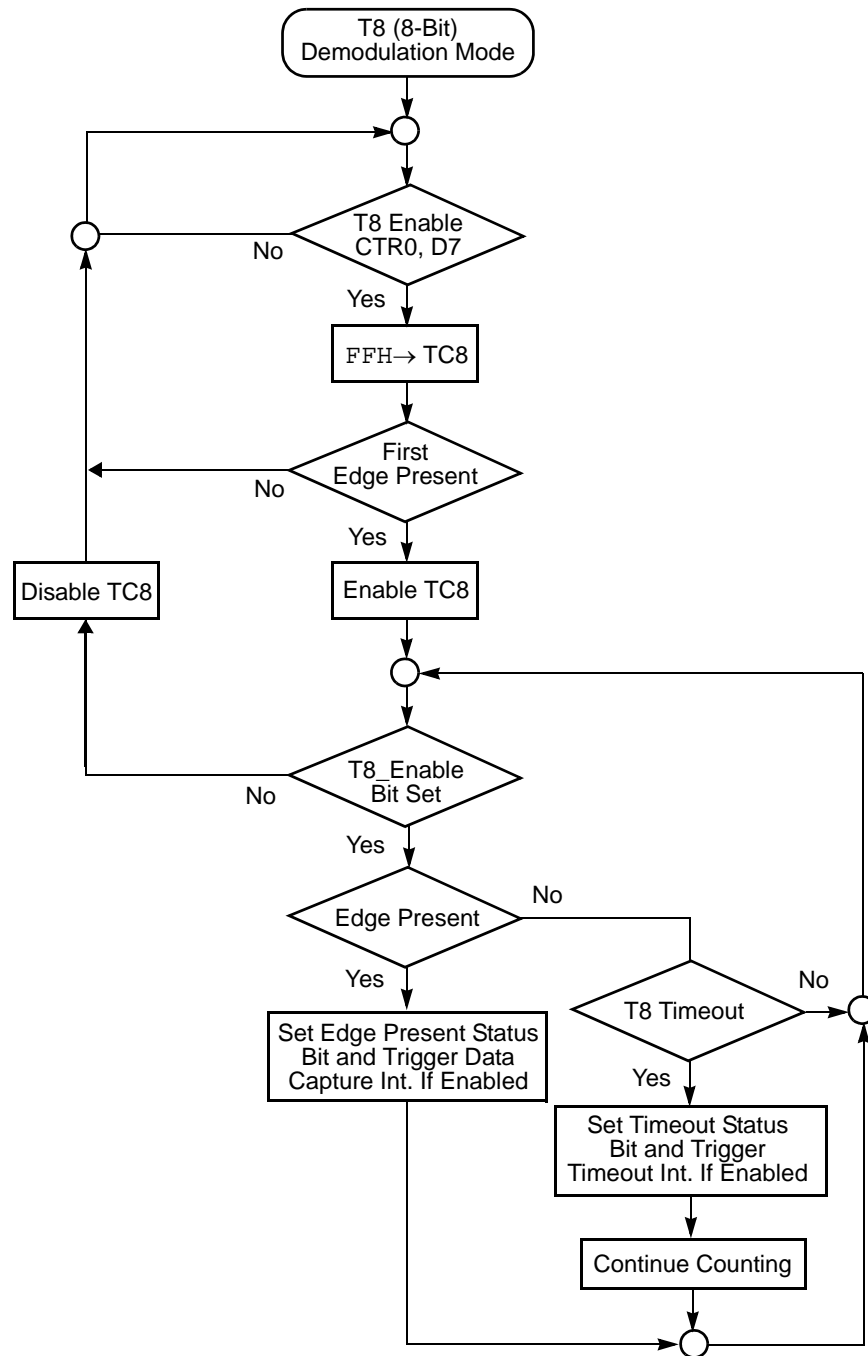
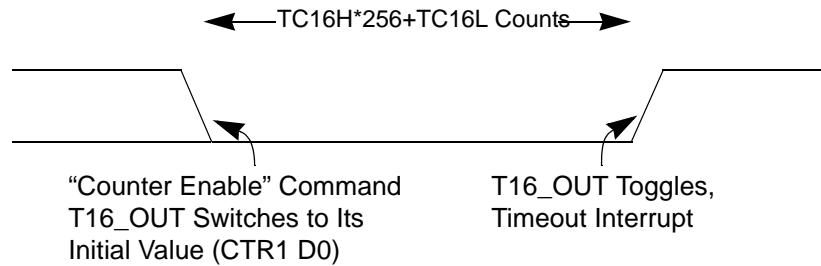


Figure 24. Demodulation Mode Flowchart

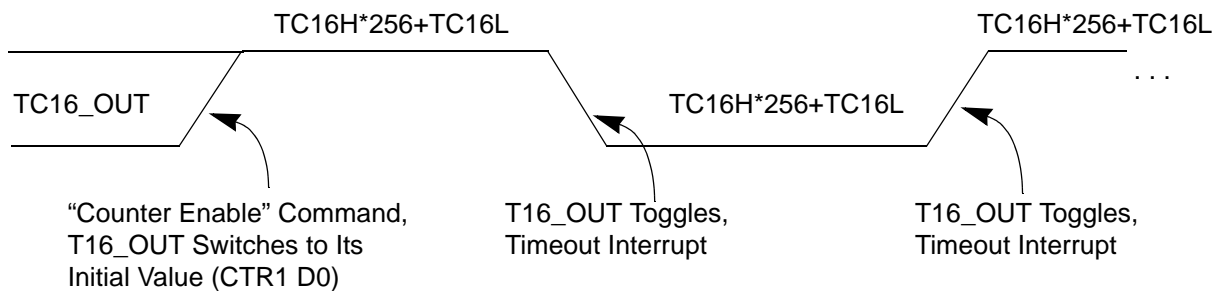


**Caution:**

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE<sub>H</sub>. Transition from 0 to FFFF<sub>H</sub> is not a timeout condition.



**Figure 26. T16\_OUT in Single-Pass Mode**



**Figure 27. T16\_OUT in Modulo-N Mode**

**T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FF<sub>H</sub>. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

**If D6 of CTR2 Is 0**

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF<sub>H</sub> and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

### **Port 0 Output Mode (D2)**

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### **Stop-Mode Recovery Register (SMR)**

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 57) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

**Table 21. EPROM Selectable Options**

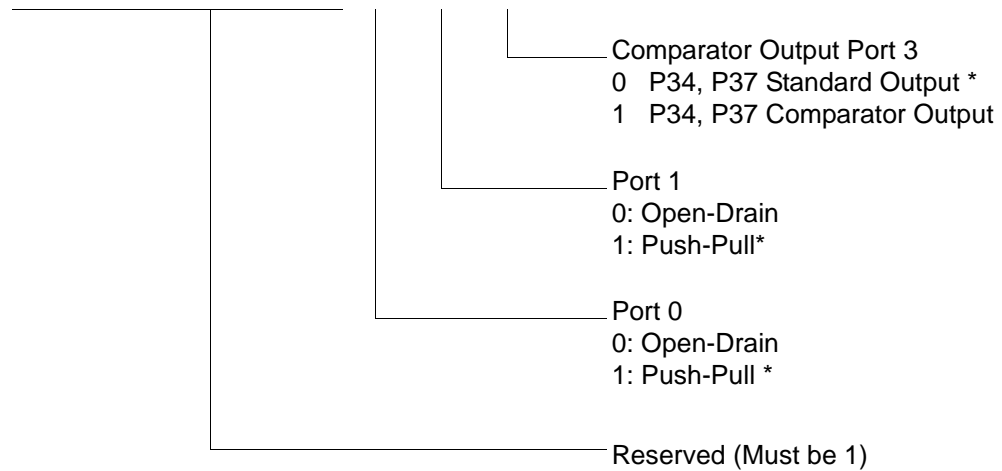
Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the  $V_{DD}$  is at the required level for correct operation of the device. Reset is globally driven when  $V_{DD}$  falls below  $V_{BO}$ . A small drop in  $V_{DD}$  causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the  $V_{DD}$  is allowed to stay above  $V_{RAM}$ , the RAM content is preserved. When the power level is returned to above  $V_{BO}$ , the device performs a POR and functions normally.

PCON(0F)00H

D7	D6	D5	D4	D3	D2	D1	D0
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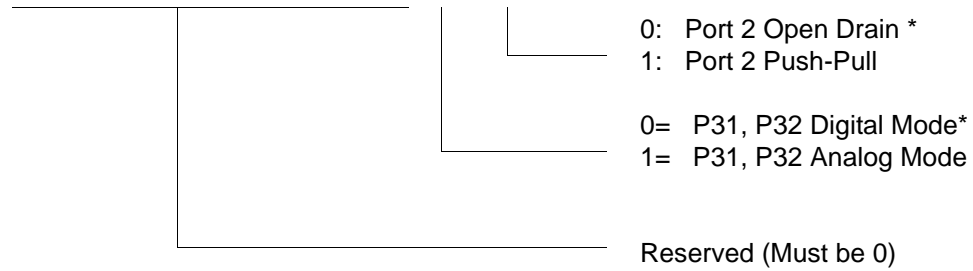


\* Default setting after reset

**Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)**

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset. Not reset with Stop Mode recovery.

**Figure 49. Port 3 Mode Register (F7H: Write Only)**

R249 IPR(F9H)

D7	D6	D5	D4	D3	D2	D1	D0
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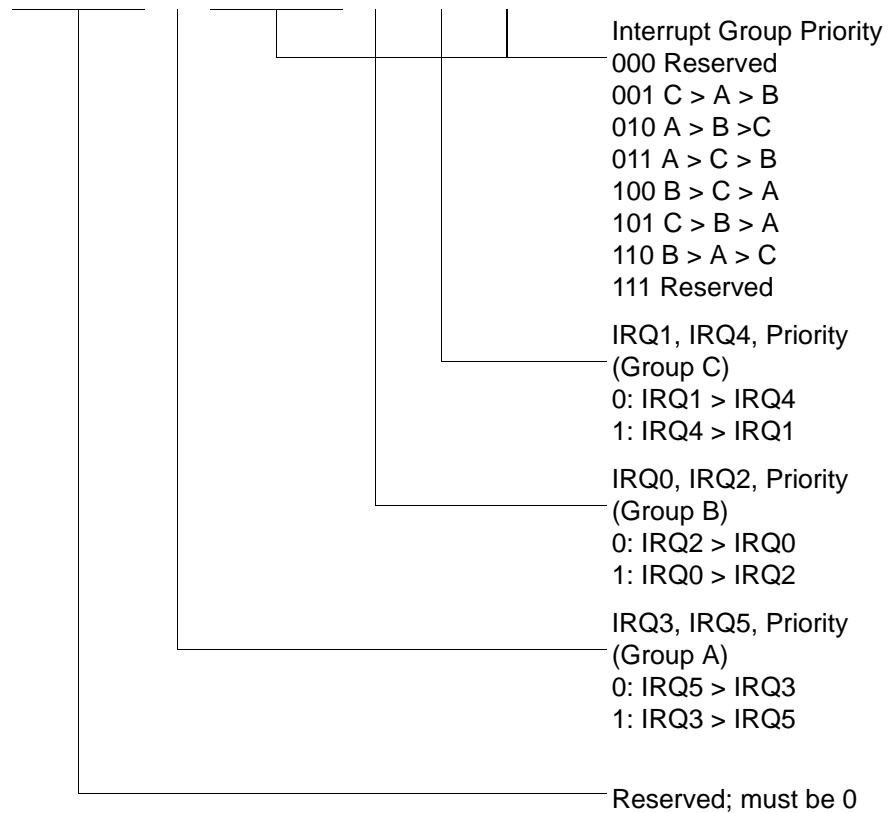


Figure 51. Interrupt Priority Register (F9H: Write Only)

## Ordering Information

<b>32KB Standard Temperature: 0° to +70°C</b>			
<b>Part Number</b>	<b>Description</b>	<b>Part Number</b>	<b>Description</b>
ZGP323LSH4832C	48-pin SSOP 32K OTP	ZGP323LSS2832C	28-pin SOIC 32K OTP
ZGP323LSP4032C	40-pin PDIP 32K OTP	ZGP323LSH2032C	20-pin SSOP 32K OTP
ZGP323LSH2832C	28-pin SSOP 32K OTP	ZGP323LSP2032C	20-pin PDIP 32K OTP
ZGP323LSP2832C	28-pin PDIP 32K OTP	ZGP323LSS2032C	20-pin SOIC 32K OTP
ZGP323LSK2032E	20-pin CDIP 32K OTP	ZGP323LSK4032E	40-pin CDIP 32K OTP
		ZGP323LSK2832E	28-pin CDIP 32K OTP
<b>32KB Extended Temperature: -40° to +105°C</b>			
<b>Part Number</b>	<b>Description</b>	<b>Part Number</b>	<b>Description</b>
ZGP323LEH4832C	48-pin SSOP 32K OTP	ZGP323LES2832C	28-pin SOIC 32K OTP
ZGP323LEP4032C	40-pin PDIP 32K OTP	ZGP323LEH2032C	20-pin SSOP 32K OTP
ZGP323LEH2832C	28-pin SSOP 32K OTP	ZGP323LEP2032C	20-pin PDIP 32K OTP
ZGP323LEP2832C	28-pin PDIP 32K OTP	ZGP323LES2032C	20-pin SOIC 32K OTP
<b>32KB Automotive Temperature: -40° to +125°C</b>			
<b>Part Number</b>	<b>Description</b>	<b>Part Number</b>	<b>Description</b>
ZGP323LAH4832C	48-pin SSOP 32K OTP	ZGP323LAS2832C	28-pin SOIC 32K OTP
ZGP323LAP4032C	40-pin PDIP 32K OTP	ZGP323LAH2032C	20-pin SSOP 32K OTP
ZGP323LAH2832C	28-pin SSOP 32K OTP	ZGP323LAP2032C	20-pin PDIP 32K OTP
ZGP323LAP2832C	28-pin PDIP 32K OTP	ZGP323LAS2032C	20-pin SOIC 32K OTP
Note: Replace C with G for Lead-Free Packaging			




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**8KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323LSH4808C	48-pin SSOP 8K OTP	ZGP323LSS2808C	28-pin SOIC 8K OTP
ZGP323LSP4008C	40-pin PDIP 8K OTP	ZGP323LSH2008C	20-pin SSOP 8K OTP
ZGP323LSH2808C	28-pin SSOP 8K OTP	ZGP323LSP2008C	20-pin PDIP 8K OTP
ZGP323LSP2808C	28-pin PDIP 8K OTP	ZGP323LSS2008C	20-pin SOIC 8K OTP

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**8KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323LEH4808C	48-pin SSOP 8K OTP	ZGP323LES2808C	28-pin SOIC 8K OTP
ZGP323LEP4008C	40-pin PDIP 8K OTP	ZGP323LEH2008C	20-pin SSOP 8K OTP
ZGP323LEH2808C	28-pin SSOP 8K OTP	ZGP323LEP2008C	20-pin PDIP 8K OTP
ZGP323LEP2808C	28-pin PDIP 8K OTP	ZGP323LES2008C	20-pin SOIC 8K OTP

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**8KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323LAH4808C	48-pin SSOP 8K OTP	ZGP323LAS2808C	28-pin SOIC 8K OTP
ZGP323LAP4008C	40-pin PDIP 8K OTP	ZGP323LAH2008C	20-pin SSOP 8K OTP
ZGP323LAH2808C	28-pin SSOP 8K OTP	ZGP323LAP2008C	20-pin PDIP 8K OTP
ZGP323LAP2808C	28-pin PDIP 8K OTP	ZGP323LAS2008C	20-pin SOIC 8K OTP

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Note: Replace C with G for Lead-Free Packaging

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**4KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323LSH4804C	48-pin SSOP 4K OTP	ZGP323LSS2804C	28-pin SOIC 4K OTP
ZGP323LSP4004C	40-pin PDIP 4K OTP	ZGP323LSH2004C	20-pin SSOP 4K OTP
ZGP323LSH2804C	28-pin SSOP 4K OTP	ZGP323LSP2004C	20-pin PDIP 4K OTP
ZGP323LSP2804C	28-pin PDIP 4K OTP	ZGP323LSS2004C	20-pin SOIC 4K OTP

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**4KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323LEH4804C	48-pin SSOP 4K OTP	ZGP323LES2804C	28-pin SOIC 4K OTP
ZGP323LEP4004C	40-pin PDIP 4K OTP	ZGP323LEH2004C	20-pin SSOP 4K OTP
ZGP323LEH2804C	28-pin SSOP 4K OTP	ZGP323LEP2004C	20-pin PDIP 4K OTP
ZGP323LEP2804C	28-pin PDIP 4K OTP	ZGP323LES2004C	20-pin SOIC 4K OTP

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**4KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323LAH4804C	48-pin SSOP 4K OTP	ZGP323LAS2804C	28-pin SOIC 4K OTP
ZGP323LAP4004C	40-pin PDIP 4K OTP	ZGP323LAH2004C	20-pin SSOP 4K OTP
ZGP323LAH2804C	28-pin SSOP 4K OTP	ZGP323LAP2004C	20-pin PDIP 4K OTP
ZGP323LAP2804C	28-pin PDIP 4K OTP	ZGP323LAS2004C	20-pin SOIC 4K OTP

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Note: Replace C with G for Lead-Free Packaging

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**Additional Components**

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer	ZGP32300100ZPR	Programming System



## **Precharacterization Product**

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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