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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323leh2032c">https://www.e-xfl.com/product-detail/zilog/zgp323leh2032c</a>



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- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

► **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K $\Omega$   $\pm$ 50% at  $V_{CC}$ =3 V and 450 K $\Omega$   $\pm$ 50% at  $V_{CC}$ =2 V.

## General Description

The Z8 GP™ OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

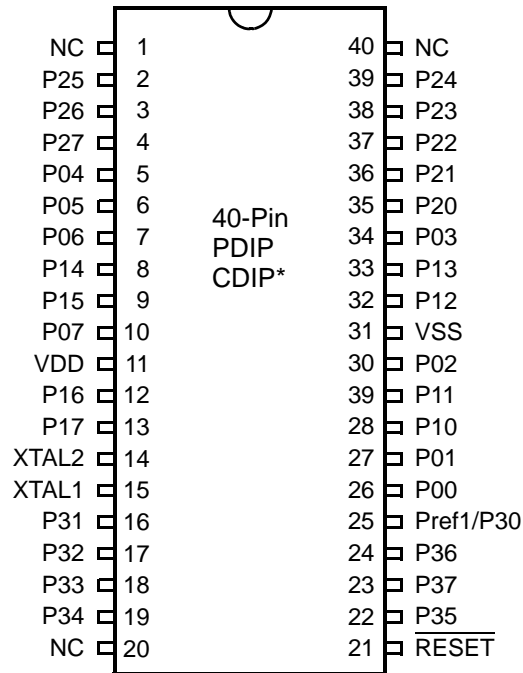
The Z8 GP™ OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, " $\overline{\phantom{x}}$ ", are active Low. For example,  $\overline{B/W}$ , in which WORD is active Low, and  $\overline{B/W}$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.



**Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration**

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

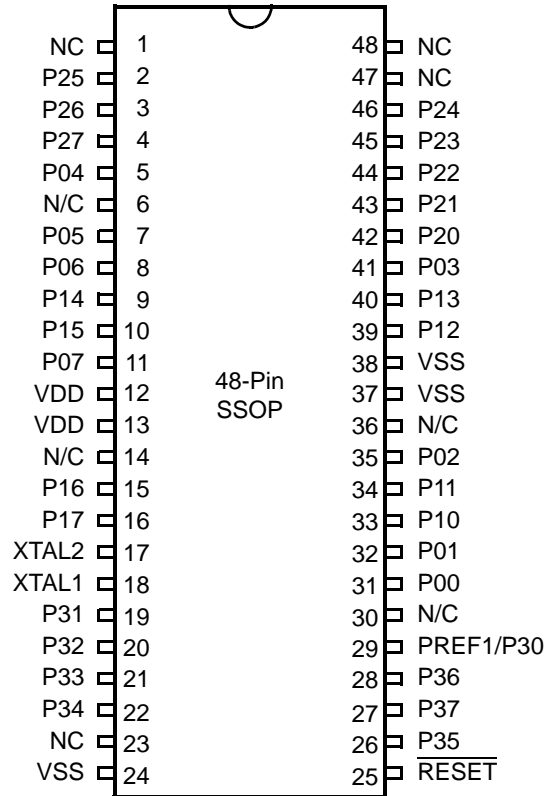


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12

## Capacitance

Table 7 lists the capacitances.

**Table 7. Capacitance**

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ\text{C}$ , $V_{CC} = \text{GND} = 0\text{V}$ , $f = 1.0\text{MHz}$ , unmeasured pins returned to GND	

## DC Characteristics

**Table 8. DC Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ	Max			
$V_{CC}$	Supply Voltage		2.0		3.6	V	See Note 5	5
$V_{CH}$	Clock Input High Voltage	2.0-3.6	0.8		$V_{CC}+0.3$	V	Driven by External Clock Generator	
$V_{CL}$	Clock Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		0.5	V	Driven by External Clock Generator	
$V_{IH}$	Input High Voltage	2.0-3.6	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
$V_{IL}$	Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
$V_{OH1}$	Output High Voltage	2.0-3.6	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
$V_{OH2}$	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
$V_{OL1}$	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 1.0\text{mA}$ $I_{OL} = 4.0\text{mA}$	
$V_{OL2}$	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	$I_{OL} = 10\text{mA}$	
$V_{OFFSET}$	Comparator Input Offset Voltage	2.0-3.6			25	mV		
$V_{REF}$	Comparator Reference Voltage	2.0-3.6	0		$V_{DD}$ -1.75	V		
$I_{IL}$	Input Leakage	2.0-3.6	-1		1	$\mu\text{A}$	$V_{IN} = 0\text{V}$ , $V_{CC}$ Pull-ups disabled	
$I_{OL}$	Output Leakage	2.0-3.6	-1		1	$\mu\text{A}$	$V_{IN} = 0\text{V}$ , $V_{CC}$	
$I_{CC}$	Supply Current	2.0			10	mA	at 8.0 MHz	1, 2
		3.6			15	mA	at 8.0 MHz	1, 2

## Timers

### T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

**Capture\_INT\_Mask**

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

**Counter\_INT\_Mask**

Set this bit to allow an interrupt when T8 has a timeout.

**P34\_Out**

This bit defines whether P34 is used as a normal output pin or the T8 output.

**T8 and T16 Common Functions—CTR1(0D)01H**

This register controls the functions in common with the T8 and T16.

Table 13 lists and briefly describes the fields for this register.

**Table 13. CTR1(0D)01H T8 and T16 Common Functions**

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0*	Transmit Mode
			1	Port Output
				T8/T16 Output
			0	Demodulation Mode
			1	P31
				P20
T8/T16_Logic/ Edge_Detect	--54----	R/W	00**	Transmit Mode
			01	AND
			10	OR
			11	NOR
				NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved



Table 14. CTR2(D)02H: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Transmit Mode
			1	Modulo-N
			0	Single Pass
			1	Demodulation Mode
Time_Out	--5-----	R	0*	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect
			01	Reset Flag to 0
			10	SCLK
			11	SCLK/2
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4
			1	SCLK/8
Counter_INT_Mask	-----1-	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.

**Note:**

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

**T16\_Enable**

This field enables T16 when set to 1.

**Single/Modulo-N**

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

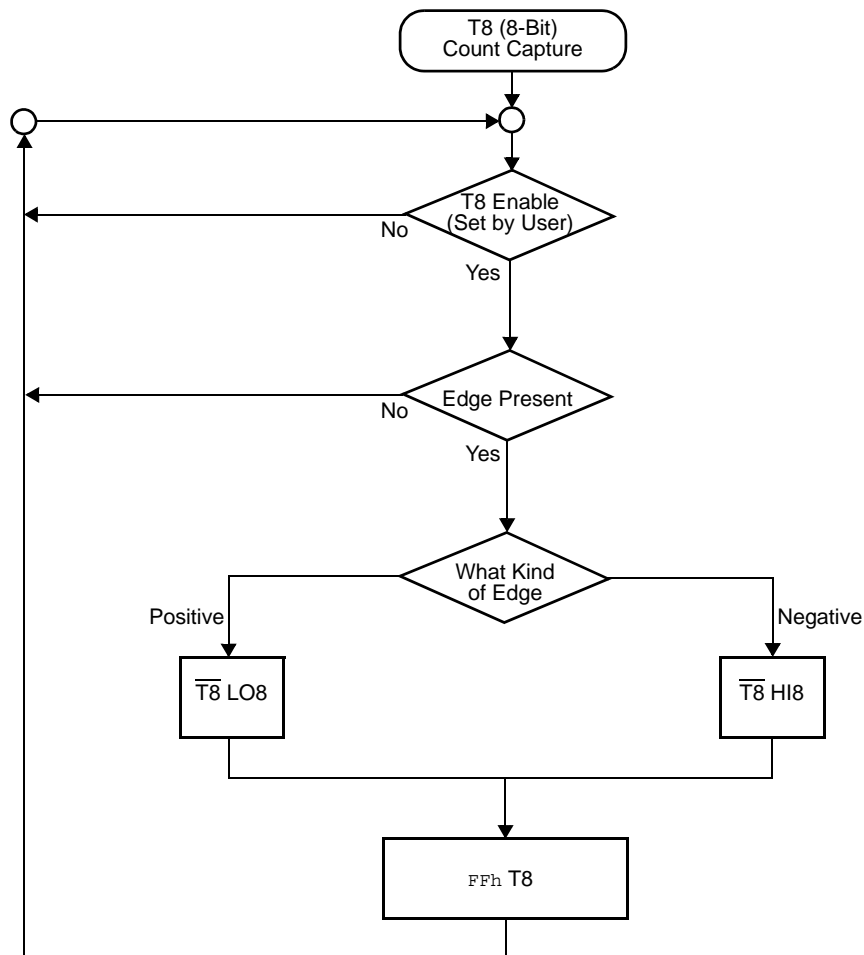


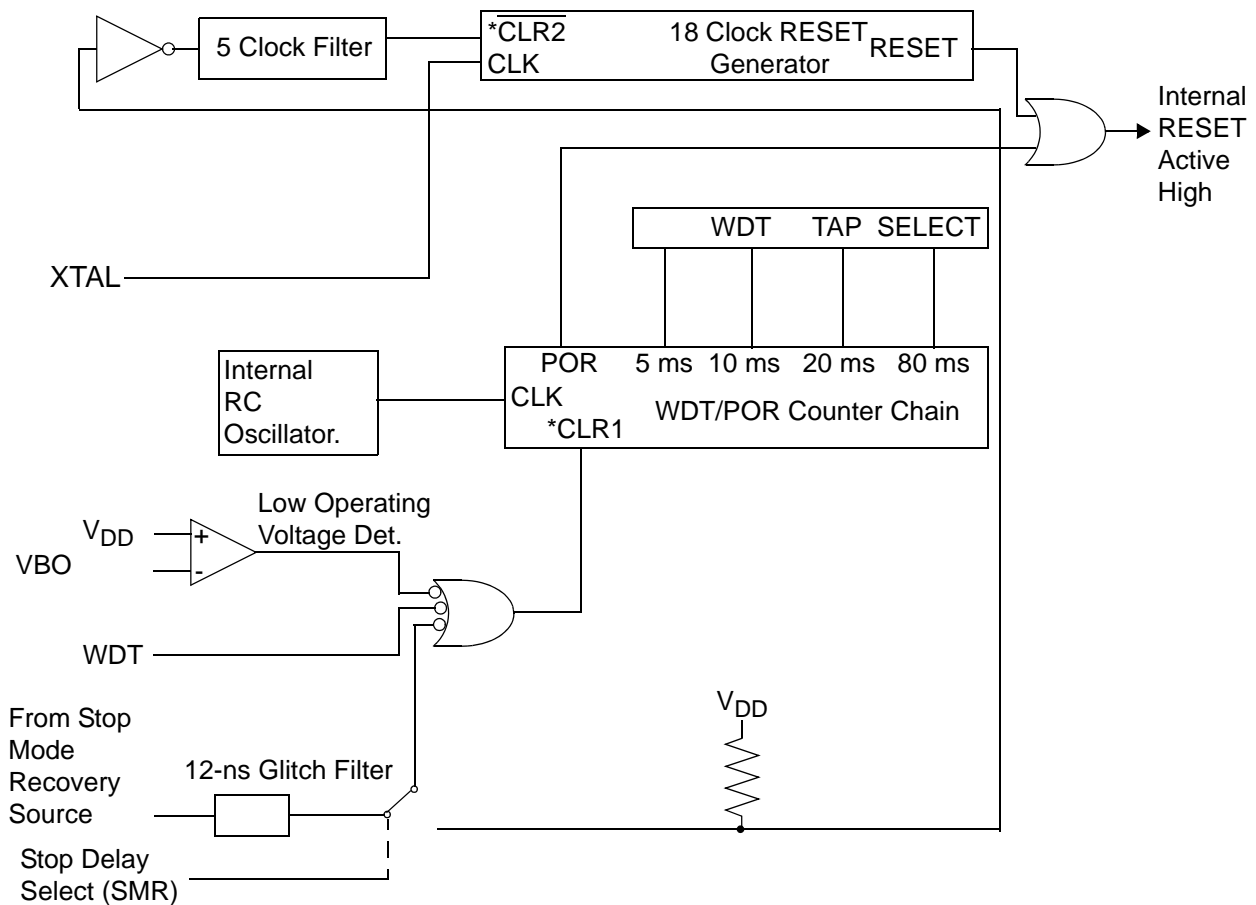
Figure 23. Demodulation Mode Count Capture Flowchart

**Table 20. Watch-Dog Timer Time Select**

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

### WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



\* CLR1 and  $\overline{\text{CLR2}}$  enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

**Figure 38. Resets and WDT**

### Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position	Description		
LVD	76543---	Reserved No Effect		
	----2--	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

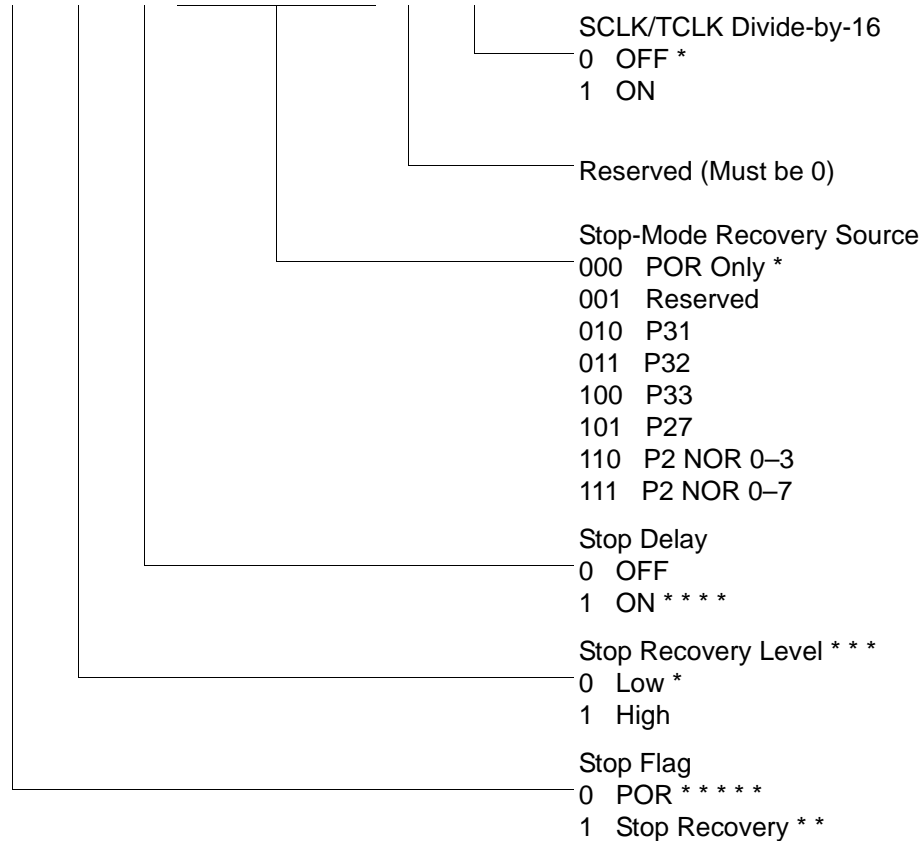


- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after Reset

\* \* Set after STOP Mode Recovery

\* \* \* At the XOR gate input

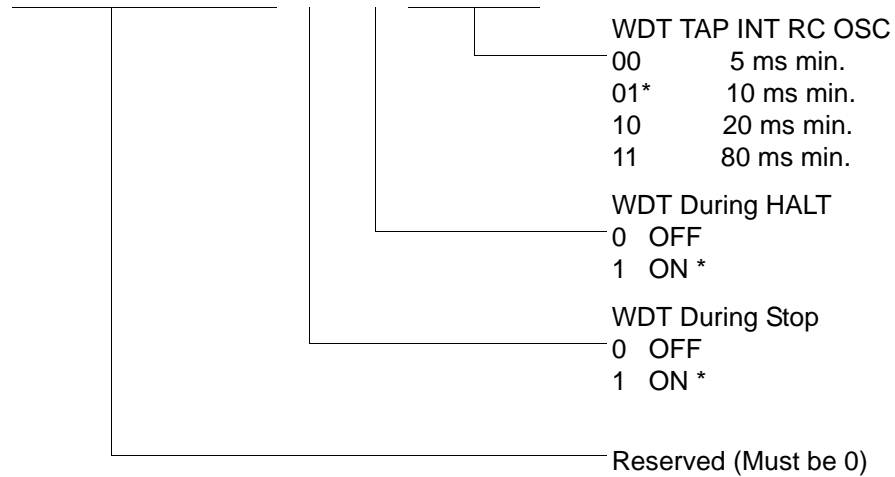
\* \* \* \* Default setting after Reset. Must be 1 if using a crystal or resonator clock source.

\* \* \* \* \* Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

**Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)**

WDTMR(0F)0FH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



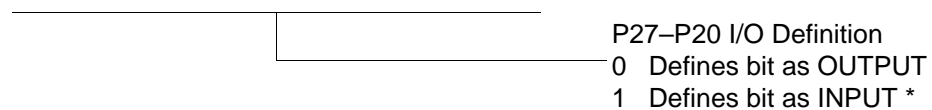
\* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

## Standard Control Registers

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

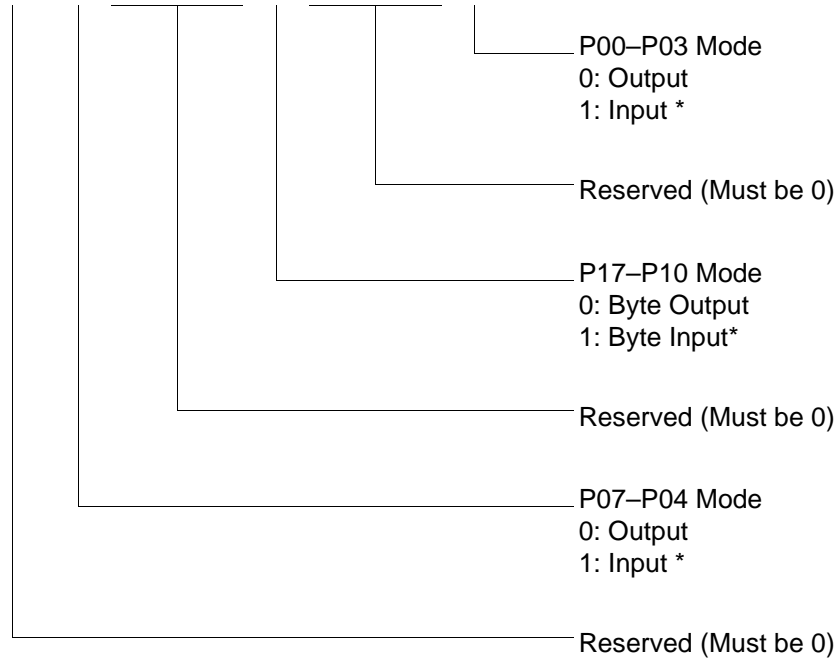


\* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)

R248 P01M(F8H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

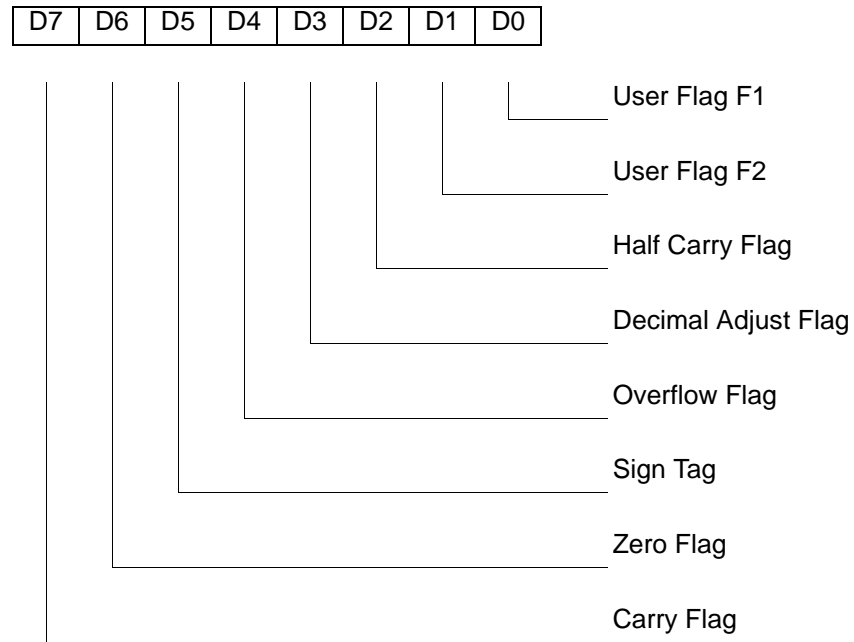


\* Default setting after reset; only P00, P01 and P07 are available in 20-pin configurations.

**Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)**

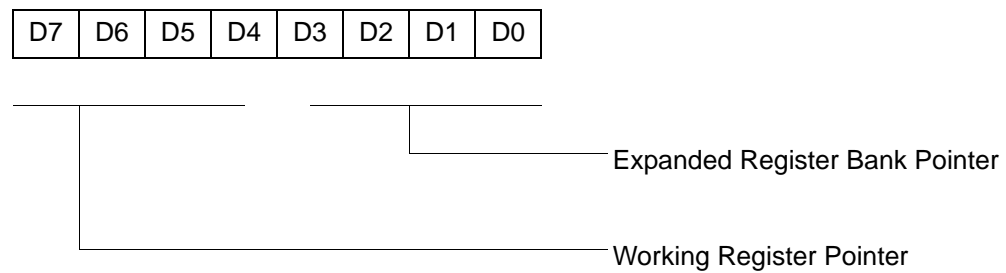


### R252 Flags(FCH)



**Figure 54. Flag Register (FCH: Read/Write)**

### R253 RP(FDH)



Default setting after reset = 0000 0000

**Figure 55. Register Pointer (FDH: Read/Write)**

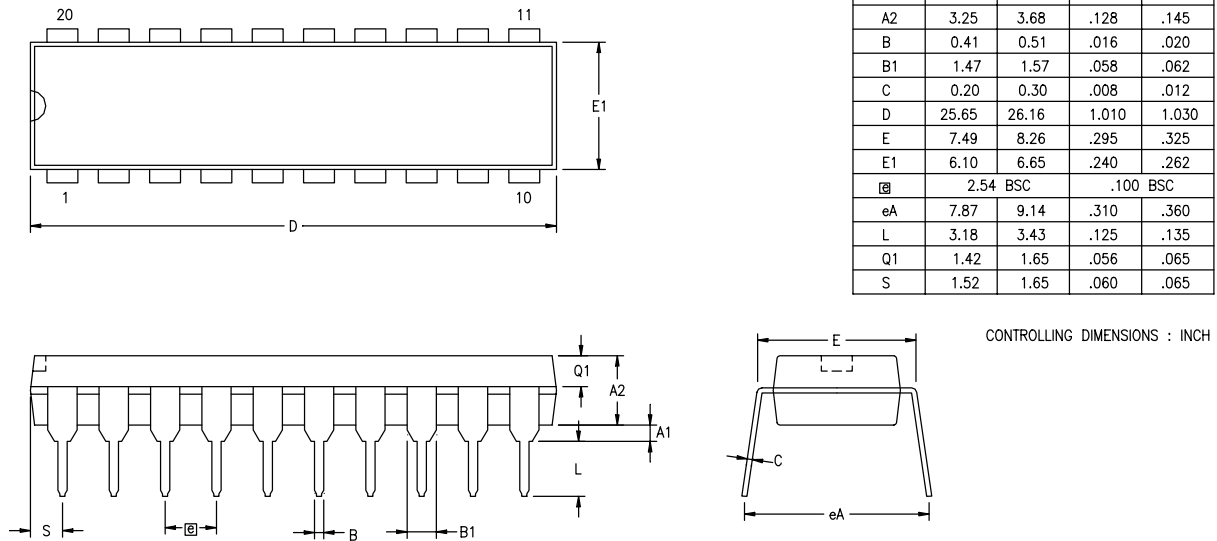


Figure 59. 20-Pin PDIP Package Diagram

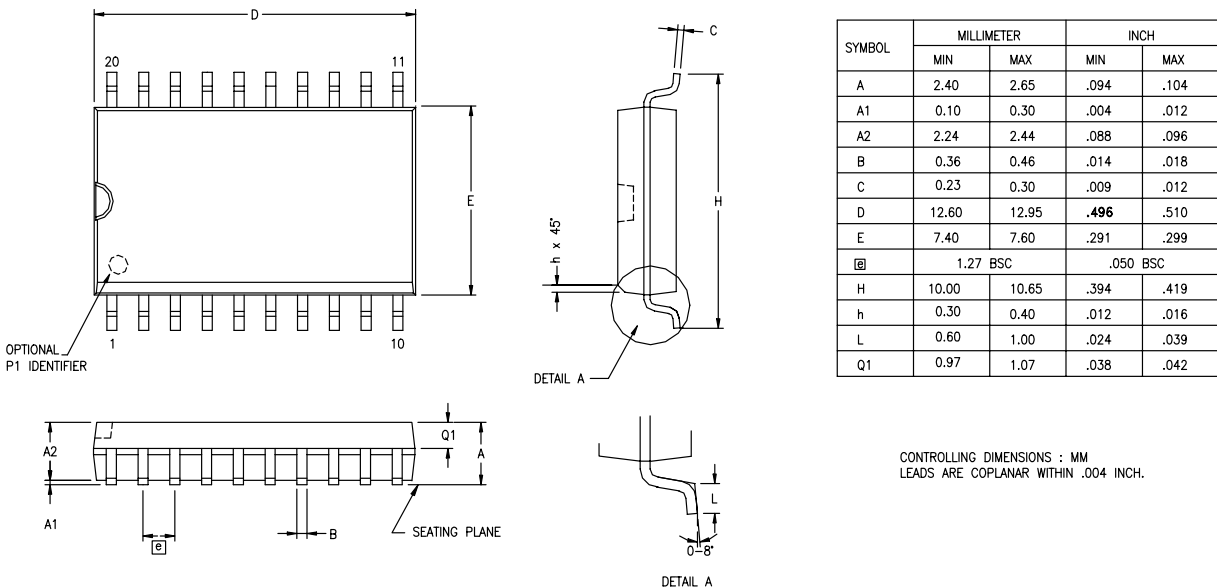
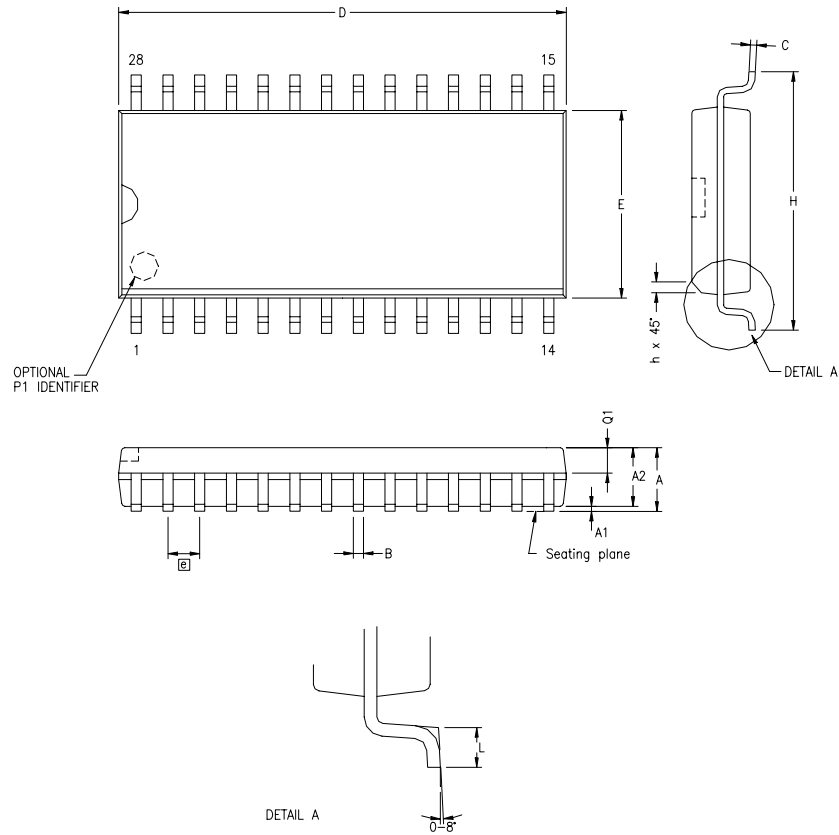


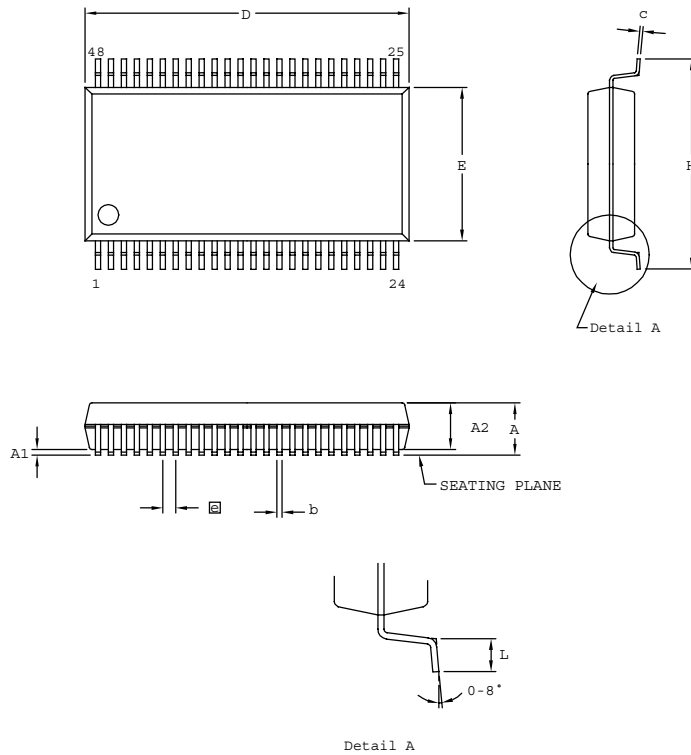
Figure 60. 20-Pin SOIC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
ⓐ	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM  
 LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 63. 28-Pin SOIC Package Diagram**



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
ⓐ	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM  
LEADS ARE COPLANAR WITHIN .004 INCH

**Figure 68. 48-Pin SSOP Package Design**

- **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



**8KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323LSH4808C	48-pin SSOP 8K OTP	ZGP323LSS2808C	28-pin SOIC 8K OTP
ZGP323LSP4008C	40-pin PDIP 8K OTP	ZGP323LSH2008C	20-pin SSOP 8K OTP
ZGP323LSH2808C	28-pin SSOP 8K OTP	ZGP323LSP2008C	20-pin PDIP 8K OTP
ZGP323LSP2808C	28-pin PDIP 8K OTP	ZGP323LSS2008C	20-pin SOIC 8K OTP

**8KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323LEH4808C	48-pin SSOP 8K OTP	ZGP323LES2808C	28-pin SOIC 8K OTP
ZGP323LEP4008C	40-pin PDIP 8K OTP	ZGP323LEH2008C	20-pin SSOP 8K OTP
ZGP323LEH2808C	28-pin SSOP 8K OTP	ZGP323LEP2008C	20-pin PDIP 8K OTP
ZGP323LEP2808C	28-pin PDIP 8K OTP	ZGP323LES2008C	20-pin SOIC 8K OTP

**8KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323LAH4808C	48-pin SSOP 8K OTP	ZGP323LAS2808C	28-pin SOIC 8K OTP
ZGP323LAP4008C	40-pin PDIP 8K OTP	ZGP323LAH2008C	20-pin SSOP 8K OTP
ZGP323LAH2808C	28-pin SSOP 8K OTP	ZGP323LAP2008C	20-pin PDIP 8K OTP
ZGP323LAP2808C	28-pin PDIP 8K OTP	ZGP323LAS2008C	20-pin SOIC 8K OTP

Note: Replace C with G for Lead-Free Packaging