



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323leh2808c



Table of Contents

Development Features	1
General Description	2
Pin Description	4
Absolute Maximum Ratings	10
Standard Test Conditions	10
DC Characteristics	11
AC Characteristics	14
Pin Functions	16
XTAL1 Crystal 1 (Time-Based Input)	16
XTAL2 Crystal 2 (Time-Based Output)	16
Port 0 (P07–P00)	16
Port 1 (P17–P10)	17
Port 2 (P27–P20)	18
Port 3 (P37–P30)	19
RESET (Input, Active Low)	23
Functional Description	23
Program Memory	23
RAM	23
Expanded Register File	24
Register File	28
Stack	29
Timers	30
Counter/Timer Functional Blocks	38
Expanded Register File Control Registers (0D)	64
Expanded Register File Control Registers (0F)	69
Standard Control Registers	73
Package Information	80
Ordering Information	89
Precharacterization Product	95

Figure 35. Stop Mode Recovery Source	57
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only) . . .	59
Figure 37. Watch-Dog Timer Mode Register (Write Only)	60
Figure 38. Resets and WDT	61
Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted) . . .	64
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write) . . .	65
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted) . . .	67
Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)	68
Figure 43. Voltage Detection Register	69
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)	70
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)	71
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only) . . .	72
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)	73
Figure 48. Port 2 Mode Register (F6H: Write Only)	73
Figure 49. Port 3 Mode Register (F7H: Write Only)	74
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)	75
Figure 51. Interrupt Priority Register (F9H: Write Only)	76
Figure 52. Interrupt Request Register (FAH: Read/Write)	77
Figure 53. Interrupt Mask Register (FBH: Read/Write)	77
Figure 54. Flag Register (FCH: Read/Write)	78
Figure 55. Register Pointer (FDH: Read/Write)	78
Figure 56. Stack Pointer High (FEH: Read/Write)	79
Figure 57. Stack Pointer Low (FFH: Read/Write)	79
Figure 58. 20-Pin CDIP Package	80
Figure 59. 20-Pin PDIP Package Diagram	81
Figure 60. 20-Pin SOIC Package Diagram	81
Figure 61. 20-Pin SSOP Package Diagram	82
Figure 62. 28-Pin CDIP Package	83
Figure 63. 28-Pin SOIC Package Diagram	84
Figure 64. 28-Pin PDIP Package Diagram	85
Figure 65. 28-Pin SSOP Package Diagram	86
Figure 66. 40-Pin CDIP Package	87
Figure 67. 40-Pin PDIP Package Diagram	87
Figure 68. 48-Pin SSOP Package Design	88

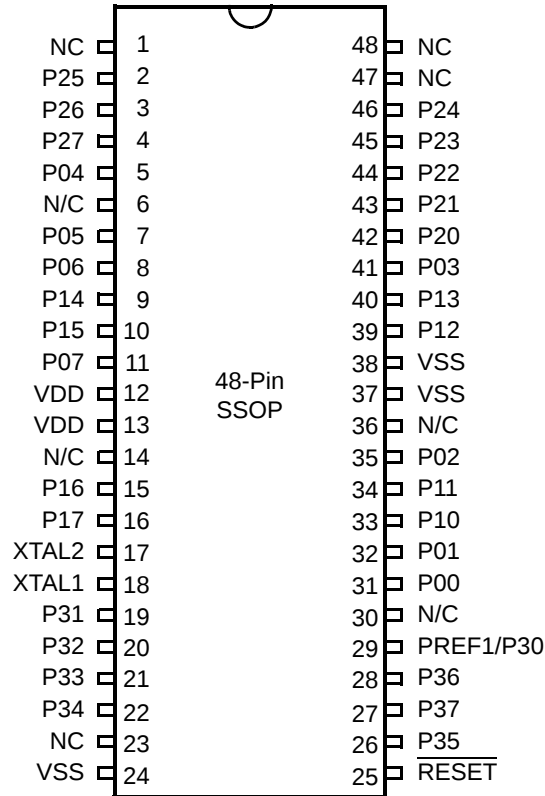


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12

Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC

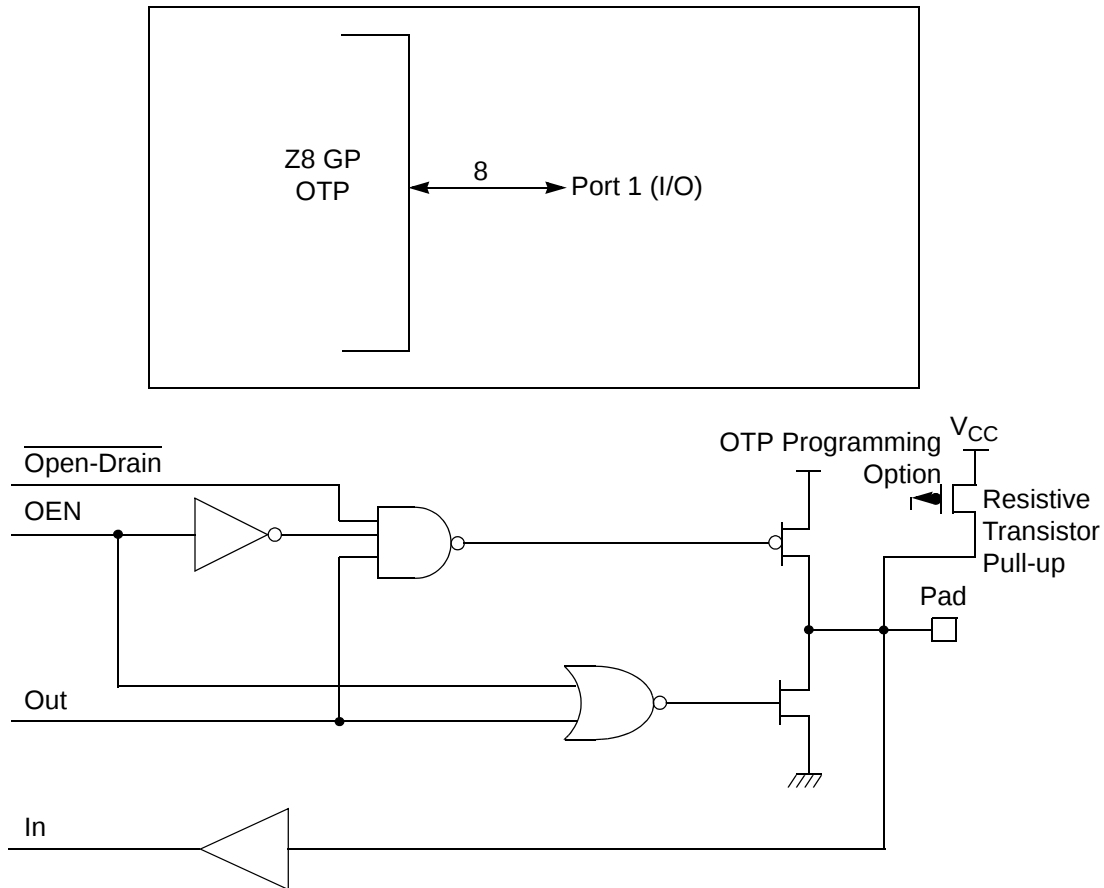


Figure 10. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

Z8® Standard Control Registers

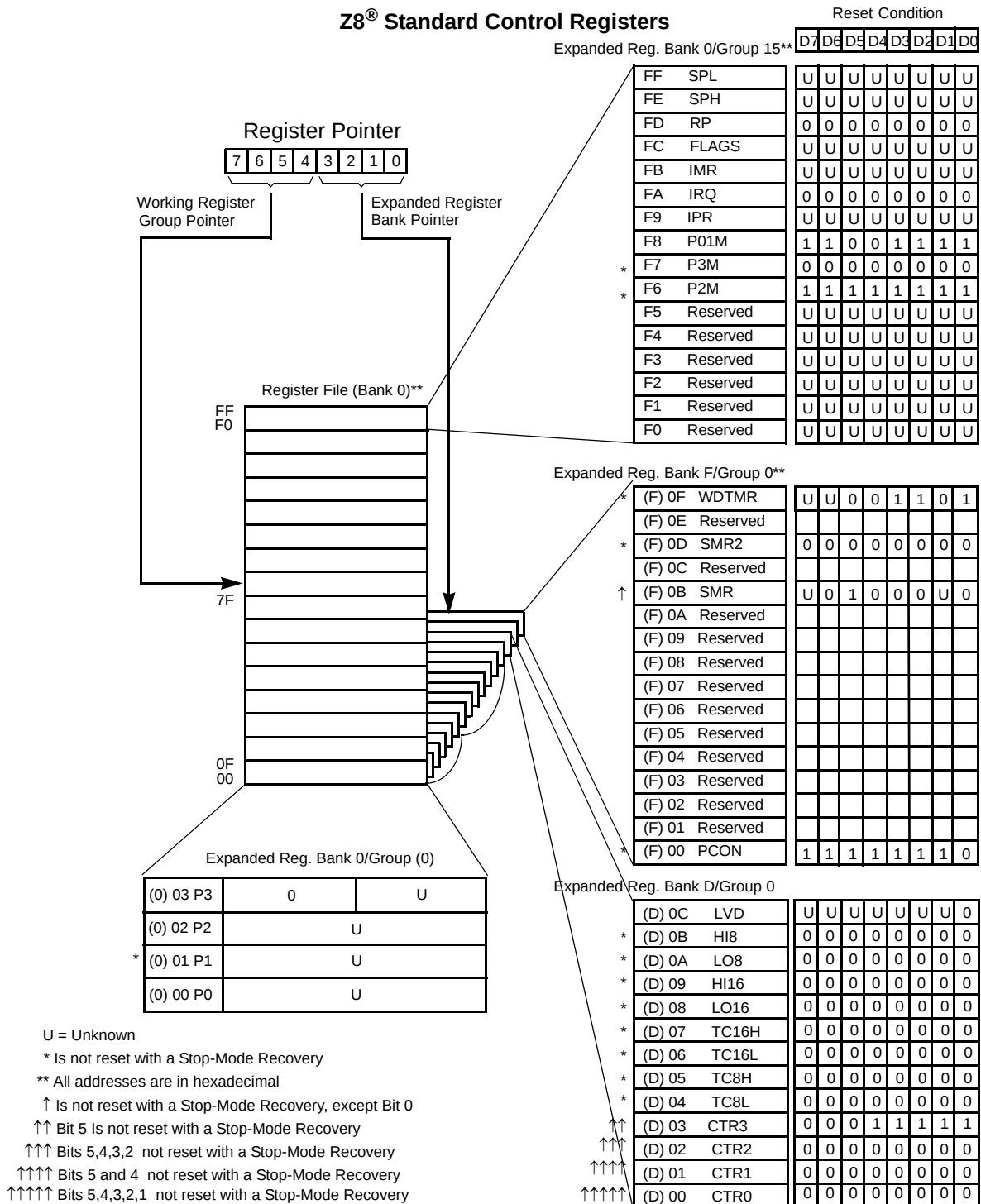


Figure 15. Expanded Register File Architecture

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          R0, #xx           ; load CTRL0
LD          1, #xx            ; load CTRL1
LD          R1, 2              ; CTRL2→CTRL1

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          RP, #7Dh          ; Select
expanded register bank D and working ; register
group 7 of bank 0 for access.
LD          71h, 2             ; CTRL2→register 71h
; CTRL2→register 71h
LD          R1, 2              ; CTRL2→register 71h
; CTRL2→register 71h

```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

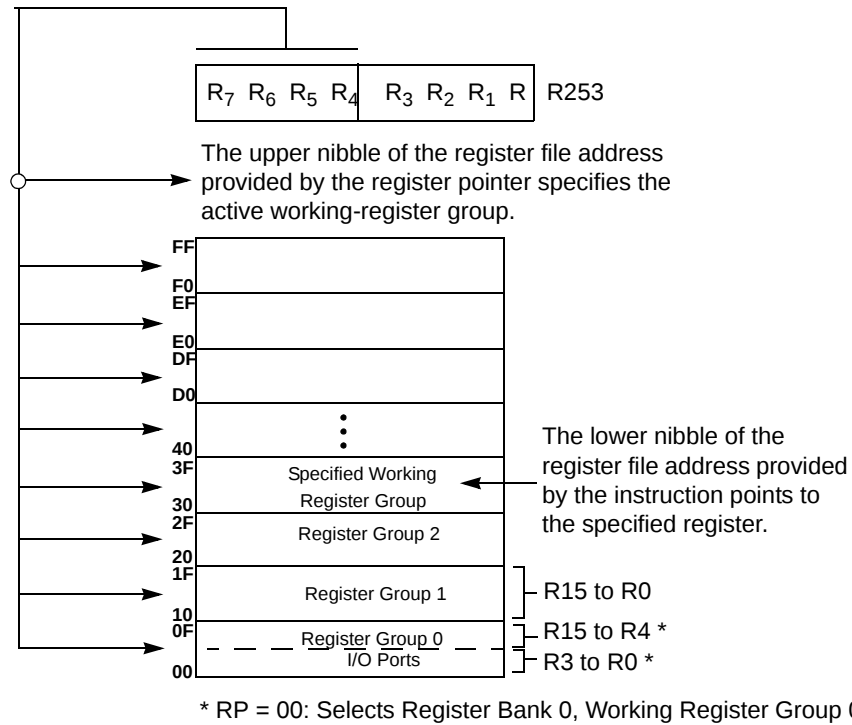


Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 14 lists and briefly describes the fields for this register.

Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

Note: *Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

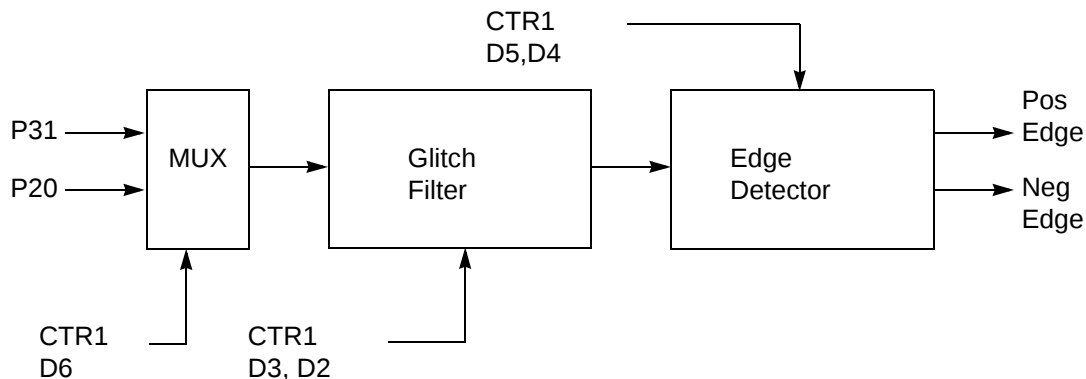


Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.

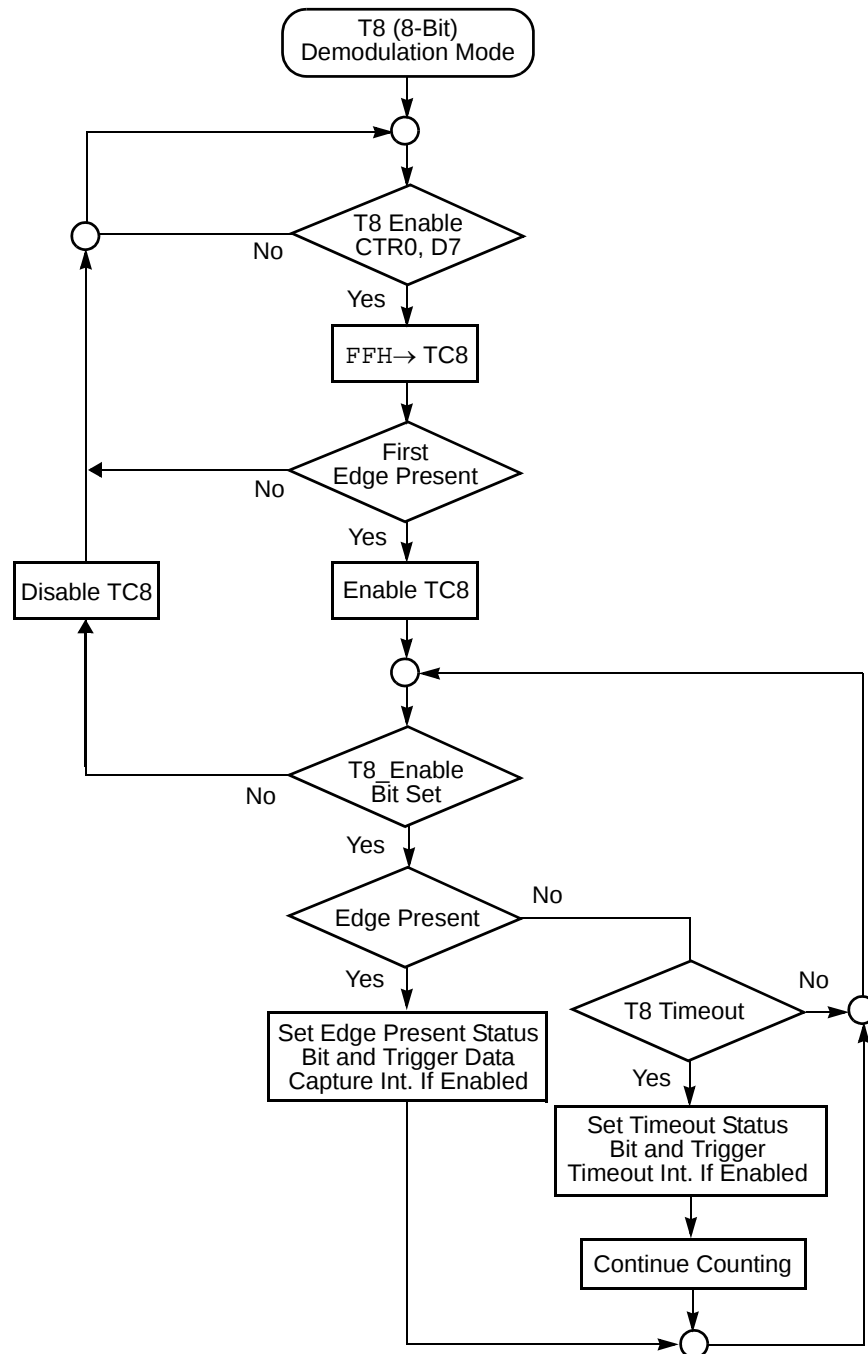


Figure 24. Demodulation Mode Flowchart

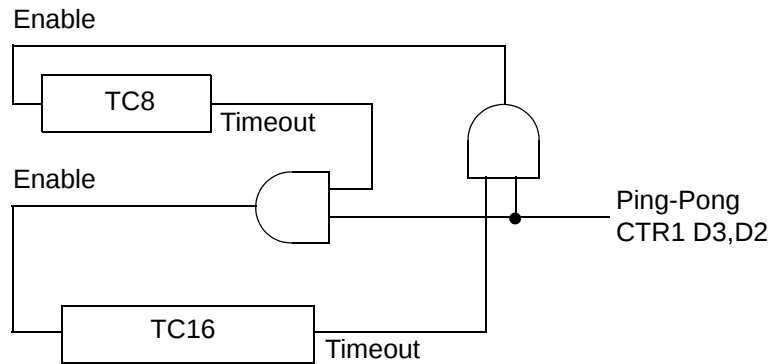


Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

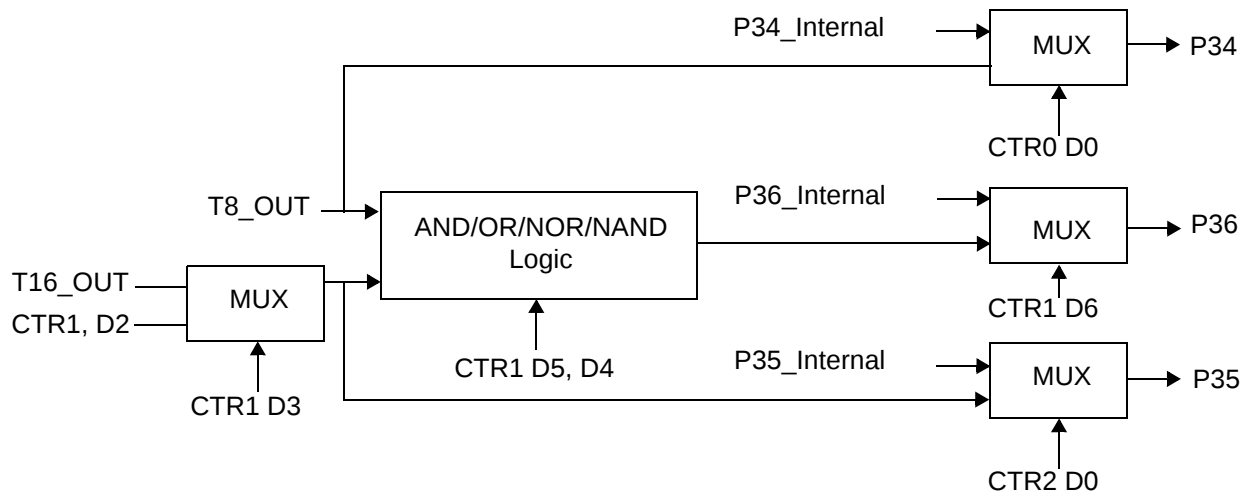
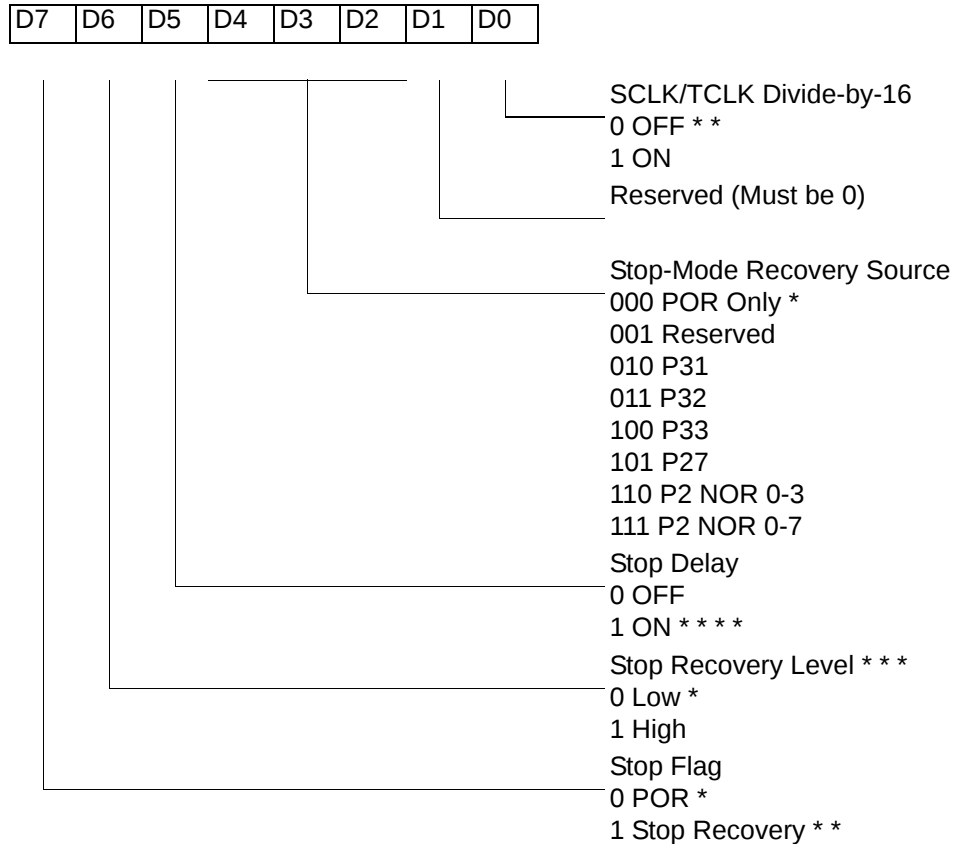


Figure 29. Output Circuit

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

** Set after STOP Mode Recovery

*** At the XOR gate input

**** Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

Table 19. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 59 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 T_{pC} .

- **Note:** It is recommended that this bit be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

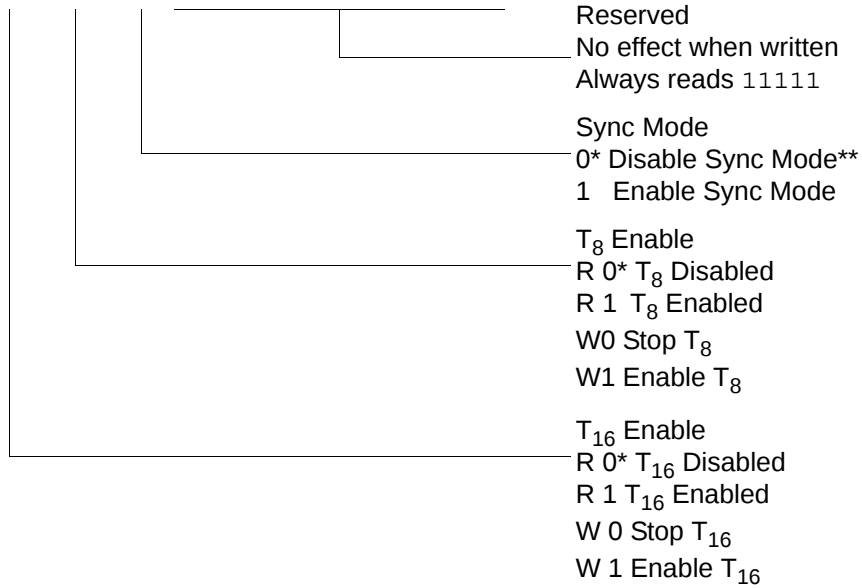
A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset.

** Default setting after reset. Not reset with Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

► **Note:** If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.

R254 SPH(FEH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

General-Purpose Register

Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Stack Pointer Low
Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

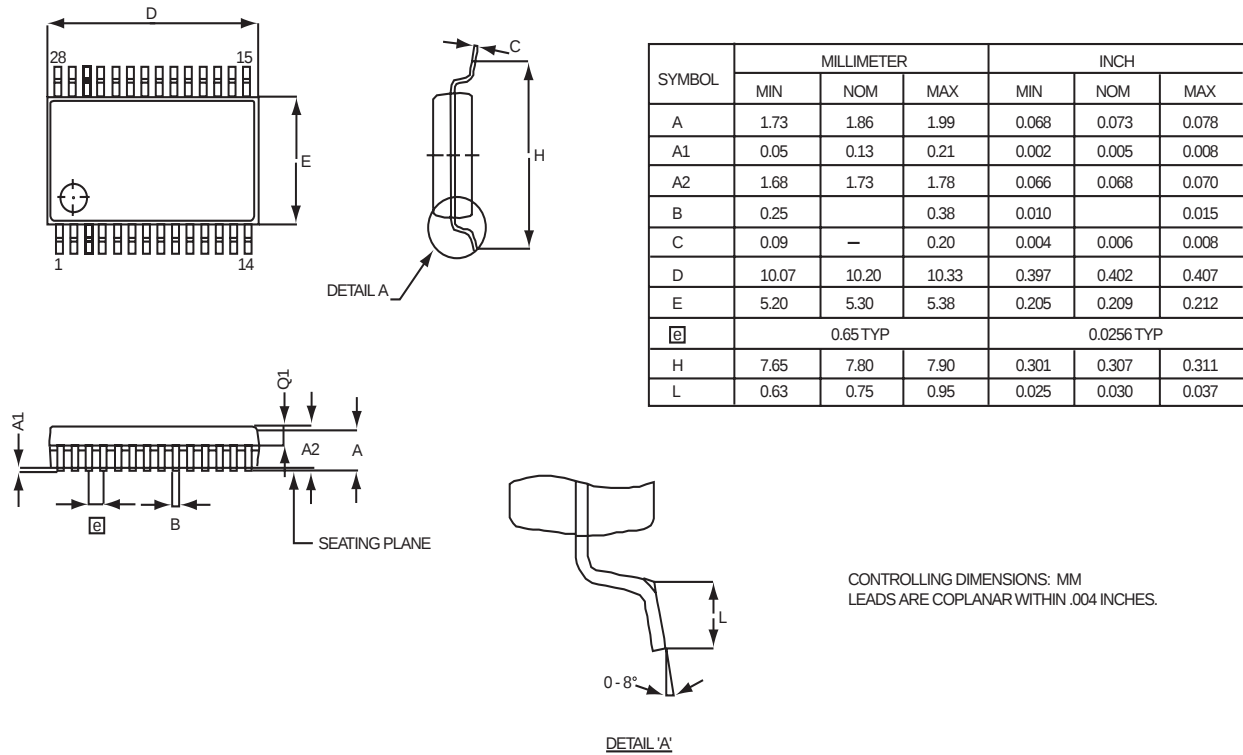


Figure 65. 28-Pin SSOP Package Diagram

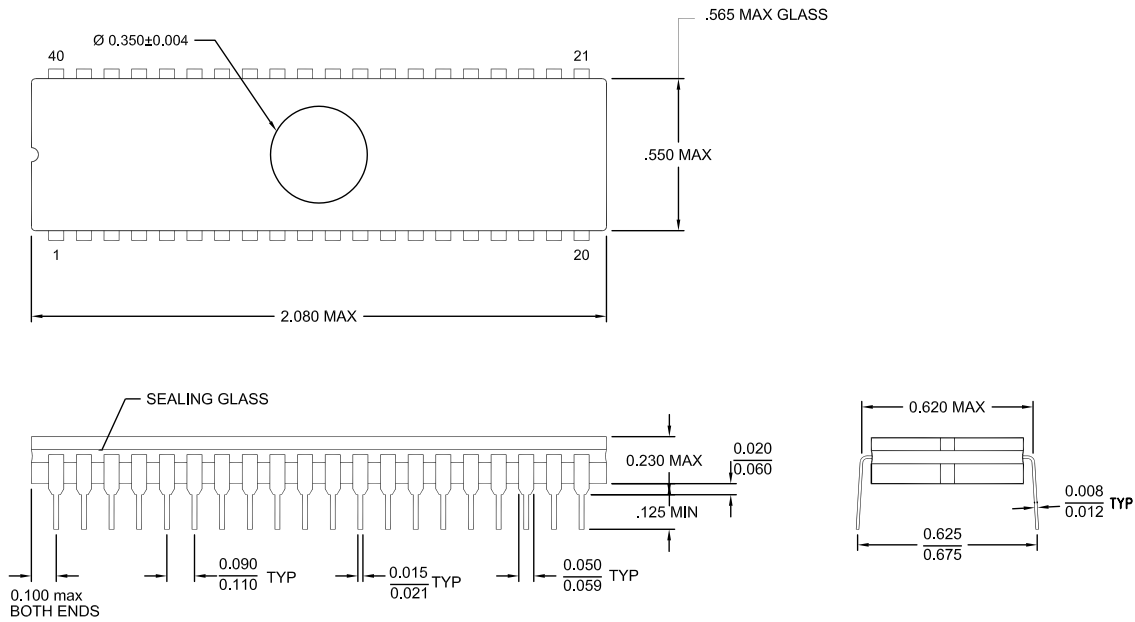


Figure 66. 40-Pin CDIP Package

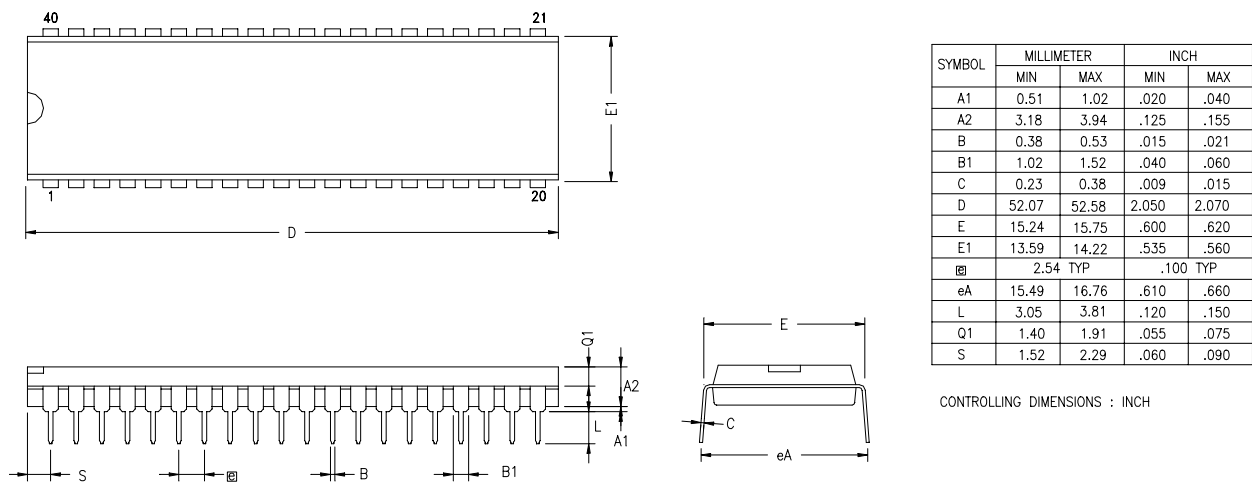


Figure 67. 40-Pin PDIP Package Diagram

4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4804C	48-pin SSOP 4K OTP	ZGP323LSS2804C	28-pin SOIC 4K OTP
ZGP323LSP4004C	40-pin PDIP 4K OTP	ZGP323LSH2004C	20-pin SSOP 4K OTP
ZGP323LSH2804C	28-pin SSOP 4K OTP	ZGP323LSP2004C	20-pin PDIP 4K OTP
ZGP323LSP2804C	28-pin PDIP 4K OTP	ZGP323LSS2004C	20-pin SOIC 4K OTP

4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4804C	48-pin SSOP 4K OTP	ZGP323LES2804C	28-pin SOIC 4K OTP
ZGP323LEP4004C	40-pin PDIP 4K OTP	ZGP323LEH2004C	20-pin SSOP 4K OTP
ZGP323LEH2804C	28-pin SSOP 4K OTP	ZGP323LEP2004C	20-pin PDIP 4K OTP
ZGP323LEP2804C	28-pin PDIP 4K OTP	ZGP323LES2004C	20-pin SOIC 4K OTP

4KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4804C	48-pin SSOP 4K OTP	ZGP323LAS2804C	28-pin SOIC 4K OTP
ZGP323LAP4004C	40-pin PDIP 4K OTP	ZGP323LAH2004C	20-pin SSOP 4K OTP
ZGP323LAH2804C	28-pin SSOP 4K OTP	ZGP323LAP2004C	20-pin PDIP 4K OTP
ZGP323LAP2804C	28-pin PDIP 4K OTP	ZGP323LAS2004C	20-pin SOIC 4K OTP

Note: Replace C with G for Lead-Free Packaging

Additional Components

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer	ZGP32300100ZPR	Programming System

D

DC characteristics 11
demodulation mode
 count capture flowchart 42
 flowchart 43
 T16 45
 T8 41
description
 functional 23
 general 2
 pin 4

E

EPROM
 selectable options 62
expanded register file 24
expanded register file architecture 26
expanded register file control registers 69
 flag 78
 interrupt mask register 77
 interrupt priority register 76
 interrupt request register 77
 port 0 and 1 mode register 75
 port 2 configuration register 73
 port 3 mode register 74
 port configuration register 73
 register pointer 78
 stack pointer high register 79
 stack pointer low register 79
 stop-mode recovery register 71
 stop-mode recovery register 2 72
 T16 control register 67
 T8 and T16 common control functions register 65
 T8/T16 control register 68
 TC8 control register 64
 watch-dog timer register 73

F

features
 standby modes 1

functional description

counter/timer functional blocks 38
CTR(D)01h register 33
CTR0(D)00h register 31
CTR2(D)02h register 35
CTR3(D)03h register 37
expanded register file 24
expanded register file architecture 26
HI16(D)09h register 30
HI8(D)0Bh register 30
LO8(D)0Ah register 30
LO16(D)08h register 30
program memory map 24
RAM 23
register description 63
register file 28
register pointer 27
register pointer detail 29
SMR2(F)0D1h register 38
stack 29
TC16H(D)07h register 30
TC16L(D)06h register 31
TC8H(D)05h register 31
TC8L(D)04h register 31

G

glitch filter circuitry 38

H

halt instruction, counter/timer 52

I

input circuit 38
interrupt block diagram, counter/timer 49
interrupt types, sources and vectors 50

L

low-voltage detection register 63