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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323leh2808g |

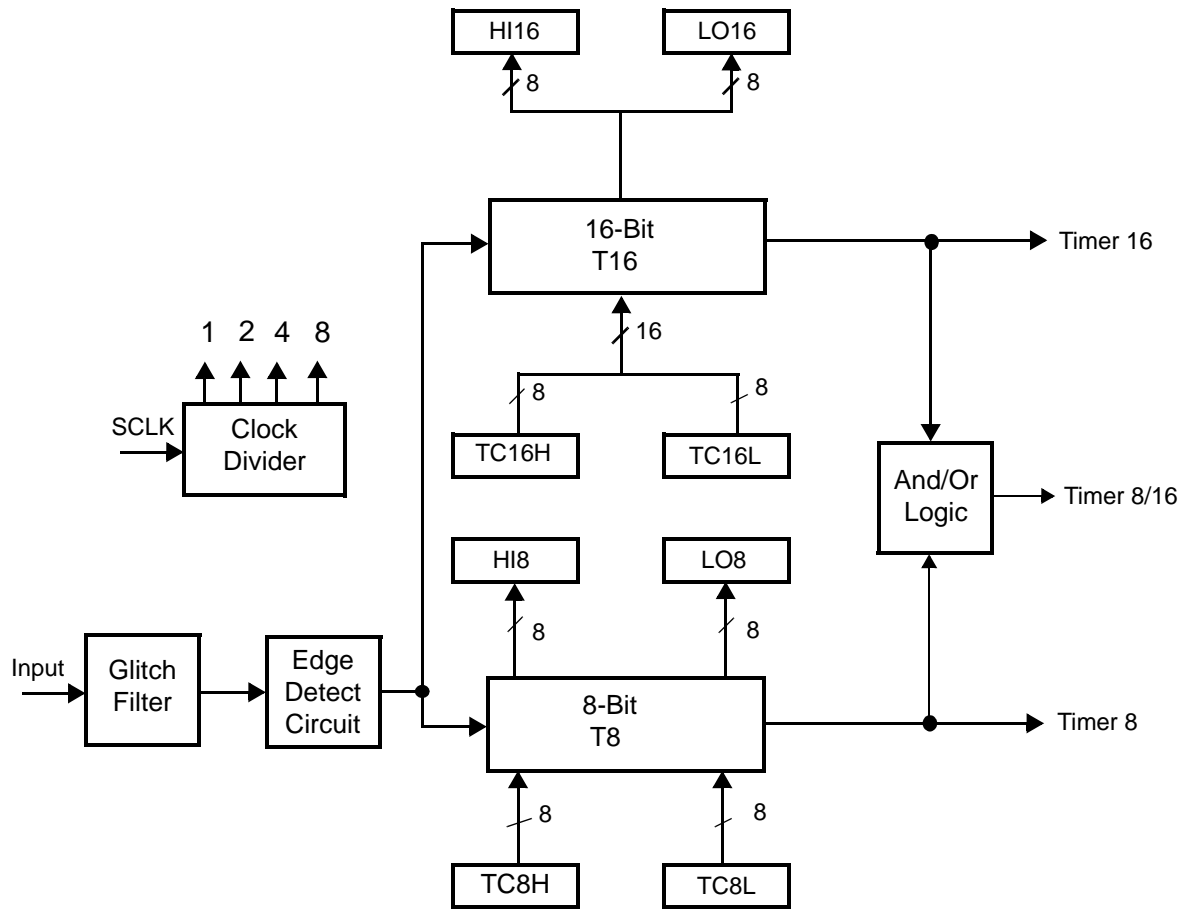


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 5.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

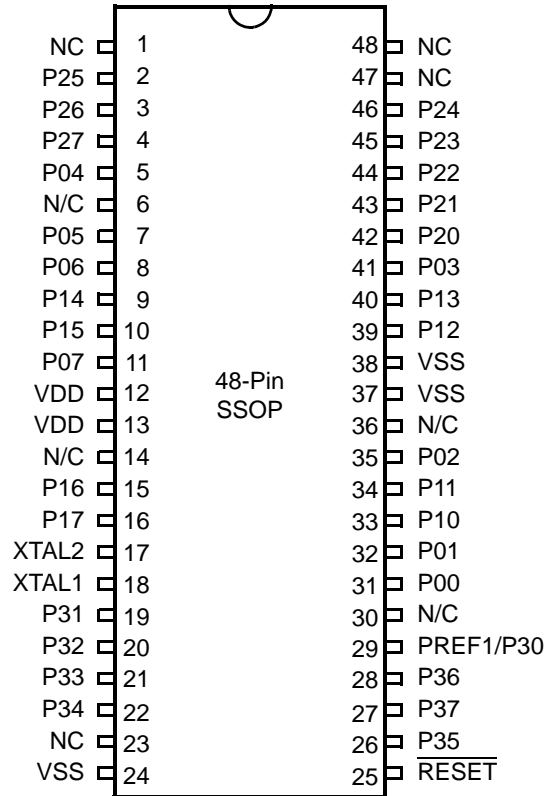


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

| 40-Pin PDIP/CDIP* # | 48-Pin SSOP # | Symbol |
|---------------------|---------------|--------|
| 26 | 31 | P00 |
| 27 | 32 | P01 |
| 30 | 35 | P02 |
| 34 | 41 | P03 |
| 5 | 5 | P04 |
| 6 | 7 | P05 |
| 7 | 8 | P06 |
| 10 | 11 | P07 |
| 28 | 33 | P10 |
| 29 | 34 | P11 |
| 32 | 39 | P12 |

AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.

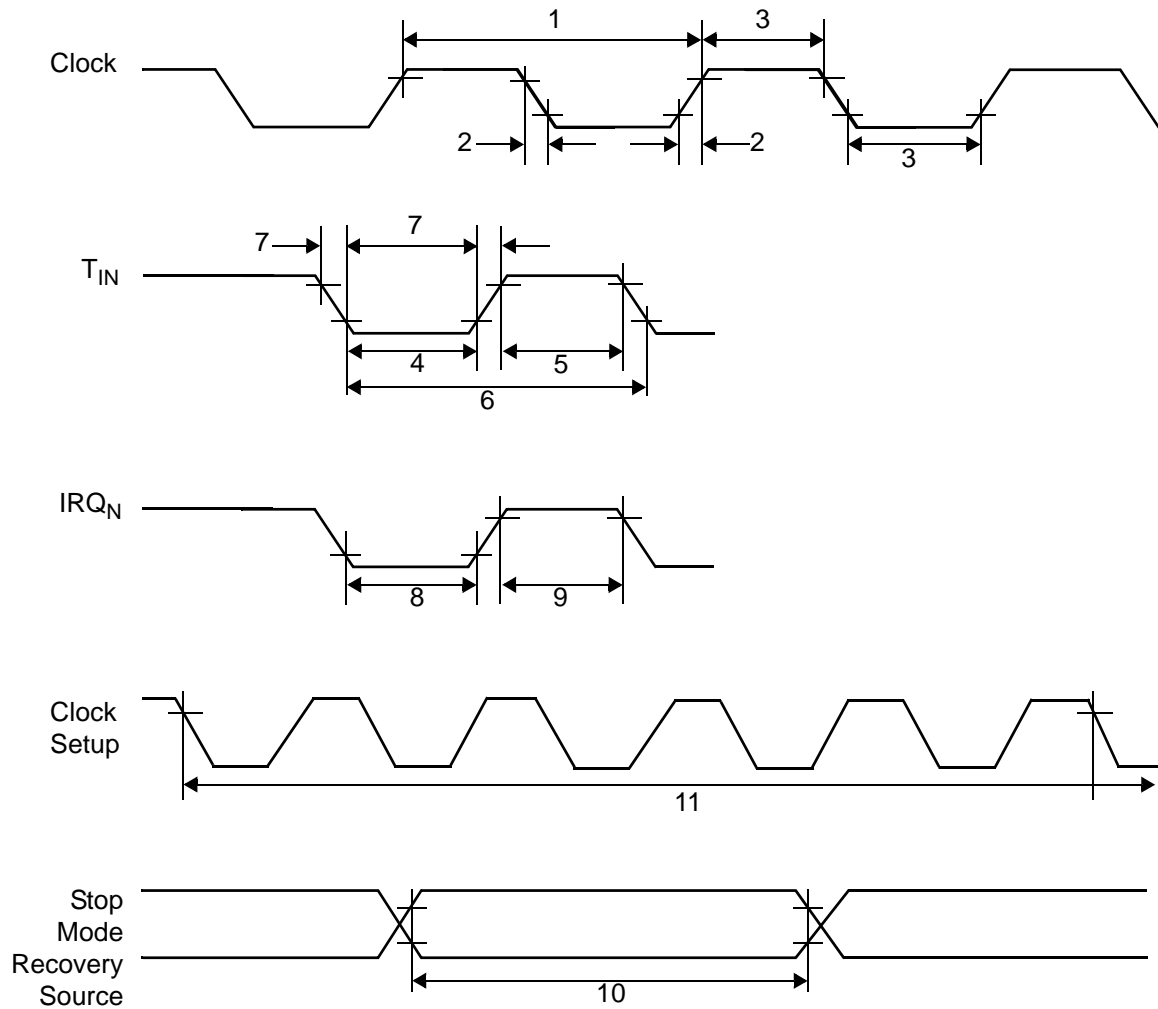


Figure 8. AC Timing Diagram

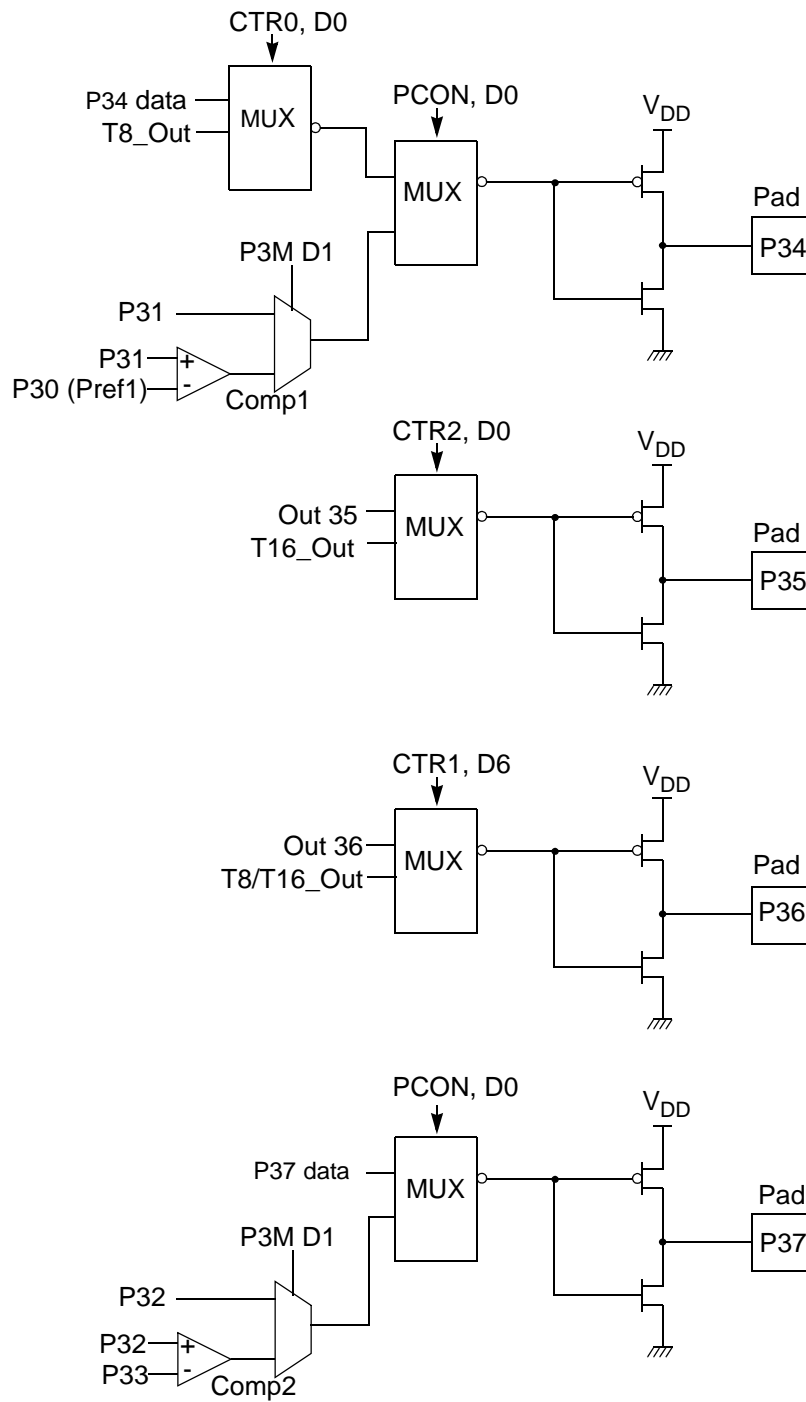


Figure 13. Port 3 Counter/Timer Output Configuration

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

- **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP™ asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP™ does not assert the RESET pin when under VBO.

- **Note:** The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8®, functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.

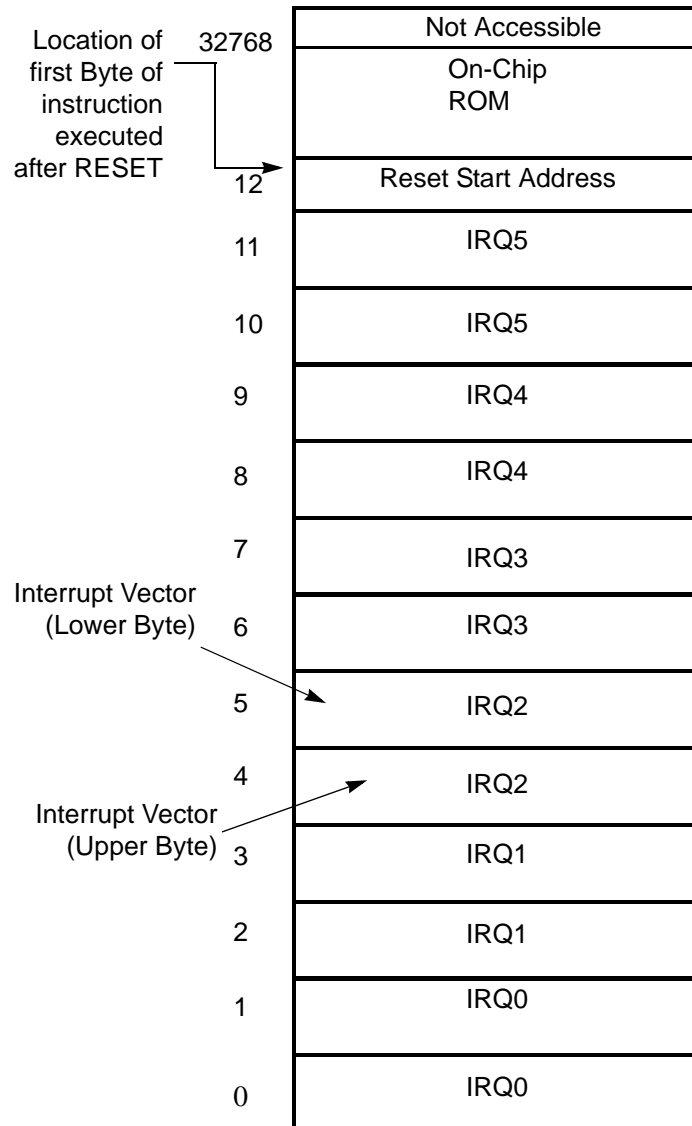


Figure 14. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8® register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the

Z8[®] Standard Control Registers

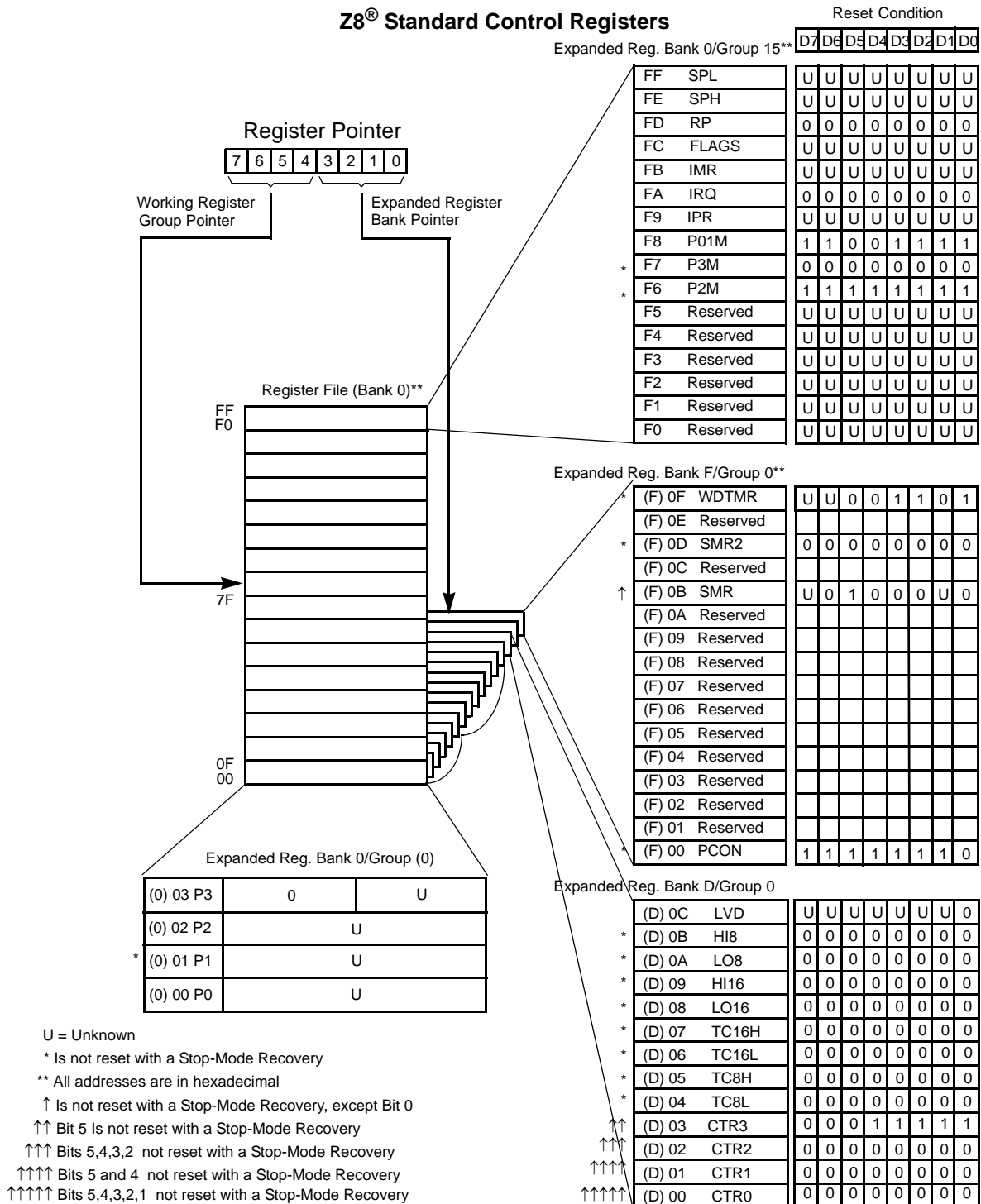


Figure 15. Expanded Register File Architecture

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

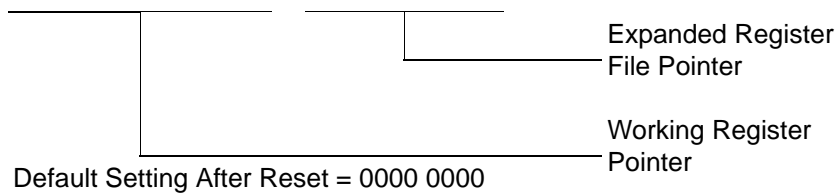


Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 26)

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTRL0

R1 = CTRL1

R2 = CTRL2

R3 = Reserved

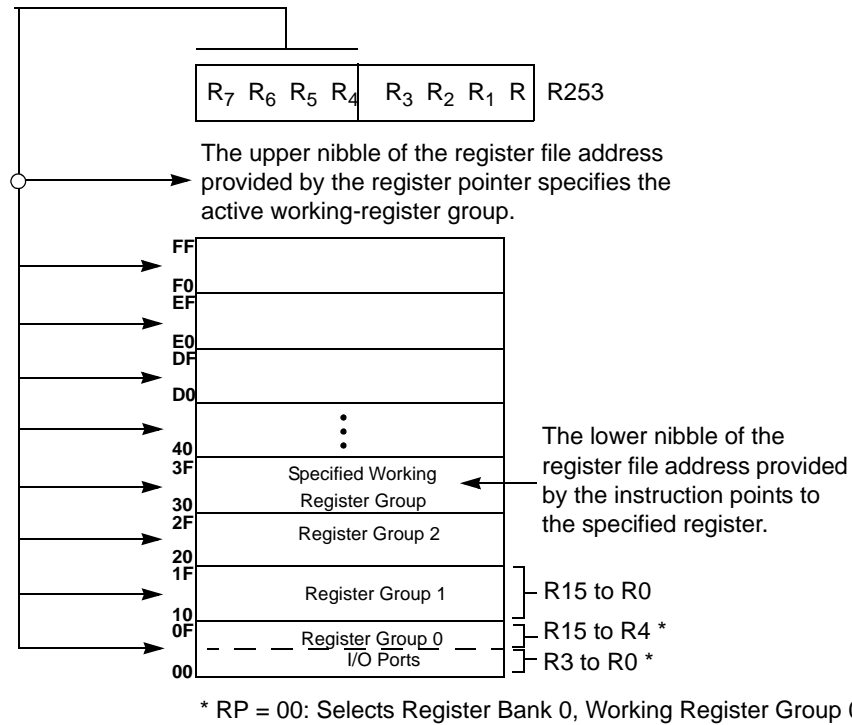


Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

| Field | Bit Position | | Description |
|---------------|--------------|-----|---------------------------|
| T8_Capture_HI | [7:0] | R/W | Captured Data - No Effect |

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

| Field | Bit Position | | Description |
|---------------|--------------|-----|---------------------------|
| T8_Capture_LO | [7:0] | R/W | Captured Data - No Effect |

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

| Field | Bit Position | | Description |
|----------------|--------------|-----|---------------------------|
| T16_Capture_HI | [7:0] | R/W | Captured Data - No Effect |

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

| Field | Bit Position | | Description |
|----------------|--------------|-----|---------------------------|
| T16_Capture_LO | [7:0] | R/W | Captured Data - No Effect |

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

| Field | Bit Position | | Description |
|-------------|--------------|-----|-------------|
| T16_Data_HI | [7:0] | R/W | Data |

Table 13. CTR1(0D)01H T8 and T16 Common Functions (Continued)

| Field | Bit Position | | Value | Description |
|------------------------------------|--------------|-----|-------|------------------------|
| Transmit_Submode/ Glitch_Filter | ----32-- | R/W | | Transmit Mode |
| | | | 00* | Normal Operation |
| | | | 01 | Ping-Pong Mode |
| | | | 10 | T16_Out = 0 |
| | | | 11 | T16_Out = 1 |
| | | | | Demodulation Mode |
| | | | 00* | No Filter |
| | | | 01 | 4 SCLK Cycle |
| | | | 10 | 8 SCLK Cycle |
| | | | 11 | Reserved |
| Initial_T8_Out/ Rising Edge | -----1- | R/W | 0* | Transmit Mode |
| | | | 1 | T8_OUT is 0 Initially |
| | | R | 0* | T8_OUT is 1 Initially |
| | | | 1 | Demodulation Mode |
| | | W | 0 | No Rising Edge |
| | | | 1 | Rising Edge Detected |
| | | | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |
| Initial_T16_Out/ Falling_Edge | -----0 | R/W | 0* | Transmit Mode |
| | | | 1 | T16_OUT is 0 Initially |
| | | R | 0* | T16_OUT is 1 Initially |
| | | | 1 | Demodulation Mode |
| | | W | 0 | No Falling Edge |
| | | | 1 | Falling Edge Detected |
| | | | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |

Note:

*Default at Power-On Reset.

**Default at Power-On Reset. Not reset with Stop Mode recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

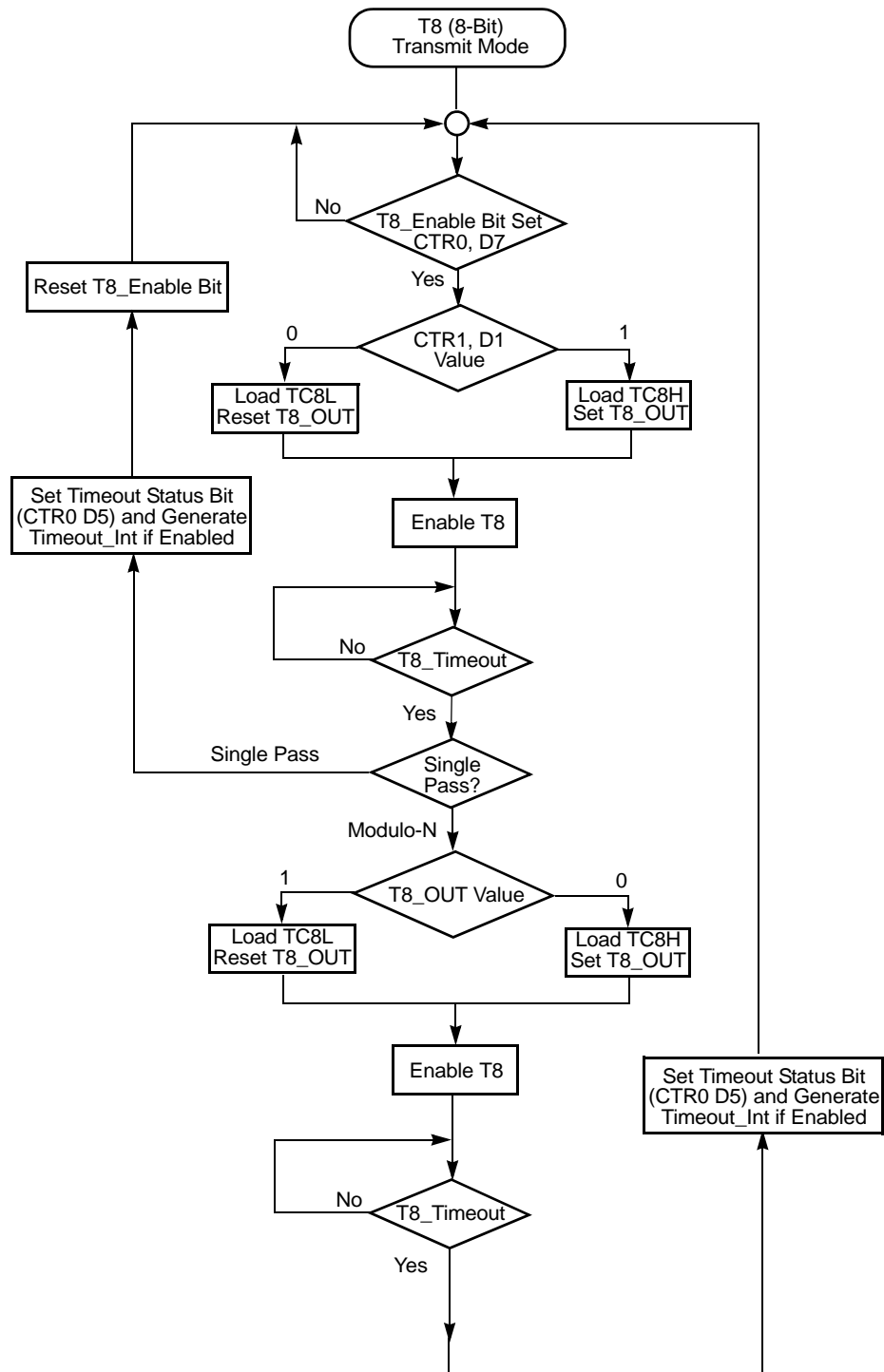


Figure 19. Transmit Mode Flowchart

Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

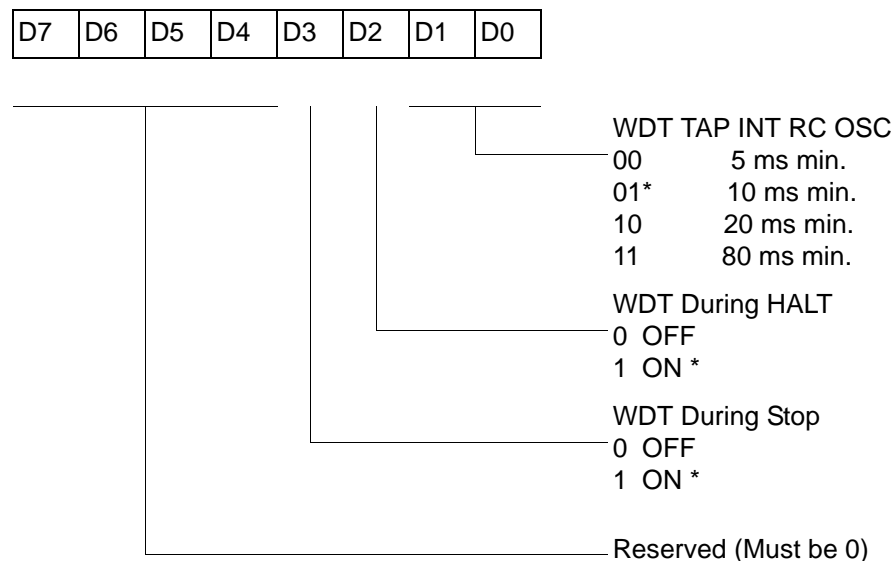
This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 57) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8® CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 20.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

Table 21. EPROM Selectable Options

| | |
|-----------------------------------|--------|
| Port 00–03 Pull-Ups | On/Off |
| Port 04–07 Pull-Ups | On/Off |
| Port 10–13 Pull-Ups | On/Off |
| Port 14–17 Pull-Ups | On/Off |
| Port 20–27 Pull-Ups | On/Off |
| EPROM Protection | On/Off |
| Watch-Dog Timer at Power-On Reset | On/Off |

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO} . A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM} , the RAM content is preserved. When the power level is returned to above V_{BO} , the device performs a POR and functions normally.

CTR1(0D)01H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

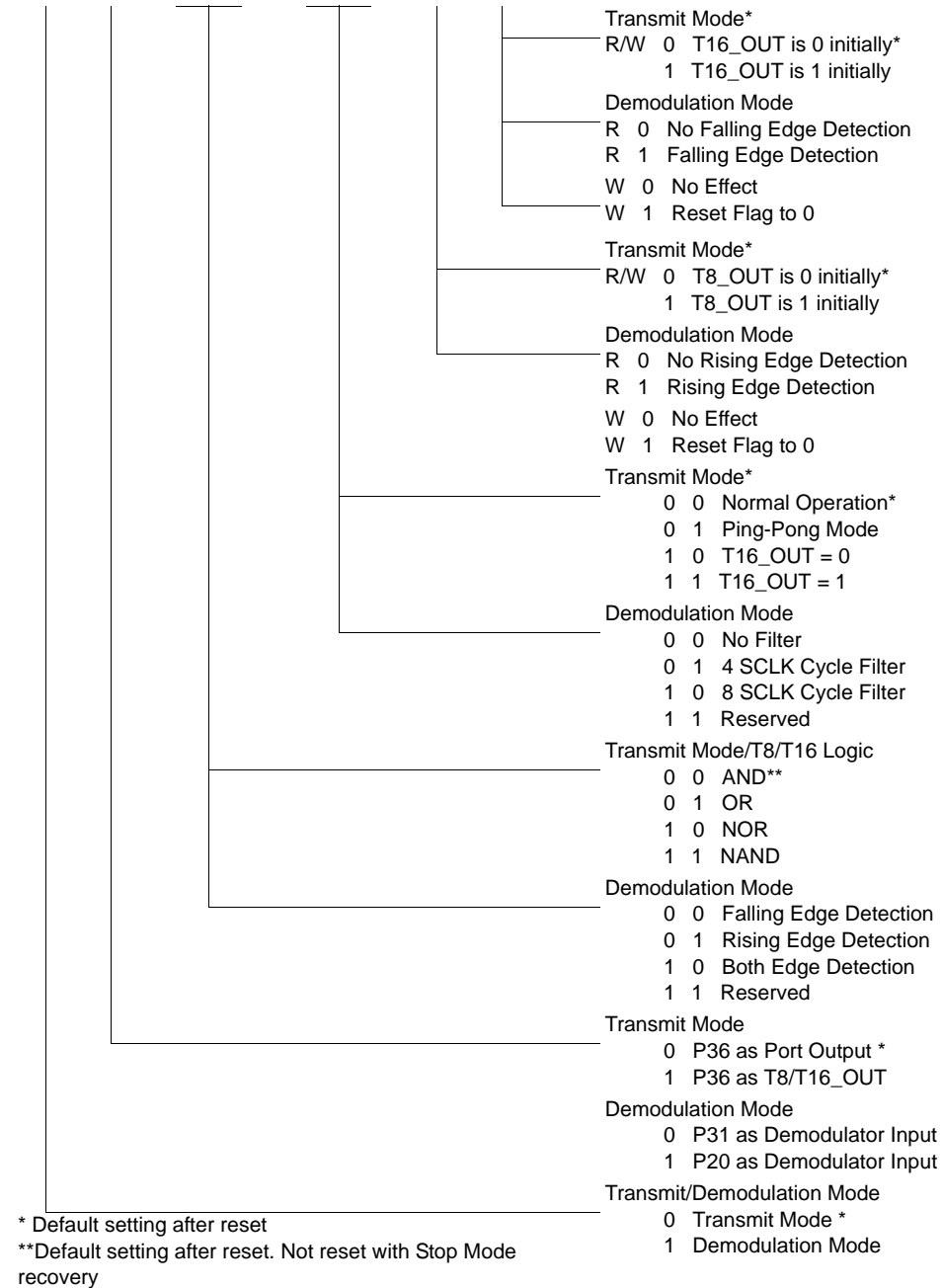
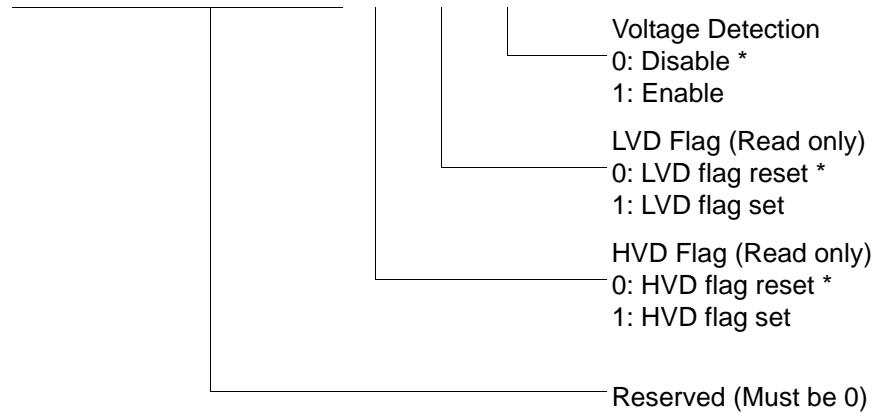


Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

LVD(0D)0CH

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



* Default

Figure 43. Voltage Detection Register

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.

R250 IRQ(FAH)

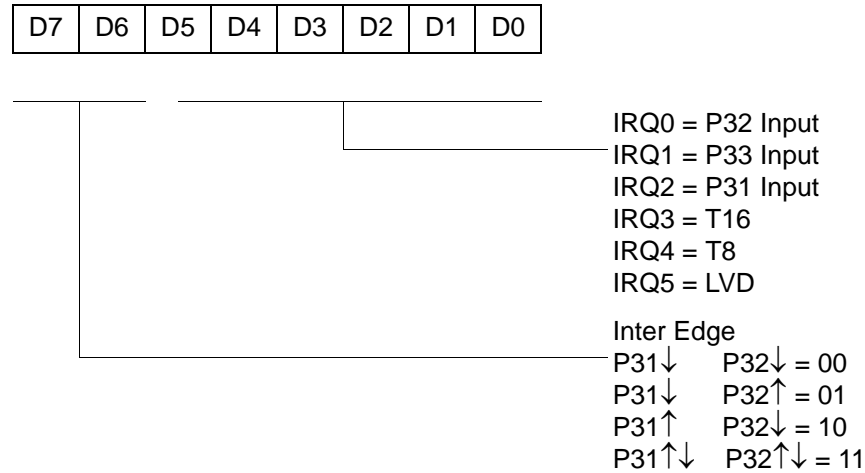
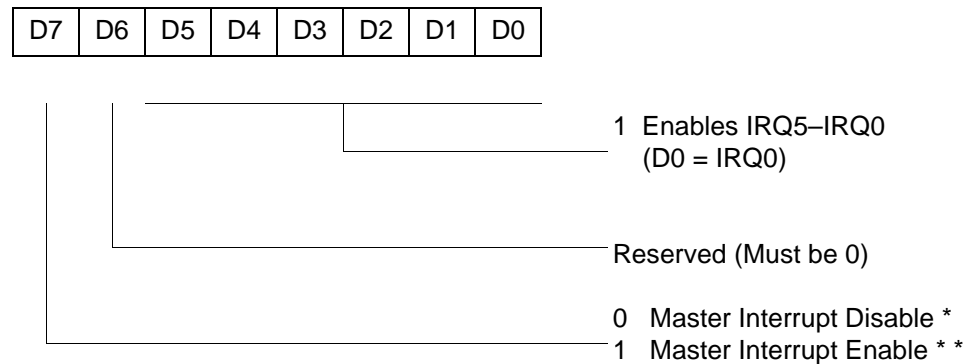


Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset

** Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)

R252 Flags(FCH)

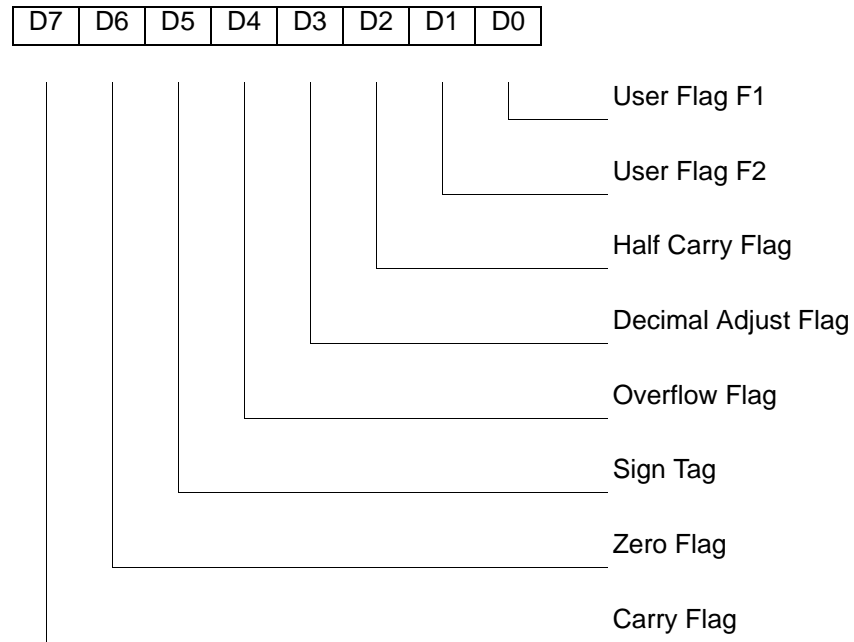
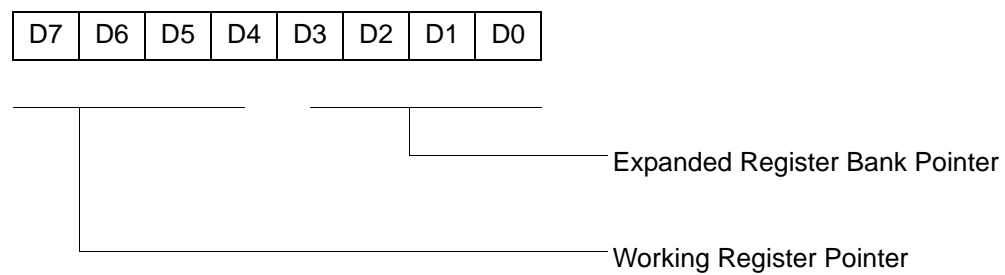


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

E = -40 to +105 degrees C (Extended)

A = -40 to +125 degrees C (Automotive)

P = Package Type:

K = Windowed Cerdip

P = PDIP

H = SSOP

S = SOIC

= Number of Pins

CC = Memory Size

M = Packaging Options

C = Non Lead-Free

G = Lead-Free

E = CDIP