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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323leh4808g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR
- **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K $\Omega$  ±50% at V<sub>CC</sub>=3 V and 450 K $\Omega$  ±50% at  $V_{CC}=2$  V.

# **General Description**

The Z8 GP<sup>TM</sup> OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG<sup>®</sup>'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z8 GP<sup>TM</sup> OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to registermapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8<sup>®</sup> offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of userselectable modes and two on-board comparators to process analog signals with separate reference voltages.

**Note:** All signals with an overline, "", are active Low. For example,  $B/\overline{W}$ , in which WORD is active Low, and  $\overline{B}/W$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.





	Г		<u> </u>		
NC		1	$\cup$	40	⊐ NC
P25		2		39	⊐ P24
P26		3		38	🗖 P23
P27		4		37	⊐ P22
P04		5		36	🗆 P21
P05		6	40-Pi	n 35	⊐ P20
P06		7		34	⊐ P03
P14		8	CDIP	* 33	🗖 P13
P15		9		32	🗆 P12
P07		10		31	⊐ VSS
VDD		11		30	□ P02
P16		12		39	🗆 P11
P17		13		28	⊐ P10
XTAL2		14		27	□ P01
XTAL1		15		26	⊐ P00
P31		16		25	□ Pref1/P30
P32		17		24	⊐ P36
P33		18		23	🗆 P37
P34		19		22	□ P35
NC		20		21	RESET

### Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration

**Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

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NC		1	$\bigcirc$	18	_	NC
DOF		2		40	_	NC
P20		2		4/	_	NC DO4
P26		3		40		P24
P27	q	4		45		P23
P04	Е	5		44		P22
N/C	Е	6		43		P21
P05	q	7		42		P20
P06		8		41		P03
P14	Е	9		40		P13
P15		10		39		P12
P07	С	11	40 D'	38	٦	VSS
VDD	Е	12	48-PIN	37		VSS
VDD	С	13	330P	36		N/C
N/C	C	14		35		P02
P16		15		34		P11
P17		16		33		P10
XTAL2		17		32		P01
XTAL1		18		31		P00
P31		19		30		N/C
P32		20		29		PREF1/P30
P33		21		28		P36
P34		22		27		P37
NC		23		26	3	P35
VSS	P	24		25		RESET
	_	24		20		

Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12

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#### Table 9. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	25			Cycles	1

Notes:

1. For windowed cerdip package only.

2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

AF = exp[(Ea/k)\*(1/Tuse - 1/TStress)] Where: Ea is the intrinsic activation energy (eV; typ. 0.8) k is Boltzman's constant (8.67 x 10-5 eV/°K) °K = -273.16°C Tuse = Use Temperature in °K TStress = Stress Temperature in °K 3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>





Figure 11. Port 2 Configuration

### Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.







\* RP = 00: Selects Register Bank 0, Working Register Group 0

Figure 17. Register Pointer—Detail

### Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

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Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16\_OUT in Modulo-N Mode

#### **T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

#### If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).



### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

#### **Ping-Pong Mode**

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1, D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16\_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

**Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

#### **Power-On Reset**

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows  $V_{DD}$  and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V<sub>BO</sub> Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

#### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

#### **STOP Mode**

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10  $\mu$ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:



#### Table 19. Stop Mode Recovery Source

SMR:432			Operation			
D4	D3	D2	Description of Action			
0	0	0	POR and/or external reset recovery			
0	0	1	Reserved			
0	1	0	P31 transition			
0	1	1	P32 transition			
1	0	0	P33 transition			
1	0	1	P27 transition			
1	1	0	Logical NOR of P20 through P23			
1	1	1	Logical NOR of P20 through P27			

**Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 59 for other recover sources.

#### Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the  $T_{POR}$  delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

**Note:** It is recommended that this bit be set to 1 if using a crystal or resonator clock source. The  $T_{POR}$  delay allows the clock source to stabilize before executing instructions.

#### Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

#### Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).



#### Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8<sup>®</sup> CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



\* Default setting after reset

#### Figure 37. Watch-Dog Timer Mode Register (Write Only)

#### WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 20.



#### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

#### **EPROM Selectable Options**

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

#### Table 21. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

#### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V<sub>DD</sub> is at the required level for correct operation of the device. Reset is globally driven when V<sub>DD</sub> falls below V<sub>BO</sub>. A small drop in V<sub>DD</sub> causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V<sub>DD</sub> is allowed to stay above V<sub>RAM</sub>, the RAM content is preserved. When the power level is returned to above V<sub>BO</sub>, the device performs a POR and functions normally.





**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



### PCON(0F)00H



\* Default setting after reset

#### Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)





Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset

\* \* At the XOR gate input





#### WDTMR(0F)0FH



\* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

# **Standard Control Registers**

#### R246 P2M(F6H)



\* Default setting after reset

#### Figure 48. Port 2 Mode Register (F6H: Write Only)



#### R248 P01M(F8H)



\* Default setting after reset; only P00, P01 and P07 are available in 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)







Figure 68. 48-Pin SSOP Package Design

**Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

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### **Precharacterization Product**

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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