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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323leh4816c00tr">https://www.e-xfl.com/product-detail/zilog/zgp323leh4816c00tr</a>



# Table of Contents

Development Features .....	1
General Description .....	2
Pin Description .....	4
Absolute Maximum Ratings .....	10
Standard Test Conditions .....	10
DC Characteristics .....	11
AC Characteristics .....	14
Pin Functions .....	16
XTAL1 Crystal 1 (Time-Based Input) .....	16
XTAL2 Crystal 2 (Time-Based Output) .....	16
Port 0 (P07–P00) .....	16
Port 1 (P17–P10) .....	17
Port 2 (P27–P20) .....	18
Port 3 (P37–P30) .....	19
RESET (Input, Active Low) .....	23
Functional Description .....	23
Program Memory .....	23
RAM .....	23
Expanded Register File .....	24
Register File .....	28
Stack .....	29
Timers .....	30
Counter/Timer Functional Blocks .....	38
Expanded Register File Control Registers (0D) .....	64
Expanded Register File Control Registers (0F) .....	69
Standard Control Registers .....	73
Package Information .....	80
Ordering Information .....	89
Precharacterization Product .....	95



Figure 35. Stop Mode Recovery Source . . . . .	57
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only) . . .	59
Figure 37. Watch-Dog Timer Mode Register (Write Only) . . . . .	60
Figure 38. Resets and WDT . . . . .	61
Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted) . . .	64
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write) . . .	65
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted) . . .	67
Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted) . . . . .	68
Figure 43. Voltage Detection Register . . . . .	69
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only) . . . . .	70
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only) . . . . .	71
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only) . . .	72
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only) . . . . .	73
Figure 48. Port 2 Mode Register (F6H: Write Only) . . . . .	73
Figure 49. Port 3 Mode Register (F7H: Write Only) . . . . .	74
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only) . . . . .	75
Figure 51. Interrupt Priority Register (F9H: Write Only) . . . . .	76
Figure 52. Interrupt Request Register (FAH: Read/Write) . . . . .	77
Figure 53. Interrupt Mask Register (FBH: Read/Write) . . . . .	77
Figure 54. Flag Register (FCH: Read/Write) . . . . .	78
Figure 55. Register Pointer (FDH: Read/Write) . . . . .	78
Figure 56. Stack Pointer High (FEH: Read/Write) . . . . .	79
Figure 57. Stack Pointer Low (FFH: Read/Write) . . . . .	79
Figure 58. 20-Pin CDIP Package . . . . .	80
Figure 59. 20-Pin PDIP Package Diagram . . . . .	81
Figure 60. 20-Pin SOIC Package Diagram . . . . .	81
Figure 61. 20-Pin SSOP Package Diagram . . . . .	82
Figure 62. 28-Pin CDIP Package . . . . .	83
Figure 63. 28-Pin SOIC Package Diagram . . . . .	84
Figure 64. 28-Pin PDIP Package Diagram . . . . .	85
Figure 65. 28-Pin SSOP Package Diagram . . . . .	86
Figure 66. 40-Pin CDIP Package . . . . .	87
Figure 67. 40-Pin PDIP Package Diagram . . . . .	87
Figure 68. 48-Pin SSOP Package Design . . . . .	88

- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

► **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K $\Omega$   $\pm$ 50% at  $V_{CC}$ =3 V and 450 K $\Omega$   $\pm$ 50% at  $V_{CC}$ =2 V.

## General Description

The Z8 GP™ OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

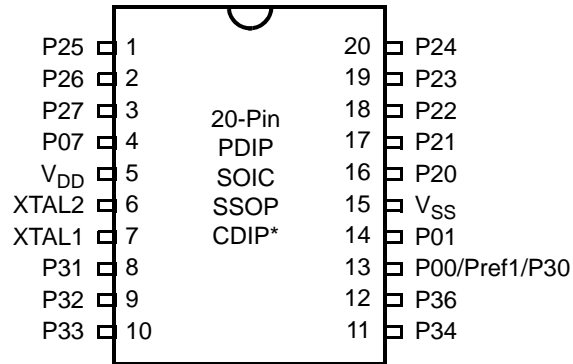
The Z8 GP™ OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, " $\overline{\phantom{x}}$ ", are active Low. For example,  $\overline{B/W}$ , in which WORD is active Low, and  $\overline{B/W}$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.



**Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration**

**Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Identification**

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

## Capacitance

Table 7 lists the capacitances.

**Table 7. Capacitance**

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ\text{C}$ , $V_{CC} = \text{GND} = 0\text{V}$ , $f = 1.0\text{MHz}$ , unmeasured pins returned to GND	

## DC Characteristics

**Table 8. DC Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ	Max			
$V_{CC}$	Supply Voltage		2.0		3.6	V	See Note 5	5
$V_{CH}$	Clock Input High Voltage	2.0-3.6	0.8		$V_{CC}+0.3$	V	Driven by External Clock Generator	
$V_{CL}$	Clock Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		0.5	V	Driven by External Clock Generator	
$V_{IH}$	Input High Voltage	2.0-3.6	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
$V_{IL}$	Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
$V_{OH1}$	Output High Voltage	2.0-3.6	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
$V_{OH2}$	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
$V_{OL1}$	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 1.0\text{mA}$ $I_{OL} = 4.0\text{mA}$	
$V_{OL2}$	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	$I_{OL} = 10\text{mA}$	
$V_{OFFSET}$	Comparator Input Offset Voltage	2.0-3.6			25	mV		
$V_{REF}$	Comparator Reference Voltage	2.0-3.6	0		$V_{DD}$ -1.75	V		
$I_{IL}$	Input Leakage	2.0-3.6	-1		1	$\mu\text{A}$	$V_{IN} = 0\text{V}$ , $V_{CC}$ Pull-ups disabled	
$I_{OL}$	Output Leakage	2.0-3.6	-1		1	$\mu\text{A}$	$V_{IN} = 0\text{V}$ , $V_{CC}$	
$I_{CC}$	Supply Current	2.0			10	mA	at 8.0 MHz	1, 2
		3.6			15	mA	at 8.0 MHz	1, 2

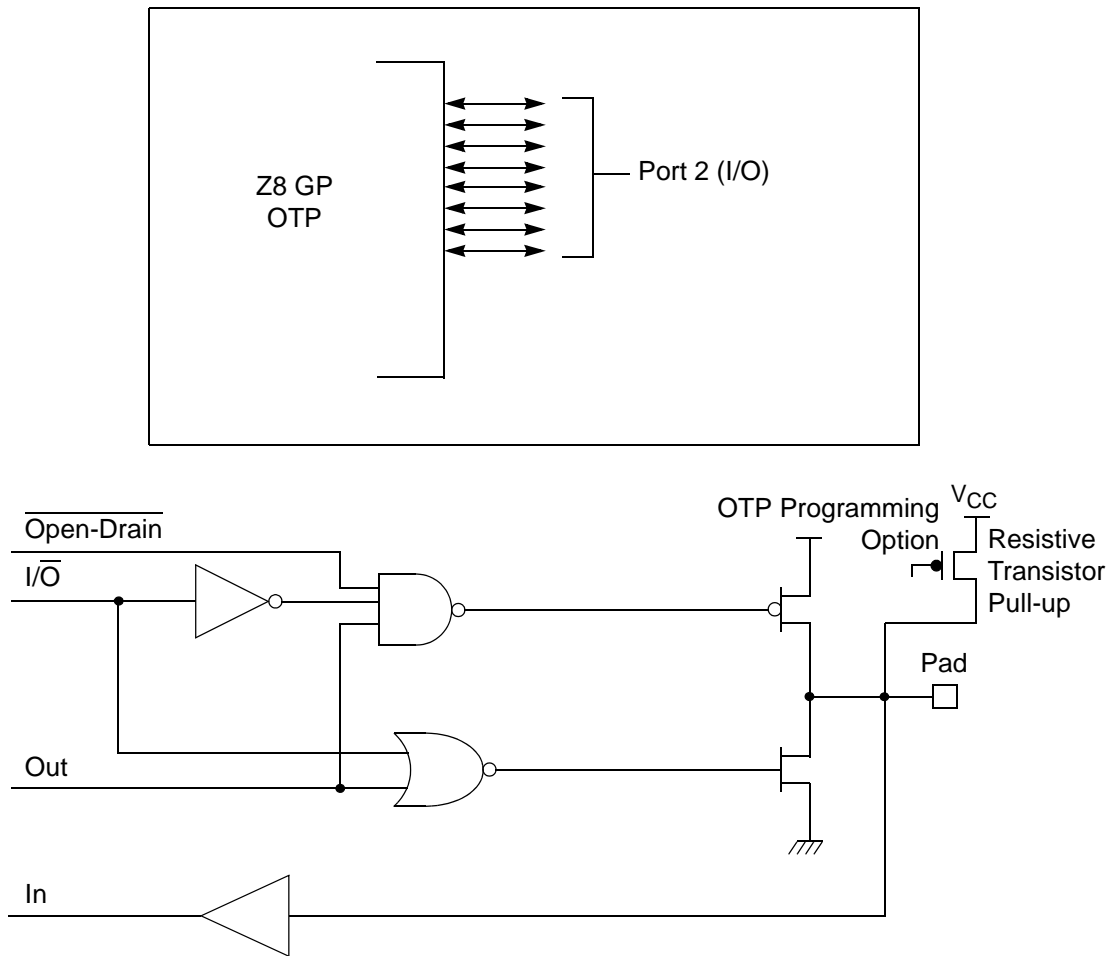


Figure 11. Port 2 Configuration

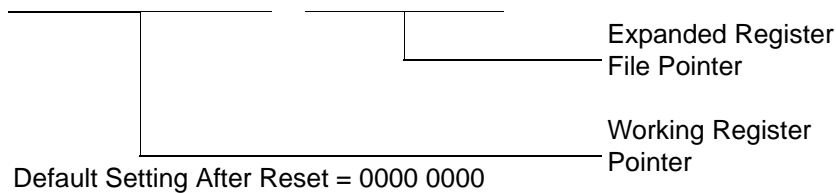
### Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



**Figure 16. Register Pointer**

**Example: Z8 GP: (See Figure 15 on page 26)**

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTRL0

R1 = CTRL1

R2 = CTRL2

R3 = Reserved

Table 14. CTR2(D)02H: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Transmit Mode
			1	Modulo-N
			0	Single Pass
			1	Demodulation Mode
Time_Out	--5-----	R	0*	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect
			01	Reset Flag to 0
			10	SCLK
			11	SCLK/2
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4
			1	SCLK/8
Counter_INT_Mask	-----1-	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.

**Note:**

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

**T16\_Enable**

This field enables T16 when set to 1.

**Single/Modulo-N**

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 45.

### Time\_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

### T16\_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

### Capture\_INT\_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

### Counter\_INT\_Mask

Set this bit to allow an interrupt when T16 times out.

### P35\_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

## CTR3 T8/T16 Control Register—CTR3(D)03H

Table 15 lists and briefly describes the fields for this register. This register allows the T<sub>8</sub> and T<sub>16</sub> counters to be synchronized.

**Table 15. CTR3 (D)03H: T8/T16 Control Register**

Field	Bit Position		Value	Description
T <sub>16</sub> Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T <sub>8</sub> Enable	-6-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows  $V_{DD}$  and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from  $V_{BO}$  Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10  $\mu$ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

### Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position	Description		
LVD	76543---	Reserved No Effect		
	----2--	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

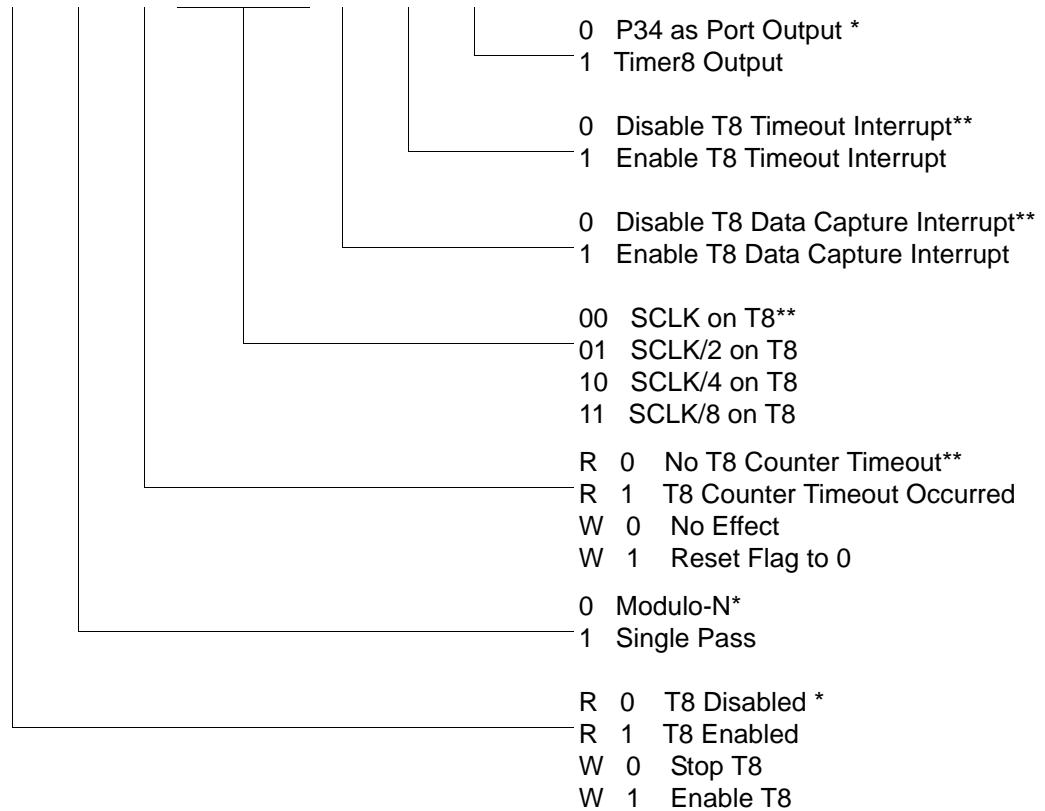
- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

## Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset

\*\*Default setting after reset. Not reset with Stop Mode recovery.

**Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)**

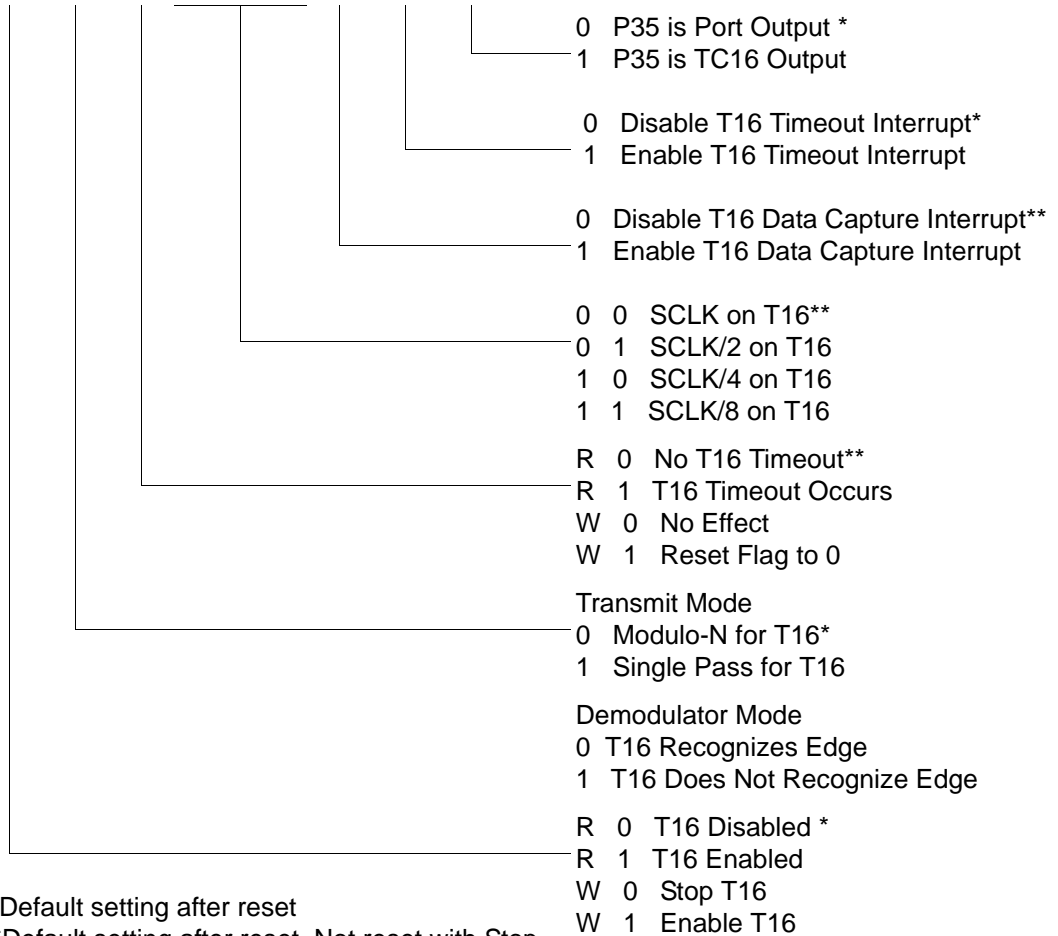


- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



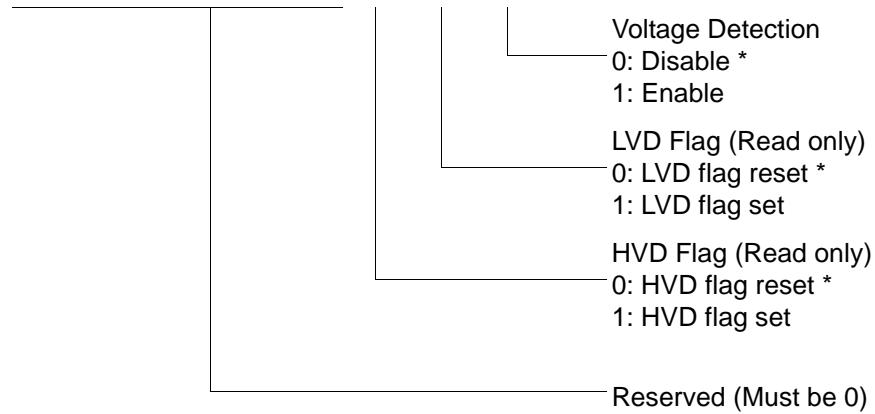
\* Default setting after reset

\*\*Default setting after reset. Not reset with Stop Mode recovery.

**Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

LVD(0D)0CH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default

**Figure 43. Voltage Detection Register**

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

## Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.

R249 IPR(F9H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

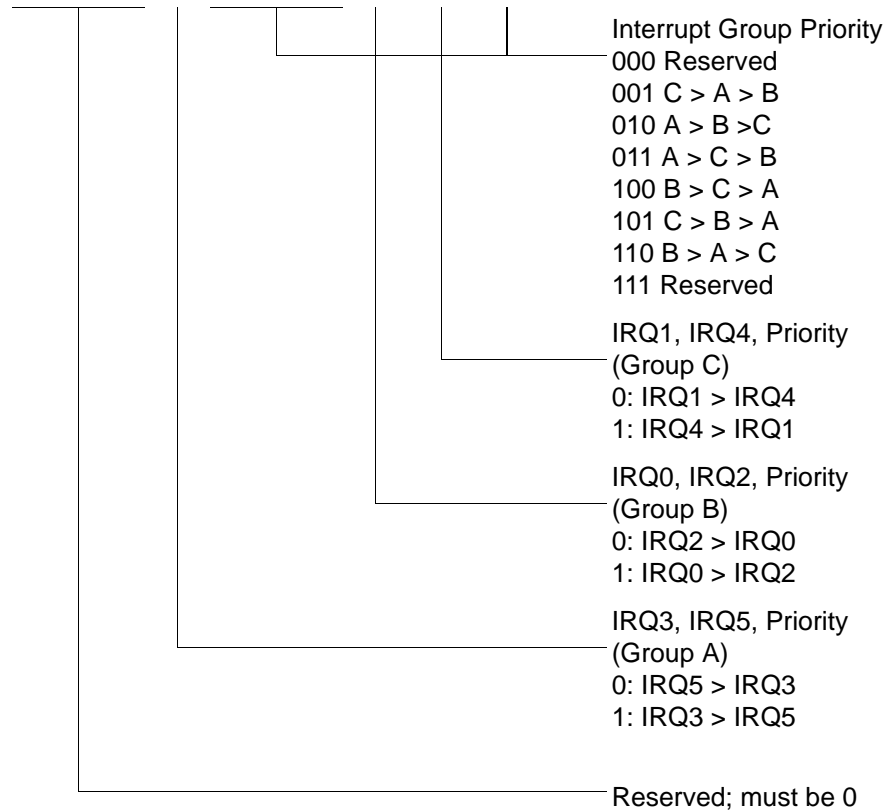
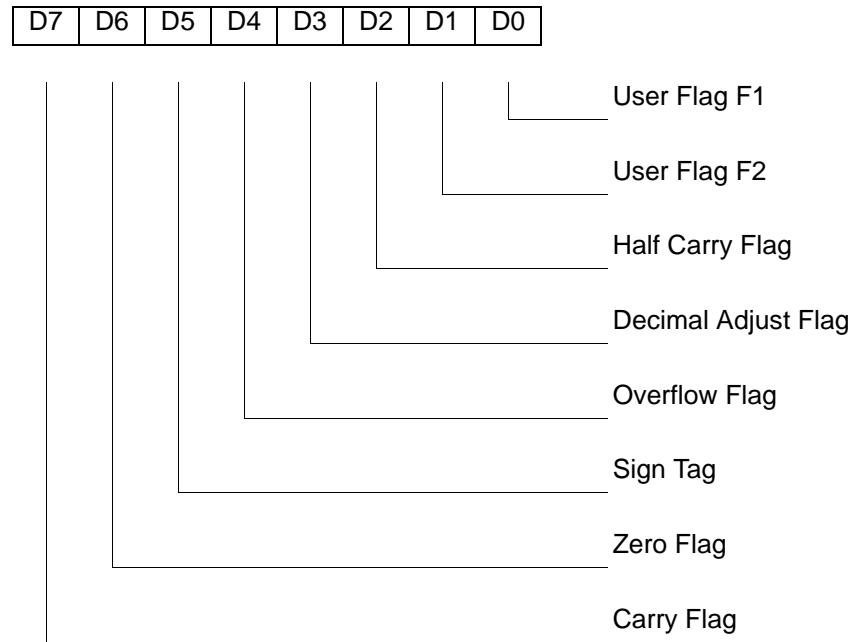


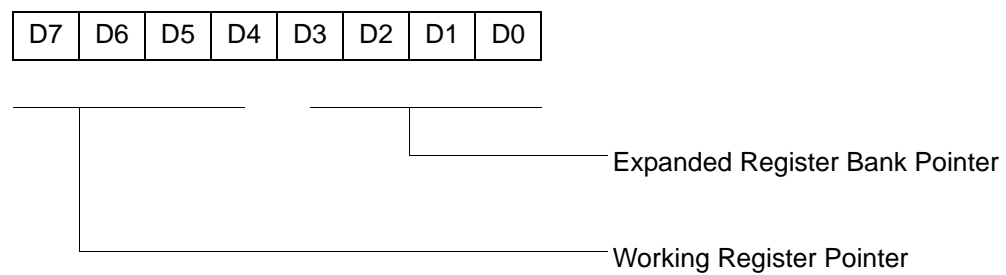
Figure 51. Interrupt Priority Register (F9H: Write Only)

### R252 Flags(FCH)



**Figure 54. Flag Register (FCH: Read/Write)**

### R253 RP(FDH)



Default setting after reset = 0000 0000

**Figure 55. Register Pointer (FDH: Read/Write)**

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**4KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323LSH4804C	48-pin SSOP 4K OTP	ZGP323LSS2804C	28-pin SOIC 4K OTP
ZGP323LSP4004C	40-pin PDIP 4K OTP	ZGP323LSH2004C	20-pin SSOP 4K OTP
ZGP323LSH2804C	28-pin SSOP 4K OTP	ZGP323LSP2004C	20-pin PDIP 4K OTP
ZGP323LSP2804C	28-pin PDIP 4K OTP	ZGP323LSS2004C	20-pin SOIC 4K OTP

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**4KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323LEH4804C	48-pin SSOP 4K OTP	ZGP323LES2804C	28-pin SOIC 4K OTP
ZGP323LEP4004C	40-pin PDIP 4K OTP	ZGP323LEH2004C	20-pin SSOP 4K OTP
ZGP323LEH2804C	28-pin SSOP 4K OTP	ZGP323LEP2004C	20-pin PDIP 4K OTP
ZGP323LEP2804C	28-pin PDIP 4K OTP	ZGP323LES2004C	20-pin SOIC 4K OTP

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**4KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323LAH4804C	48-pin SSOP 4K OTP	ZGP323LAS2804C	28-pin SOIC 4K OTP
ZGP323LAP4004C	40-pin PDIP 4K OTP	ZGP323LAH2004C	20-pin SSOP 4K OTP
ZGP323LAH2804C	28-pin SSOP 4K OTP	ZGP323LAP2004C	20-pin PDIP 4K OTP
ZGP323LAP2804C	28-pin PDIP 4K OTP	ZGP323LAS2004C	20-pin SOIC 4K OTP

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Note: Replace C with G for Lead-Free Packaging

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**Additional Components**

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer	ZGP32300100ZPR	Programming System

## **M**

memory, program 23  
 modulo-N mode  
     T16\_OUT 45  
     T8\_OUT 41

## **O**

oscillator configuration 51  
 output circuit, counter/timer 47

## **P**

package information  
     20-pin DIP package diagram 81  
     20-pin SSOP package diagram 82  
     28-pin DIP package diagram 85  
     28-pin SOIC package diagram 84  
     28-pin SSOP package diagram 86  
     40-pin DIP package diagram 87  
     48-pin SSOP package diagram 88  
 pin configuration  
     20-pin DIP/SOIC/SSOP 5  
     28-pin DIP/SOIC/SSOP 6  
     40- and 48-pin 8  
     40-pin DIP 7  
     48-pin SSOP 8  
 pin functions  
     port 0 (P07 - P00) 16  
     port 0 (P17 - P10) 17  
     port 0 configuration 17  
     port 1 configuration 18  
     port 2 (P27 - P20) 18  
     port 2 (P37 - P30) 19  
     port 2 configuration 19  
     port 3 configuration 20  
     port 3 counter/timer configuration 22  
     reset) 23  
     XTAL1 (time-based input 16  
     XTAL2 (time-based output) 16  
 ping-pong mode 46  
 port 0 configuration 17  
 port 0 pin function 16

port 1 configuration 18  
 port 1 pin function 17  
 port 2 configuration 19  
 port 2 pin function 18  
 port 3 configuration 20  
 port 3 pin function 19  
 port 3 counter/timer configuration 22  
 port configuration register 53  
 power connections 3  
 power supply 5  
 precharacterization product 95  
 program memory 23  
     map 24

## **R**

ratings, absolute maximum 10  
 register 59  
     CTR(D)01h 33  
     CTR0(D)00h 31  
     CTR2(D)02h 35  
     CTR3(D)03h 37  
     flag 78  
     HI16(D)09h 30  
     HI8(D)0Bh 30  
     interrupt priority 76  
     interrupt request 77  
     interruptmask 77  
     L016(D)08h 30  
     L08(D)0Ah 30  
     LVD(D)0Ch 63  
     pointer 78  
     port 0 and 1 75  
     port 2 configuration 73  
     port 3 mode 74  
     port configuration 53, 73  
     SMR2(F)0Dh 38  
     stack pointer high 79  
     stack pointer low 79  
     stop mode recovery 55  
     stop mode recovery 2 59  
     stop-mode recovery 71  
     stop-mode recovery 2 72  
     T16 control 67

- T8 and T16 common control functions 65
- T8/T16 control 68
- TC16H(D)07h 30
- TC16L(D)06h 31
- TC8 control 64
- TC8H(D)05h 31
- TC8L(D)04h 31
- voltage detection 69
- watch-dog timer 73
- register description
  - Counter/Timer2 LS-Byte Hold 31
  - Counter/Timer2 MS-Byte Hold 30
  - Counter/Timer8 Control 31
  - Counter/Timer8 High Hold 31
  - Counter/Timer8 Low Hold 31
  - CTR2 Counter/Timer 16 Control 35
  - CTR3 T8/T16 Control 37
  - Stop Mode Recovery2 38
  - T16\_Capture\_LO 30
  - T8 and T16 Common functions 33
  - T8\_Capture\_HI 30
  - T8\_Capture\_LO 30
- register file 28
  - expanded 24
- register pointer 27
  - detail 29
- reset pin function 23
- resets and WDT 61

## S

- SCLK circuit 56
- single-pass mode
  - T16\_OUT 45
  - T8\_OUT 41
- stack 29
- standard test conditions 10
- standby modes 1
- stop instruction, counter/timer 52
- stop mode recovery
  - 2 register 59
  - source 57
- stop mode recovery 2 59
- stop mode recovery register 55

## T

- T16 transmit mode 44
- T16\_Capture\_HI 30
- T8 transmit mode 38
- T8\_Capture\_HI 30
- test conditions, standard 10
- test load diagram 10
- timing diagram, AC 14
- transmit mode flowchart 39

## V

- VCC 5
- voltage
  - brown-out/standby 62
  - detection and flags 63
- voltage detection register 69

## W

- watch-dog timer
  - mode registerwatch-dog timer mode register 60
  - time select 61

## X

- XTAL1 5
- XTAL1 pin function 16
- XTAL2 5
- XTAL2 pin function 16