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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.600", 15.24mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323lep2804c |



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Development Features

Table 1 lists the features of ZiLOG®'s Z8 GP™ OTP MCU Family family members.

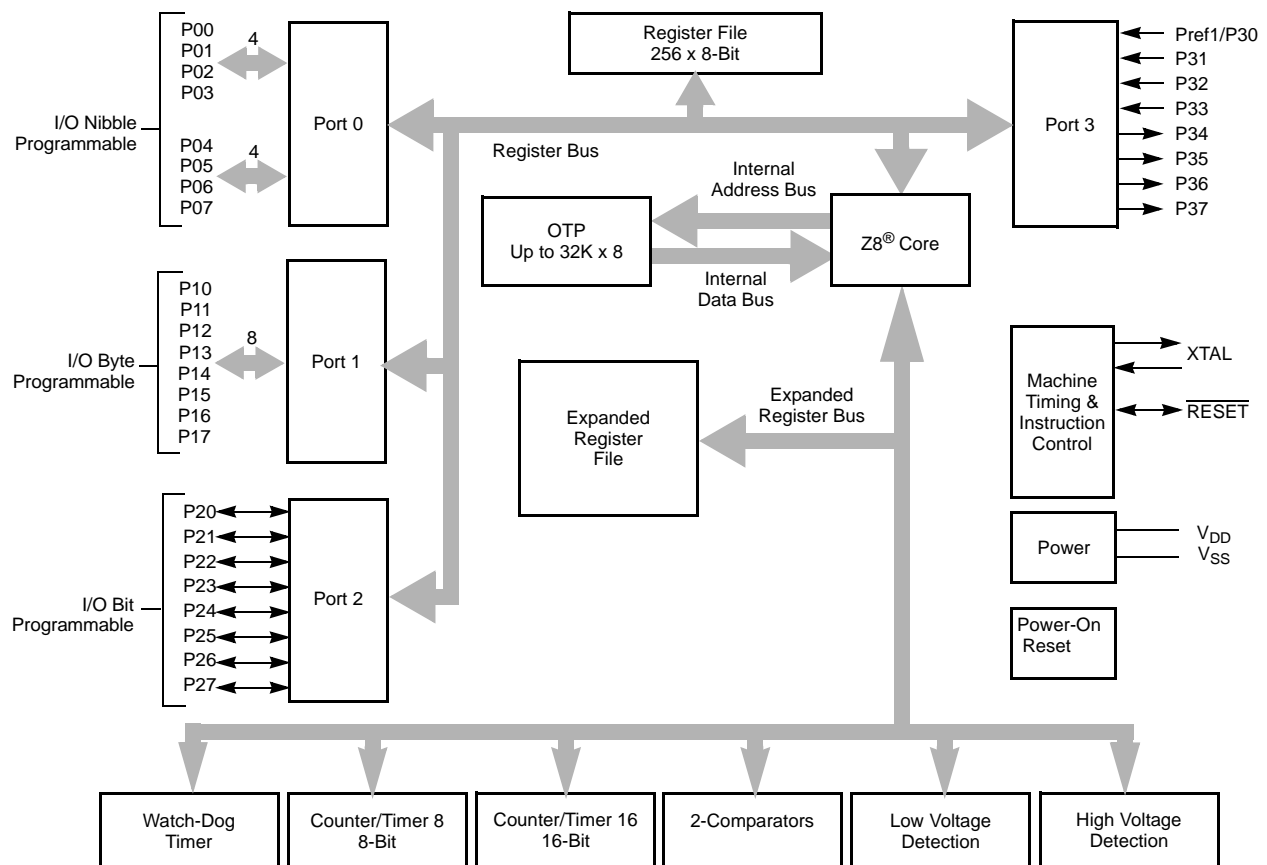
Table 1. Features

| Device | OTP (KB) | RAM (Bytes) | I/O Lines | Voltage Range |
|------------------------|--------------|-------------|--------------|---------------|
| ZGP323L OTP MCU Family | 4, 8, 16, 32 | 237 | 32, 24 or 16 | 2.0V–3.6V |

- Low power consumption—6mW (typical)
- T = Temperature
S = Standard 0° to +70°C
E = Extended -40° to +105°C
A = Automotive -40° to +125°C
- Three standby modes:
 - STOP—2μA (typical)
 - HALT—0.8mA (typical)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors

Table 2. Power Connections

| Connection | Circuit | Device |
|------------|-----------------|-----------------|
| Power | V _{CC} | V _{DD} |
| Ground | GND | V _{SS} |



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

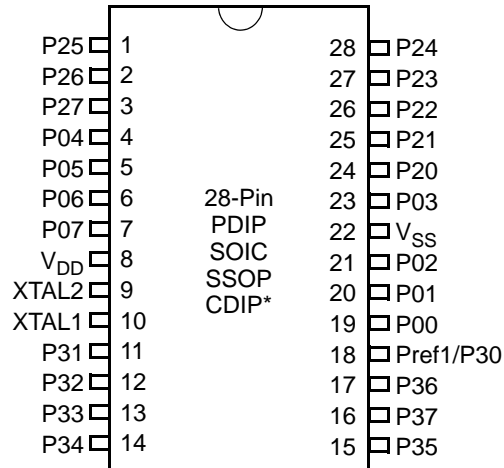


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

| Pin | Symbol | Direction | Description |
|-------|---------------------------|--------------|---------------------------------------------------------------------------------|
| 1-3 | P25-P27 | Input/Output | Port 2, Bits 5,6,7 |
| 4-7 | P04-P07 | Input/Output | Port 0, Bits 4,5,6,7 |
| 8 | V _{DD} | | Power supply |
| 9 | XTAL2 | Output | Crystal, oscillator clock |
| 10 | XTAL1 | Input | Crystal, oscillator clock |
| 11-13 | P31-P33 | Input | Port 3, Bits 1,2,3 |
| 14 | P34 | Output | Port 3, Bit 4 |
| 15 | P35 | Output | Port 3, Bit 5 |
| 16 | P37 | Output | Port 3, Bit 7 |
| 17 | P36 | Output | Port 3, Bit 6 |
| 18 | Pref1/P30 Port 3 Bit 0 | Input | Analog ref input; connect to V _{CC} if not used Input for Pref1/P30 |
| 19-21 | P00-P02 | Input/Output | Port 0, Bits 0,1,2 |
| 22 | V _{SS} | | Ground |
| 23 | P03 | Input/Output | Port 0, Bit 3 |
| 24-28 | P20-P24 | Input/Output | Port 2, Bits 0-4 |

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Absolute Maximum Ratings

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 6. Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Units | Notes |
|-----------------------------------------------------|---------|---------|---------|-------|
| Ambient temperature under bias | 0 | +70 | C | |
| Storage temperature | -65 | +150 | C | |
| Voltage on any pin with respect to V_{SS} | -0.3 | +5.5 | V | 1 |
| Voltage on V_{DD} pin with respect to V_{SS} | -0.3 | +3.6 | V | |
| Maximum current on input and/or inactive output pin | -5 | +5 | μ A | |
| Maximum output current from active output pin | -25 | +25 | mA | |
| Maximum current into V_{DD} or out of V_{SS} | | 75 | mA | |

Notes:
This voltage applies to all pins except the following: V_{DD} , P32, P33 and $\overline{\text{RESET}}$.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

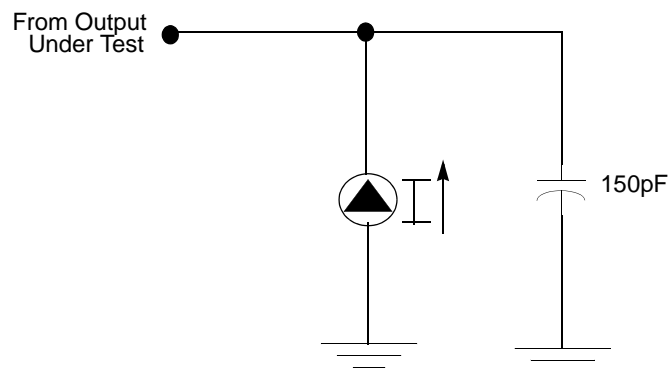


Figure 7. Test Load Diagram

CTR1(0D)01H" on page 33). Other edge detect and IRQ modes are described in Table 11.

- **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Table 11. Port 3 Pin Function Summary

| Pin | I/O | Counter/Timers | Comparator | Interrupt |
|-----------|-----|----------------|------------|-----------|
| Pref1/P30 | IN | | RF1 | |
| P31 | IN | IN | AN1 | IRQ2 |
| P32 | IN | | AN2 | IRQ0 |
| P33 | IN | | RF2 | IRQ1 |
| P34 | OUT | T8 | AO1 | |
| P35 | OUT | T16 | | |
| P36 | OUT | T8/16 | | |
| P37 | OUT | | AO2 | |
| P20 | I/O | IN | | |

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)

| Field | Bit Position | | Value | Description |
|----------|--------------|---|-------|--------------------|
| Reserved | ---43210 | R | 1 | Always reads 11111 |
| | | W | x | No Effect |

Note: *Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

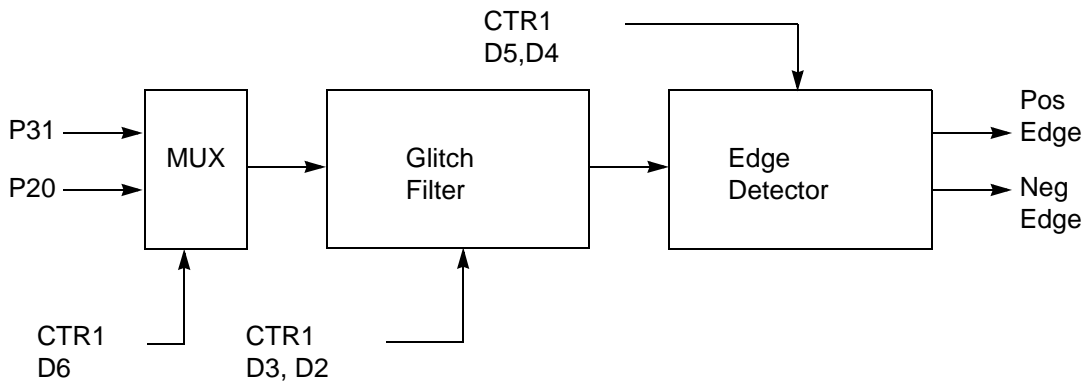


Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.

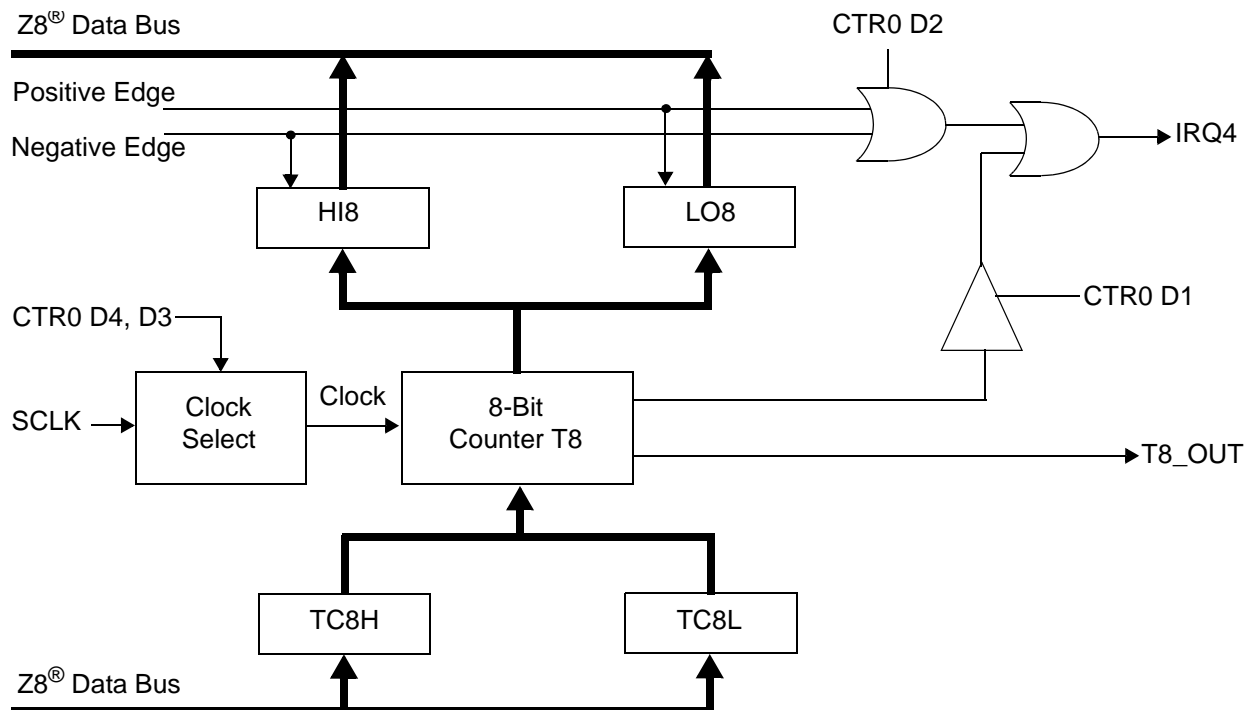


Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.*

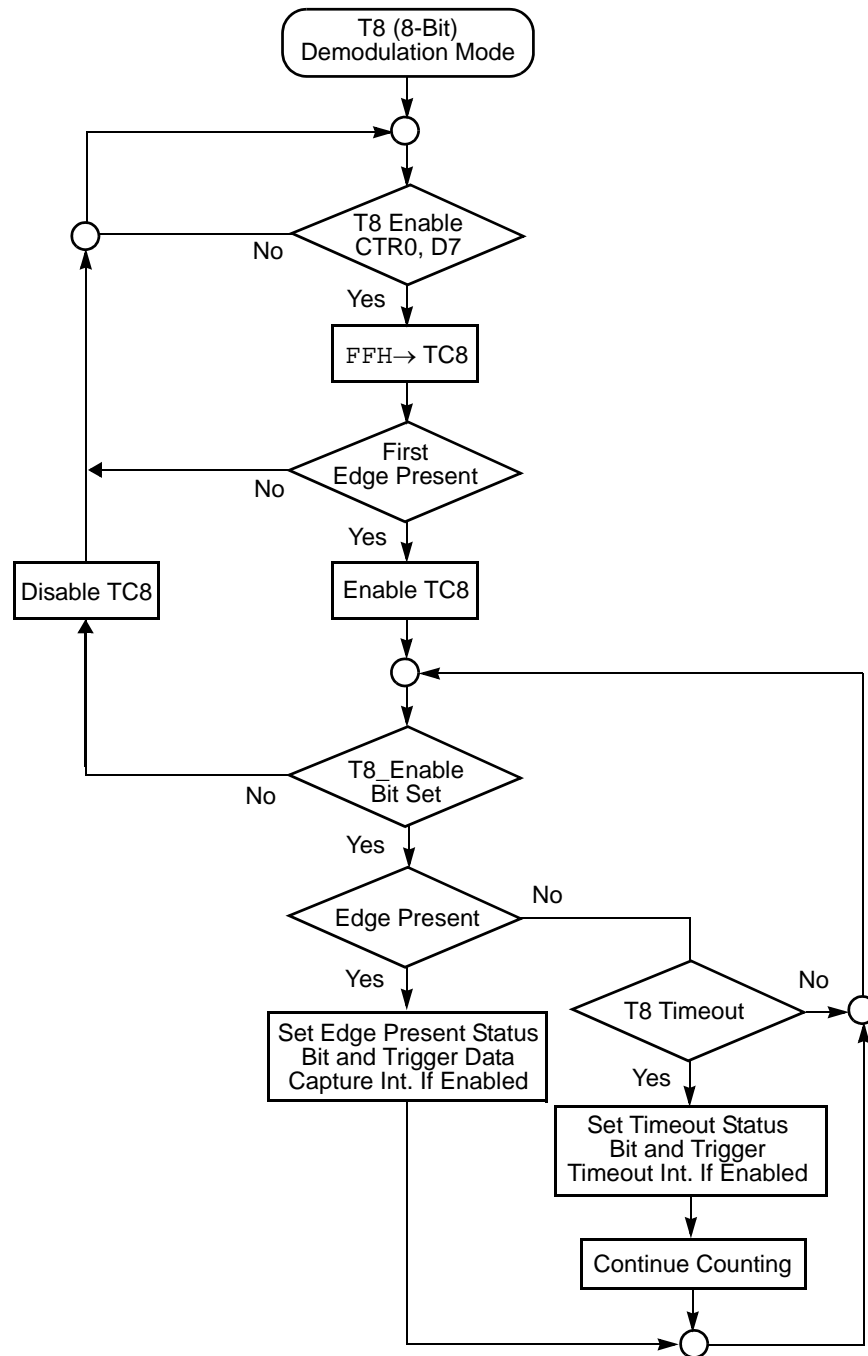


Figure 24. Demodulation Mode Flowchart

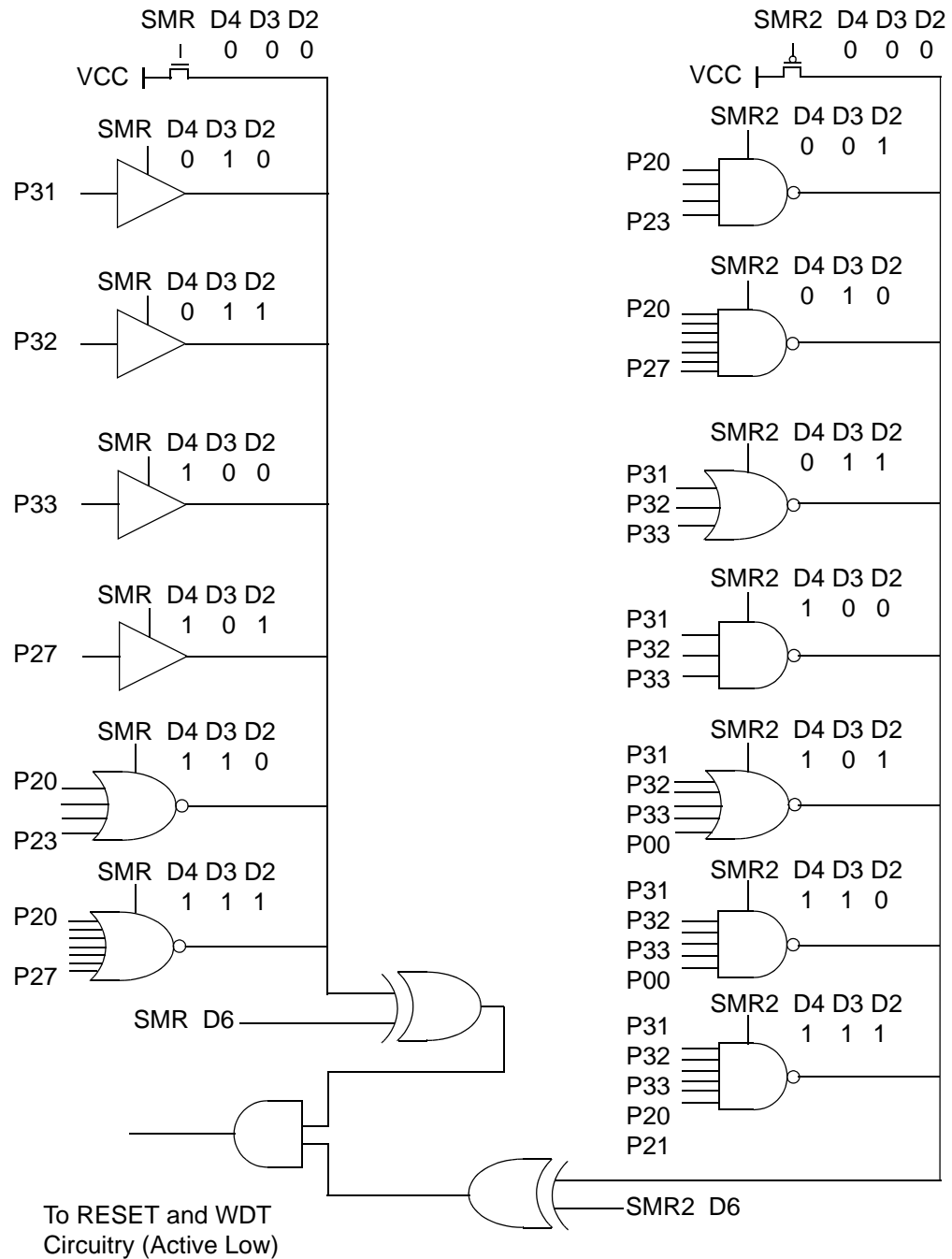


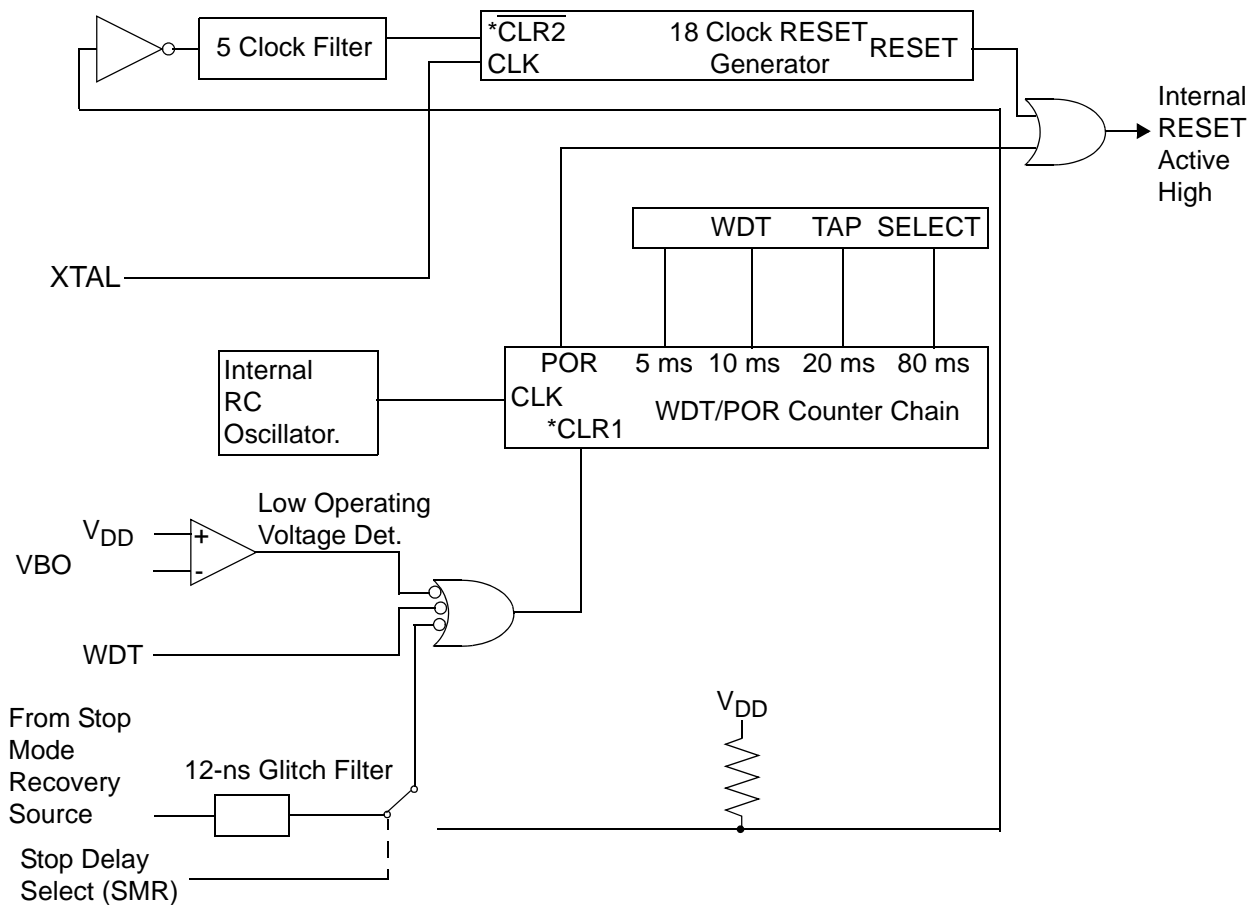
Figure 35. Stop Mode Recovery Source

Table 20. Watch-Dog Timer Time Select

| D1 | D0 | Timeout of Internal RC-Oscillator |
|----|----|-----------------------------------|
| 0 | 0 | 5ms min. |
| 0 | 1 | 10ms min. |
| 1 | 0 | 20ms min. |
| 1 | 1 | 80ms min. |

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.

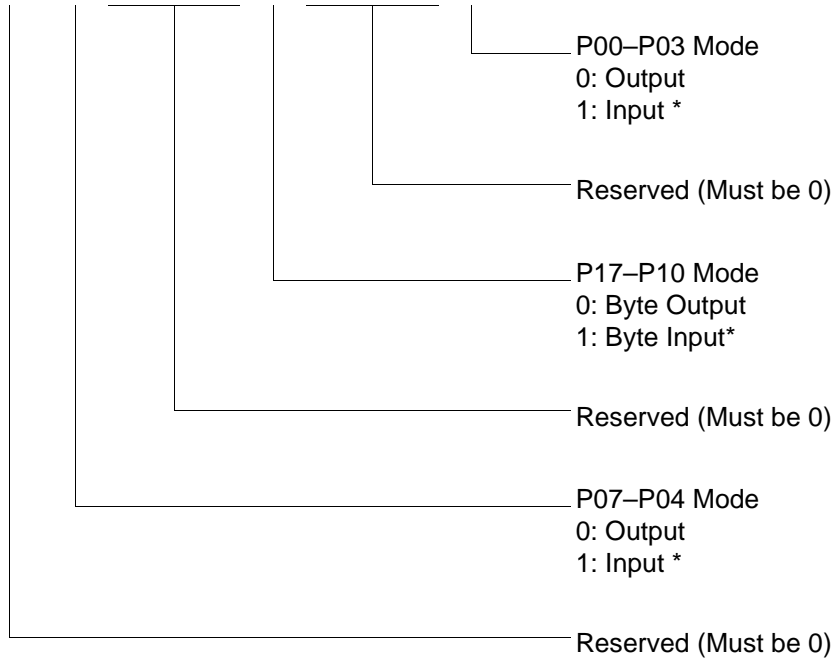


* CLR1 and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

Figure 38. Resets and WDT

R248 P01M(F8H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



* Default setting after reset; only P00, P01 and P07 are available in 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)

R249 IPR(F9H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

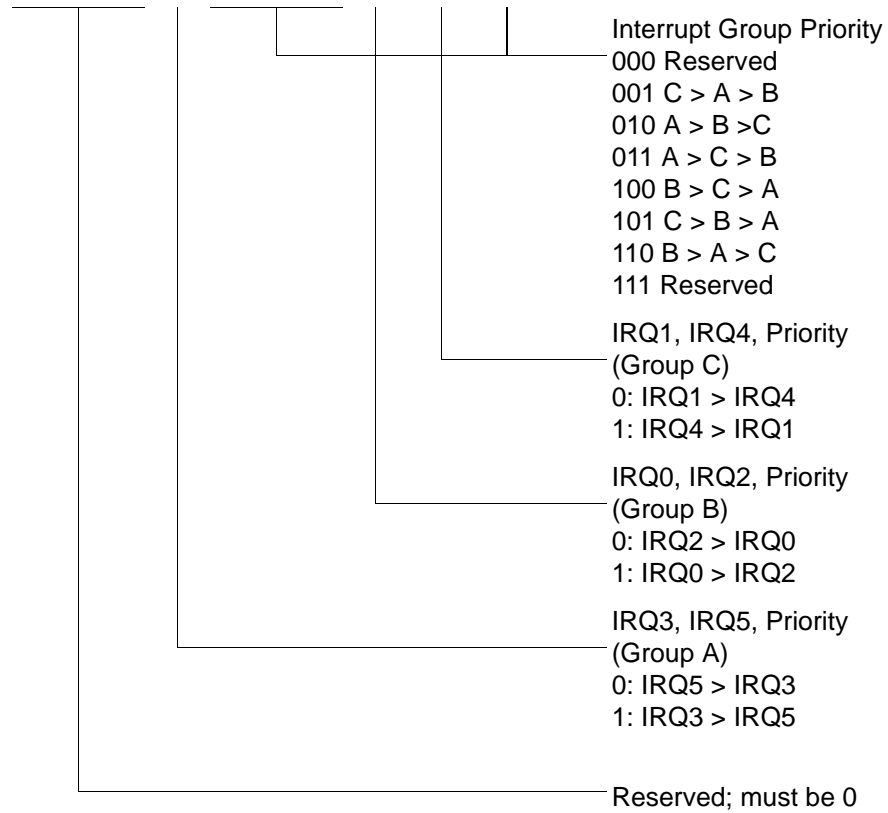


Figure 51. Interrupt Priority Register (F9H: Write Only)

R254 SPH(FEH)

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

General-Purpose Register

Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Stack Pointer Low
Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of Z8 GP™ OTP MCU Family are depicted in Figures 58 through Figure 68.

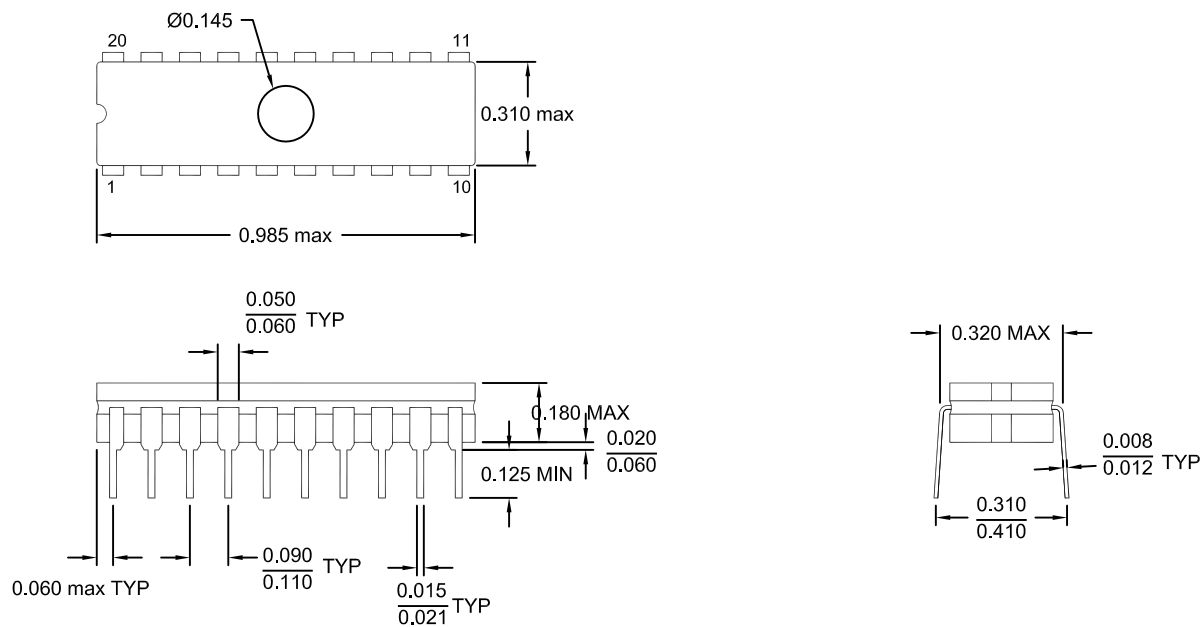


Figure 58. 20-Pin CDIP Package

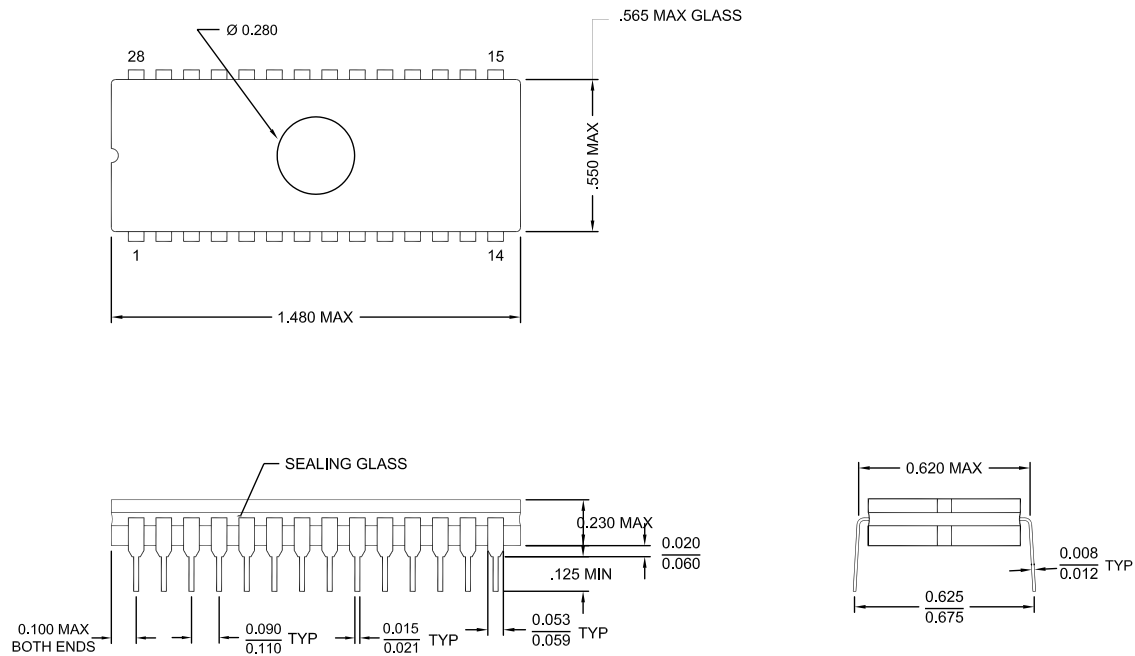
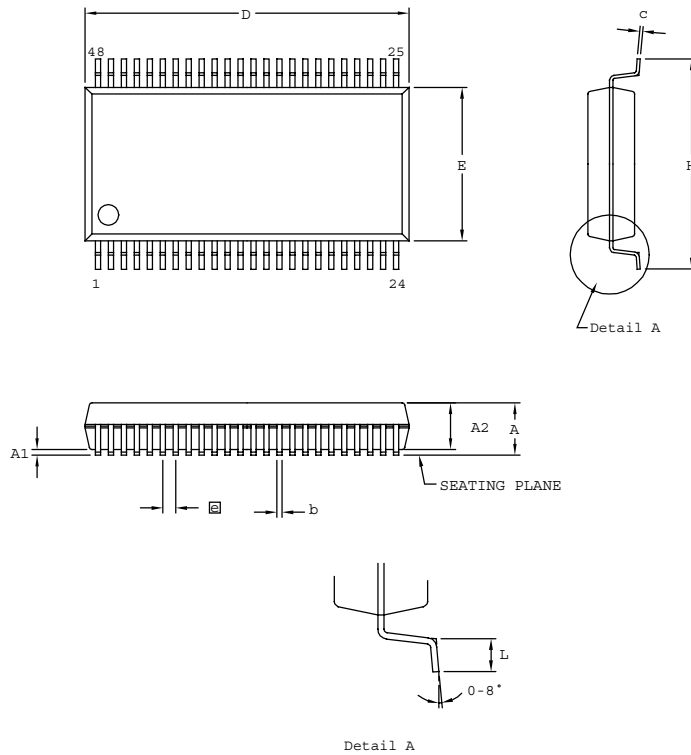


Figure 62. 28-Pin CDIP Package



| SYMBOL | MILLIMETER | | INCH | |
|--------|------------|-------|-----------|--------|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.79 | 0.095 | 0.110 |
| A1 | 0.23 | 0.38 | 0.009 | 0.015 |
| A2 | 2.18 | 2.39 | 0.086 | 0.094 |
| b | 0.20 | 0.34 | 0.008 | 0.0135 |
| c | 0.13 | 0.25 | 0.005 | 0.010 |
| D | 15.75 | 16.00 | 0.620 | 0.630 |
| E | 7.39 | 7.59 | 0.291 | 0.299 |
| ⓐ | 0.635 BSC | | 0.025 BSC | |
| H | 10.16 | 10.41 | 0.400 | 0.410 |
| L | 0.51 | 1.016 | 0.020 | 0.040 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 68. 48-Pin SSOP Package Design

- **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



16KB Standard Temperature: 0° to +70°C

| Part Number | Description | Part Number | Description |
|--------------------|---------------------|--------------------|---------------------|
| ZGP323LSH4816C | 48-pin SSOP 16K OTP | ZGP323LSS2816C | 28-pin SOIC 16K OTP |
| ZGP323LSP4016C | 40-pin PDIP 16K OTP | ZGP323LSH2016C | 20-pin SSOP 16K OTP |
| ZGP323LSH2816C | 28-pin SSOP 16K OTP | ZGP323LSP2016C | 20-pin PDIP 16K OTP |
| ZGP323LSP2816C | 28-pin PDIP 16K OTP | ZGP323LSS2016C | 20-pin SOIC 16K OTP |

16KB Extended Temperature: -40° to +105°C

| Part Number | Description | Part Number | Description |
|--------------------|---------------------|--------------------|---------------------|
| ZGP323LEH4816C | 48-pin SSOP 16K OTP | ZGP323LES2816C | 28-pin SOIC 16K OTP |
| ZGP323LEP4016C | 40-pin PDIP 16K OTP | ZGP323LES2016C | 20-pin SOIC 16K OTP |
| ZGP323LEH2816C | 28-pin SSOP 16K OTP | ZGP323LEH2016C | 20-pin SSOP 16K OTP |
| ZGP323LEP2816C | 28-pin PDIP 16K OTP | ZGP323LEP2016C | 20-pin PDIP 16K OTP |

16KB Automotive Temperature: -40° to +125°C

| Part Number | Description | Part Number | Description |
|--------------------|---------------------|--------------------|---------------------|
| ZGP323LAH4816C | 48-pin SSOP 16K OTP | ZGP323LAS2816C | 28-pin SOIC 16K OTP |
| ZGP323LAP4016C | 40-pin PDIP 16K OTP | ZGP323LAH2016C | 20-pin SSOP 16K OTP |
| ZGP323LAH2816C | 28-pin SSOP 16K OTP | ZGP323LAP2016C | 20-pin PDIP 16K OTP |
| ZGP323LAP2816C | 28-pin PDIP 16K OTP | ZGP323LAS2016C | 20-pin SOIC 16K OTP |

Note: Replace C with G for Lead-Free Packaging



8KB Standard Temperature: 0° to +70°C

| Part Number | Description | Part Number | Description |
|----------------|--------------------|----------------|--------------------|
| ZGP323LSH4808C | 48-pin SSOP 8K OTP | ZGP323LSS2808C | 28-pin SOIC 8K OTP |
| ZGP323LSP4008C | 40-pin PDIP 8K OTP | ZGP323LSH2008C | 20-pin SSOP 8K OTP |
| ZGP323LSH2808C | 28-pin SSOP 8K OTP | ZGP323LSP2008C | 20-pin PDIP 8K OTP |
| ZGP323LSP2808C | 28-pin PDIP 8K OTP | ZGP323LSS2008C | 20-pin SOIC 8K OTP |

8KB Extended Temperature: -40° to +105°C

| Part Number | Description | Part Number | Description |
|----------------|--------------------|----------------|--------------------|
| ZGP323LEH4808C | 48-pin SSOP 8K OTP | ZGP323LES2808C | 28-pin SOIC 8K OTP |
| ZGP323LEP4008C | 40-pin PDIP 8K OTP | ZGP323LEH2008C | 20-pin SSOP 8K OTP |
| ZGP323LEH2808C | 28-pin SSOP 8K OTP | ZGP323LEP2008C | 20-pin PDIP 8K OTP |
| ZGP323LEP2808C | 28-pin PDIP 8K OTP | ZGP323LES2008C | 20-pin SOIC 8K OTP |

8KB Automotive Temperature: -40° to +125°C

| Part Number | Description | Part Number | Description |
|----------------|--------------------|----------------|--------------------|
| ZGP323LAH4808C | 48-pin SSOP 8K OTP | ZGP323LAS2808C | 28-pin SOIC 8K OTP |
| ZGP323LAP4008C | 40-pin PDIP 8K OTP | ZGP323LAH2008C | 20-pin SSOP 8K OTP |
| ZGP323LAH2808C | 28-pin SSOP 8K OTP | ZGP323LAP2008C | 20-pin PDIP 8K OTP |
| ZGP323LAP2808C | 28-pin PDIP 8K OTP | ZGP323LAS2008C | 20-pin SOIC 8K OTP |

Note: Replace C with G for Lead-Free Packaging

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