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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lep2808c

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Table 2. Power Connections

Connection	Circuit	Device	
Power	V _{CC}	V _{DD}	
Ground	GND	V _{SS}	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram



40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC

Table 5. 40- and 48-Pin Configuration (Continued)



AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.









Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP^{TM} asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP^{TM} does not assert the RESET pin when under VBO.



Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®], functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.



Location of 32	768	Not Accessible
first Byte of		On-Chip
executed		ROW
after RESET	12	Reset Start Address
	11	IRQ5
	10	IRQ5
	9	IRQ4
	8	IRQ4
Interrupt Vector	7	IRQ3
(Lower Byte)	6	IRQ3
	5	► IRQ2
Interrupt Vector	4	┍ IRQ2
(Upper Byte)	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0

Figure 14. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The $Z8^{\ensuremath{\mathbb{R}}}$ register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



Z8 [®] Standard Control Registers	F	Rese	et C	onc	litio	n	
Expanded Reg. Bank 0/Group 15**			D4	D3	D2	D1	D0
		1					
			0	0	0	0	0
		0	0	0	0	0	0
Register Pointer	0 0	0	0	0	0	0	0
	00	0	0	0	0	0	0
	00	U	U	U	U	U	U
Working Register Expanded Register	0 0	0	0	0	0	0	0
Group Pointer Bank Pointer F9 IPK		U	U	U	U	U	U
	1 1	0	0	1	1	1	1
* F7 P3M	0 0	0	0	0	0	0	0
* F6 P2M	1 1	1	1	1	1	1	1
F5 Reserved	UU	U	U	U	U	U	U
F4 Reserved	UU	U	U	U	U	U	U
F3 Reserved	UU	U	U	U	U	U	U
Register File (Bank 0)** /	UU	U	U	U	U	U	U
FF F1 Reserved	UU	U	U	U	U	U	U
F0 Reserved	υυ	U	U	U	U	U	U
Expanded Reg. Bank E/Group 0**							
L (F) OF WDTMR		0	0	1	1	0	1
(F) OF Reserved	0 0	0	0	-	-	0	-
* (F) 0D_SMR2	0.0	0	0	0	0	0	0
(F) OC Reserved	00	-	0	-	•	•	0
		4	0	0	0		0
7F	0 0	-	0	0	0	0	0
		-		_	_	-	_
				_		_	
				_		_	
				-		_	
				-		_	
				-		_	
				_	-	-	_
				_	-	-	_
				_	-	-	_
			4	-	4	-	~
Expanded Reg. Bank 0/Group (0)	1 1		ſ	1	1	1	0
(0) 03 P3 0 U Hxpanded\Reg. Bank D/Group 0							_
(0) 02 P2 U (D) 0C LVD		0	0	U	U	0	0
* (0) 01 P1	0 0	0	0	0	0	0	0
(0) 01 1 1 0 (D) 02 100 (D) 02 116	0 0	0	0	0	0	0	0
(0) 00 P0 U * (D) 08 LO16	0 0	0	0	0	0	0	0
U = Unknown	0 0	0	0	0	0	0	0
* Is not reset with a Stop-Mode Recovery	0 0	0	0	0	0	0	0
** All addresses are in hexadecimal	0 0	0	0	0	0	0	0
↑ Is not reset with a Stop-Mode Recovery, except Bit 0	0 0	0	0	0	0	0	0
↑↑ Bit 5 Is not reset with a Stop-Mode Recovery	0 0	0	1	1	1	1	1
↑↑↑ Bits 5.4.3.2 not reset with a Stop-Mode Recovery	0 0	0	0	0	0	0	0
↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery	0 0	0	0	0	0	0	0
1111 Dia 5 4 2 2 4 not react with a Stan Made Decouvery	0 0	0	0	0	0	0	0

Figure 15. Expanded Register File Architecture



Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description	
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect	

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field Bit Position		Description	
T16_Data_HI	[7:0]	R/W	Data



T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



Figure 25. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in "Interrupts" on page 48.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.





Figure 30. Interrupt Block Diagram





SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

- * * Set after STOP Mode Recovery
- * * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



Table 19. Stop Mode Recovery Source

SMR:432			Operation		
D4	D3	D2	Description of Action		
0	0	0	POR and/or external reset recovery		
0	0	1	Reserved		
0	1	0	P31 transition		
0	1	1	P32 transition		
1	0	0	P33 transition		
1	0	1	P27 transition		
1	1	0	Logical NOR of P20 through P23		
1	1	1	Logical NOR of P20 through P27		

>

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 59 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

Note: It is recommended that this bit be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).



Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8[®] CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 20.



WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

Table 21. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.



CTR1(0D)01H D7 D6 D5 D3 D1 D0 D4 D2 Transmit Mode* R/W 0 T16_OUT is 0 initially* 1 T16_OUT is 1 initially **Demodulation Mode** R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially **Demodulation Mode** R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 **Demodulation Mode** 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 1 Reserved Transmit Mode/T8/T16 Logic 0 0 AND** 0 1 OR 1 0 NOR 1 1 NAND **Demodulation Mode** 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 1 Reserved Transmit Mode 0 P36 as Port Output * 1 P36 as T8/T16_OUT **Demodulation Mode** 0 P31 as Demodulator Input 1 P20 as Demodulator Input Transmit/Demodulation Mode 0 Transmit Mode * * Default setting after reset **Default setting after reset. Not reset with Stop Mode 1 Demodulation Mode recovery





PCON(0F)00H



* Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)



SMR(0F)0BH



- * Default setting after Reset
- * * Set after STOP Mode Recovery
- * * * At the XOR gate input
- **** Default setting after Reset. Must be 1 if using a crystal or resonator clock source.
- * * * * * Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)





Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

* * At the XOR gate input





WDTMR(0F)0FH



* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

R246 P2M(F6H)



* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)







Figure 68. 48-Pin SSOP Package Design

Note: Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

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