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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lep2816c

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Development Features

Table 1 lists the features of $ZiLOG^{(R)}$'s Z8 GP^{TM} OTP MCU Family family members.

Table 1. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323L OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V-3.6V

- Low power consumption–6mW (typical)
- T = Temperature
 - S = Standard 0° to +70°C
 - $E = Extended 40^{\circ} to + 105^{\circ}C$
 - A = Automotive -40° to $+125^{\circ}$ C
- Three standby modes:
 - STOP-2µA (typical)
 - HALT-0.8mA (typical)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors



- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR
- **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K Ω ±50% at V_{CC}=3 V and 450 K Ω ±50% at $V_{CC}=2$ V.

General Description

The Z8 GPTM OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG[®]'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z8 GPTM OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to registermapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8[®] offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of userselectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: All signals with an overline, "", are active Low. For example, B/\overline{W} , in which WORD is active Low, and \overline{B}/W , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.



AC Characteristics

Figure 8 and Table 10 describe the Alternating Current (AC) characteristics.





		T _A =0°C to +70°C 8.0MHz						
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes	Register (D1, D0)
1	ТрС	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width	2.0–3.6	12		ns	3	
		Spec		10TpC			4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5ТрС		4	
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms		

Table 10. AC Characteristics

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0. 2. Interrupt request through Port 3 (P33–P31).

3. SMR – D5 = 1.

4. SMR - D5 = 0.



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTRL0
LD	1, #xx	;	load CTRL1
LD	R1, 2	;	$CTRL2 \rightarrow CTRL1$
LD	RP. #0Dh	;	Select ERF D
for access to bank D	,	,	
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 \rightarrow register 71h			
LD	R1, 2		
; CTRL2 \rightarrow register 71h			

Register File

>

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.



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In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 45.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03H

Table 15 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Table 15. CTR3 (D)03H: 18/116 Control Regist
--

Field	Bit Position		Value	Description
T ₁₆ Enable	7	R	0*	Counter Disabled
-		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T ₈ Enable	-6	R	0*	Counter Disabled
-		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	5	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

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Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description	
Reserved	43210	R	1	Always reads 11111	
		W	х	No Effect	

Note: *Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5– D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).



Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.



into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).



Figure 23. Demodulation Mode Count Capture Flowchart



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

Z8 GPTM OTP MCU Family Product Specification



Figure 35. Stop Mode Recovery Source



Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH

D7	D6	D5	D4	D3	D2	D1	D0]
								Reserved (Must be 0) Reserved (Must be 0) Stop-Mode Recovery Source 2 000 POR Only * 001 NAND P20, P21, P22, P23 010 NAND P20, P21, P22, P23, P24, P25, P26, P27 011 NOR P31, P32, P33 100 NAND P31, P32, P33 101 NOR P31, P32, P33, P00, P07 110 NAND P31, P32, P33, P00, P07
								Reserved (Must be 0) Recovery Level * * 0 Low * 1 High
								Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

* * At the XOR gate input

Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.



Note: Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.



Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H



* Default setting after reset

**Default setting after reset. Not reset with Stop Mode recovery.

Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)





CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved No effect when written Always reads 11111
								Sync Mode 0* Disable Sync Mode** 1 Enable Sync Mode
								T ₈ Enable R 0* T ₈ Disabled R 1 T ₈ Enabled W0 Stop T ₈ W1 Enable T ₈
								T ₁₆ Enable R 0* T ₁₆ Disabled R 1 T ₁₆ Enabled W 0 Stop T ₁₆ W 1 Enable T ₁₆

* Default setting after reset. ** Default setting after reset. Not reset with Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.



LVD(0D)0CH



* Default

Figure 43. Voltage Detection Register

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



WDTMR(0F)0FH



* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

R246 P2M(F6H)



* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)



ZILOG

R249 IPR(F9H)



Figure 51. Interrupt Priority Register (F9H: Write Only)







Figure 66. 40-Pin CDIP Package



MILLIMETER INCH SYMBOL MIN MAX MIN MAX .040 A1 0.51 .020 A2 3.94 .125 .155 3.18 В 0.38 0.53 .015 .021 B1 .040 .060 1.02 1.52 С 0.38 .009 .015 0.23 D 2.050 2.070 52.07 52.58 Ε 15.24 15.75 .600 .620 .100 TYP E1 13.59 .59 14.22 2.54 TYP .535 e .660 eA 15.49 16.76 .610 3.81 .120 .150 L 3.05 Q1 1.91 .075 1.40 .055 S .060 1.52 2.29 .090

Figure 67. 40-Pin PDIP Package Diagram

CONTROLLING DIMENSIONS : INCH

Z i L 0 G 92

4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4804C	48-pin SSOP 4K OTP	ZGP323LSS2804C	28-pin SOIC 4K OTP
ZGP323LSP4004C	40-pin PDIP 4K OTP	ZGP323LSH2004C	20-pin SSOP 4K OTP
ZGP323LSH2804C	28-pin SSOP 4K OTP	ZGP323LSP2004C	20-pin PDIP 4K OTP
ZGP323LSP2804C	28-pin PDIP 4K OTP	ZGP323LSS2004C	20-pin SOIC 4K OTP

4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4804C	48-pin SSOP 4K OTP	ZGP323LES2804C	28-pin SOIC 4K OTP
ZGP323LEP4004C	40-pin PDIP 4K OTP	ZGP323LEH2004C	20-pin SSOP 4K OTP
ZGP323LEH2804C	28-pin SSOP 4K OTP	ZGP323LEP2004C	20-pin PDIP 4K OTP
ZGP323LEP2804C	28-pin PDIP 4K OTP	ZGP323LES2004C	20-pin SOIC 4K OTP

4KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4804C	48-pin SSOP 4K OTP	ZGP323LAS2804C	28-pin SOIC 4K OTP
ZGP323LAP4004C	40-pin PDIP 4K OTP	ZGP323LAH2004C	20-pin SSOP 4K OTP
ZGP323LAH2804C	28-pin SSOP 4K OTP	ZGP323LAP2004C	20-pin PDIP 4K OTP
ZGP323LAP2804C	28-pin PDIP 4K OTP	ZGP323LAS2004C	20-pin SOIC 4K OTP

Note: Replace C with G for Lead-Free Packaging

Additional Components

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer	ZGP32300100ZPR	Programming System

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For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

- 323 = Family Designation
- L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

- E = -40 to +105 degrees C (Extended)
- A = -40 to +125 degrees C (Automotive)
- P = Package Type:
 - K = Windowed Cerdip
 - P = PDIP
 - H = SSOP
 - S = SOIC
- ## = Number of Pins
- CC = Memory Size
- M = Packaging Options
 - C = Non Lead-Free
 - G = Lead-Free
 - E = CDIP