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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lep4004g



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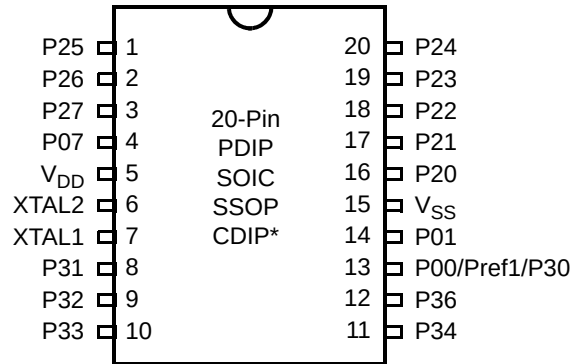


Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC

Capacitance

Table 7 lists the capacitances.

Table 7. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{MHz}$, unmeasured pins returned to GND	

DC Characteristics

Table 8. DC Characteristics

Symbol	Parameter	V_{CC}	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ	Max			
V_{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-3.6	0.8		$V_{CC}+0.3$	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
V_{IL}	Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
V_{OH1}	Output High Voltage	2.0-3.6	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 1.0\text{mA}$ $I_{OL} = 4.0\text{mA}$	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	$I_{OL} = 10\text{mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-3.6	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC} Pull-ups disabled	
I_{OL}	Output Leakage	2.0-3.6	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC}	
I_{CC}	Supply Current	2.0			10	mA	at 8.0 MHz	1, 2
		3.6			15	mA	at 8.0 MHz	1, 2

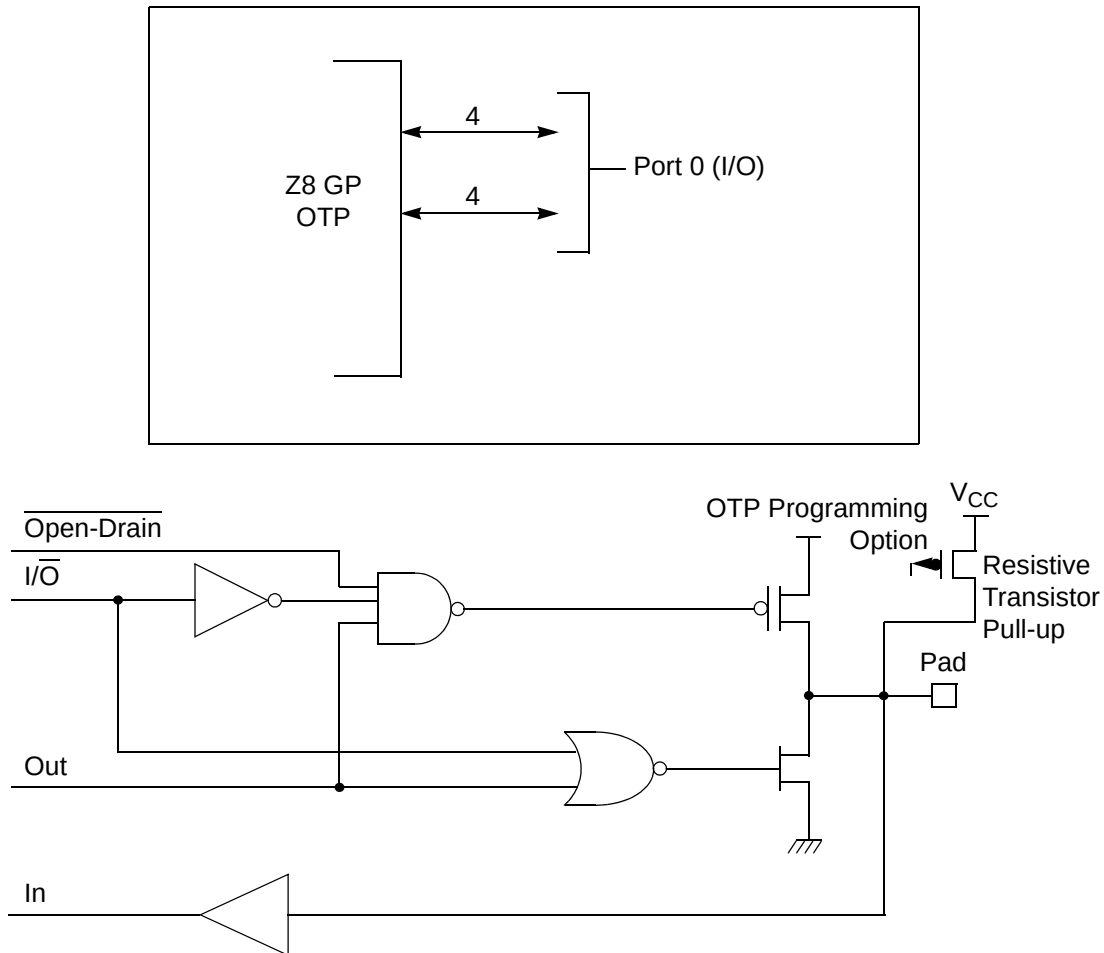


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to be input following an SMR.

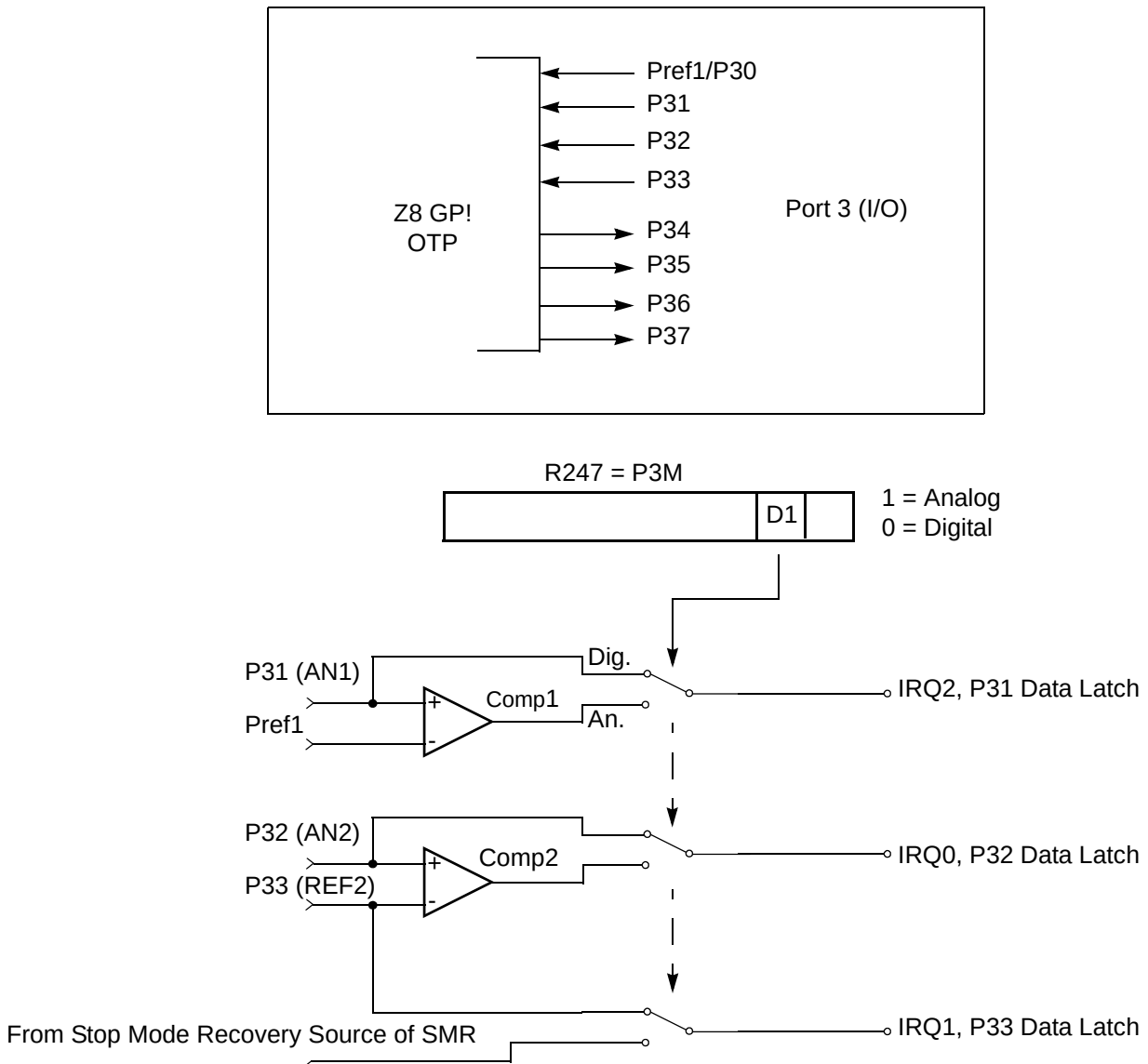


Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—

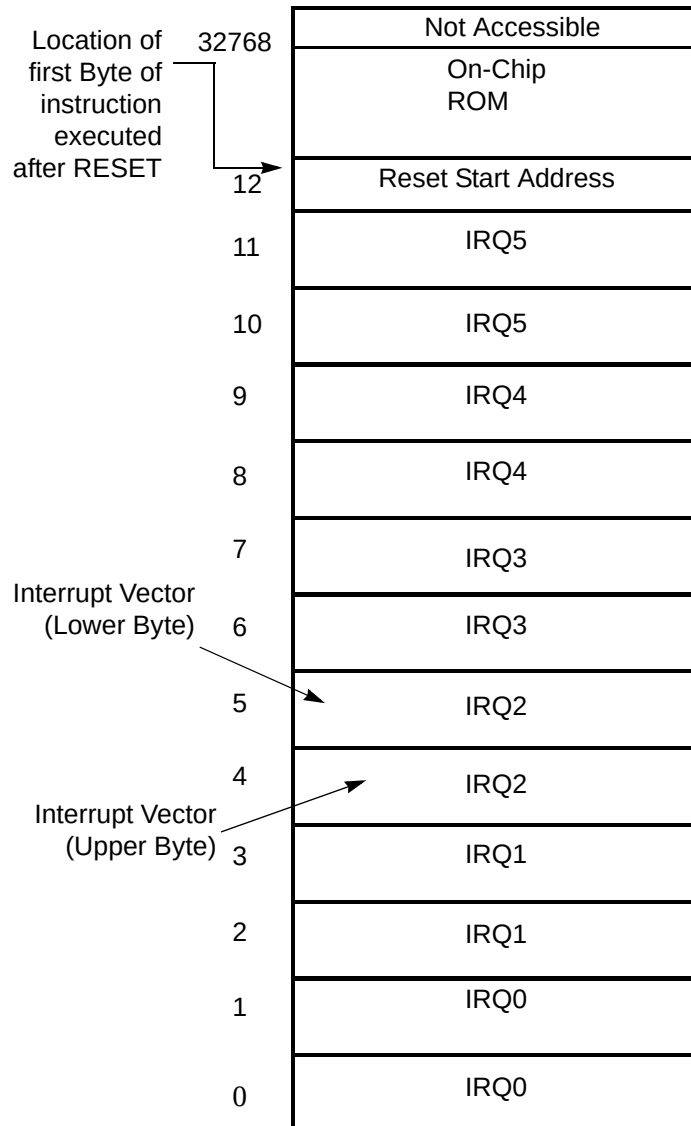


Figure 14. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8® register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          R0, #xx          ; load CTRL0
LD          1, #xx          ; load CTRL1
LD          R1, 2            ; CTRL2→CTRL1

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          RP, #7Dh          ; Select
expanded register bank D and working ; register
group 7 of bank 0 for access.
LD          71h, 2
; CTRL2→register 71h
LD          R1, 2
; CTRL2→register 71h

```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

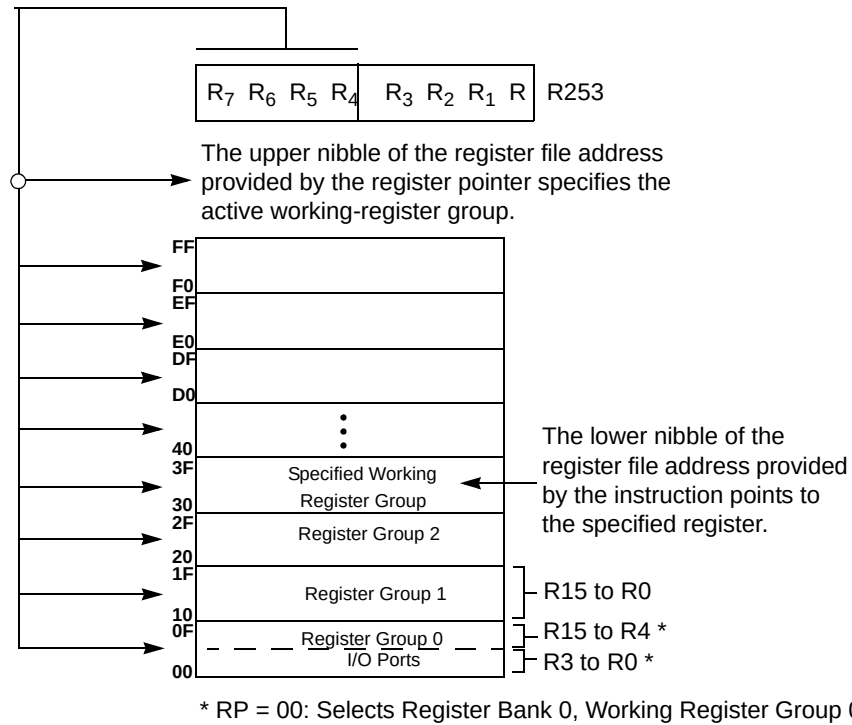


Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



Caution:

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE_H. Transition from 0 to FFFF_H is not a timeout condition.

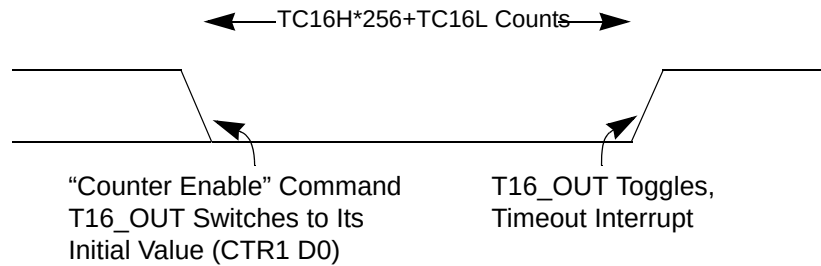


Figure 26. T16_OUT in Single-Pass Mode

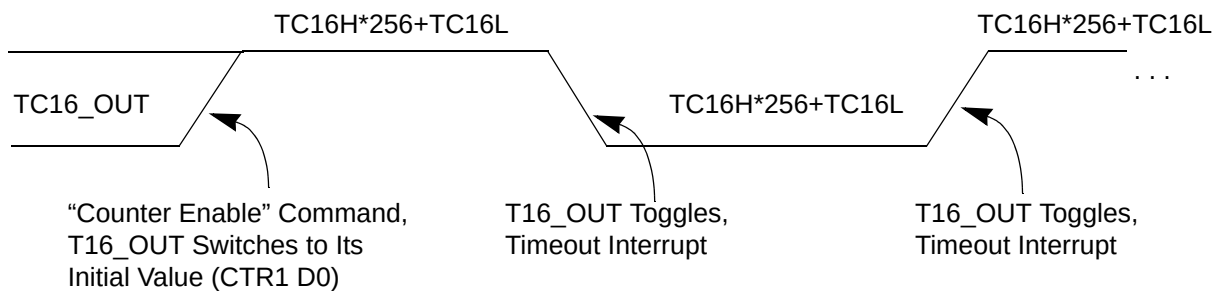


Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FF_H. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF_H and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

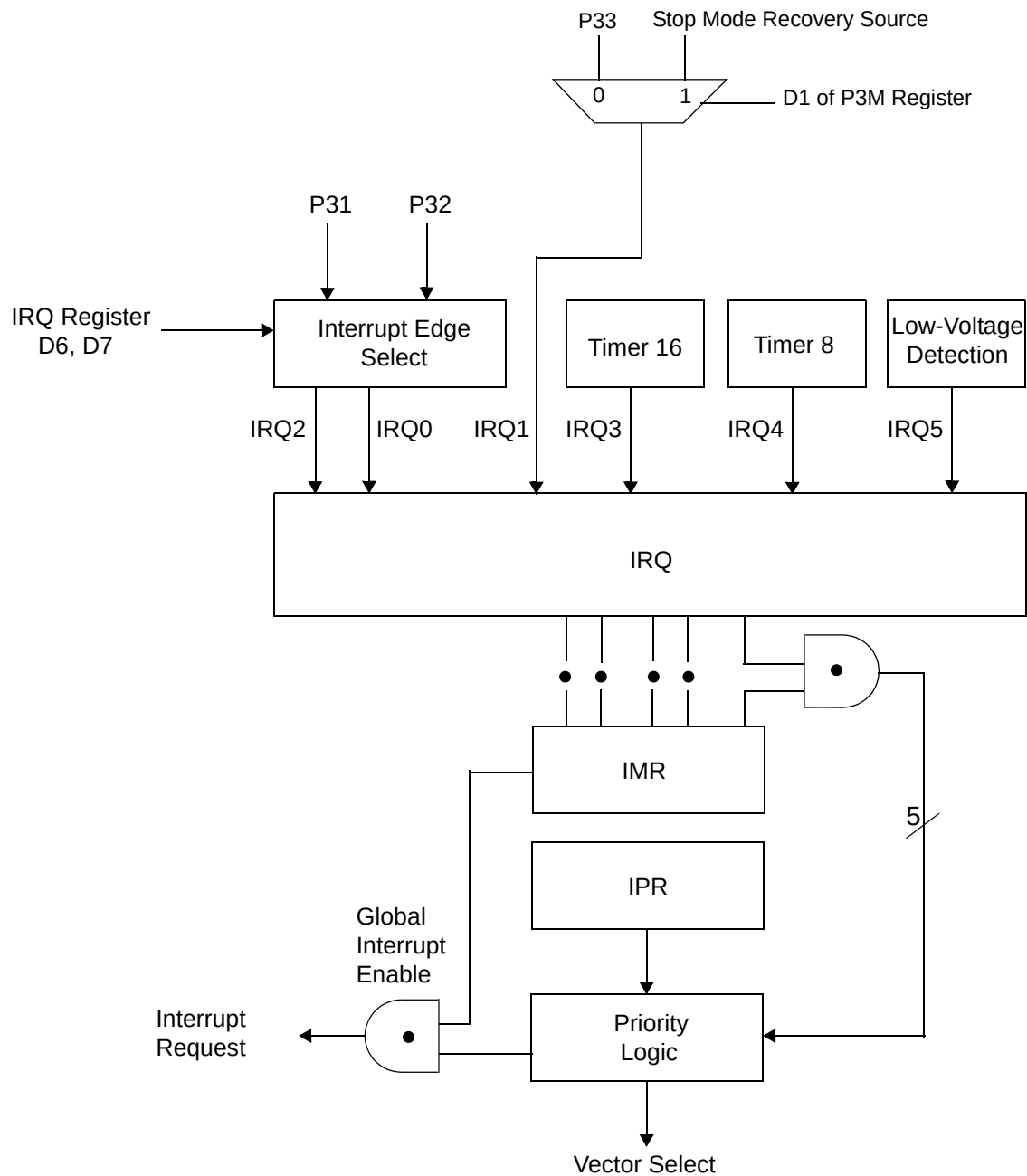


Figure 30. Interrupt Block Diagram

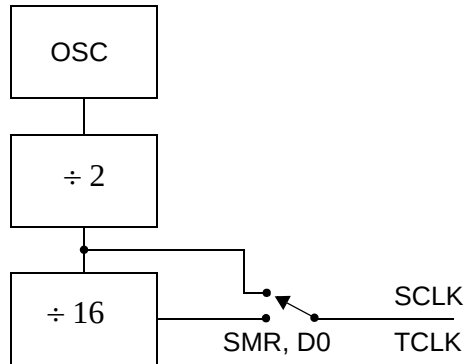


Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 19).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 18 lists and briefly describes the fields for this register.

Table 18. SMR2(F)0DH:Stop Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-----		0	Reserved (Must be 0)
Recovery Level	-6-----	W	0 [†] 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000 [†] 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND of P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	-----10		00	Reserved (Must be 0)

Notes:

* Port pins configured as outputs are ignored as a SMR recovery source.

[†] Indicates the value upon Power-On Reset

Table 19. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 59 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 T_{pC} .

- **Note:** It is recommended that this bit be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

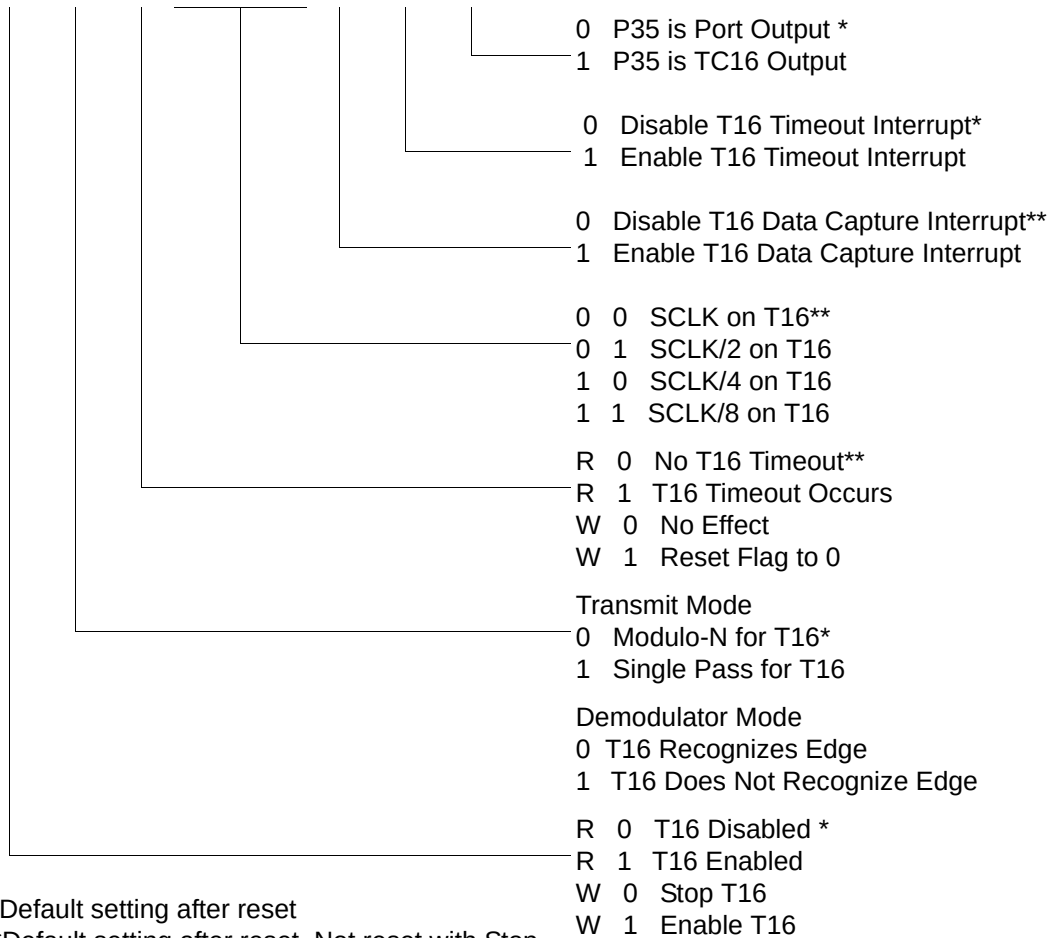
A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



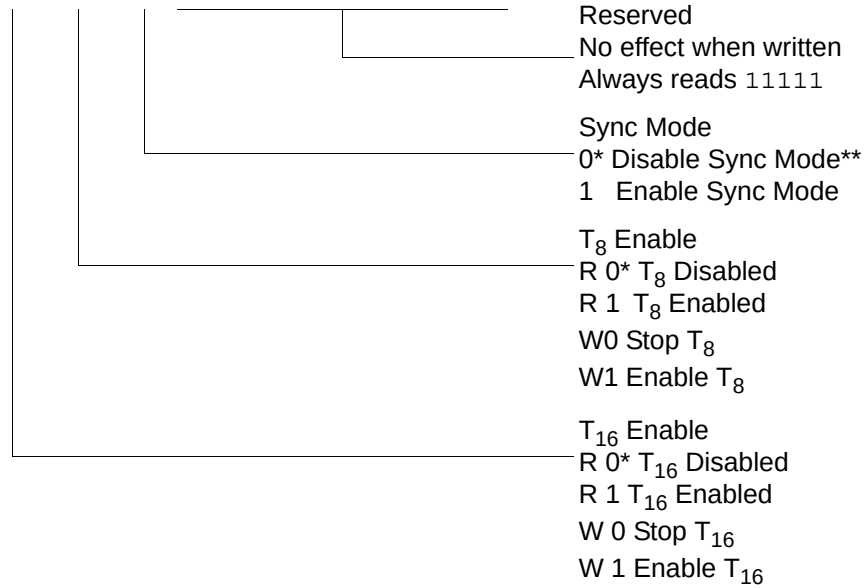
* Default setting after reset

**Default setting after reset. Not reset with Stop Mode recovery.

Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset.

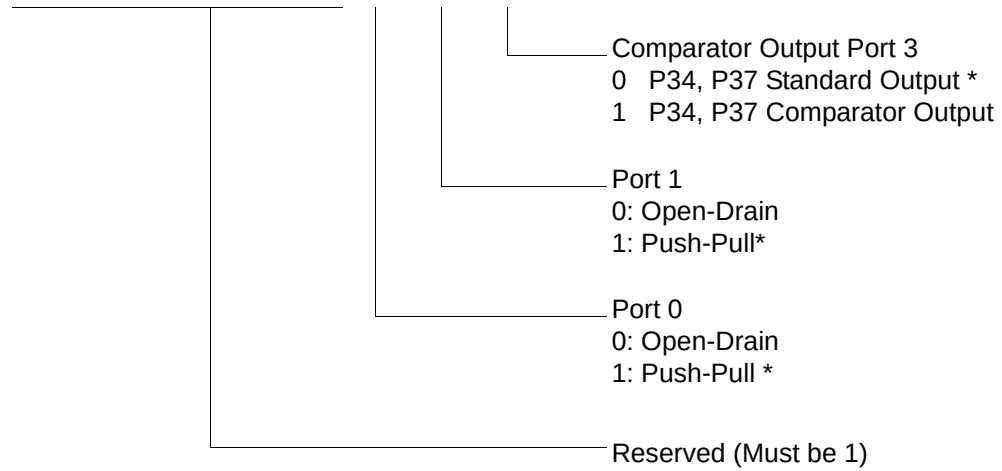
** Default setting after reset. Not reset with Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

► **Note:** If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.

PCON(0F)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

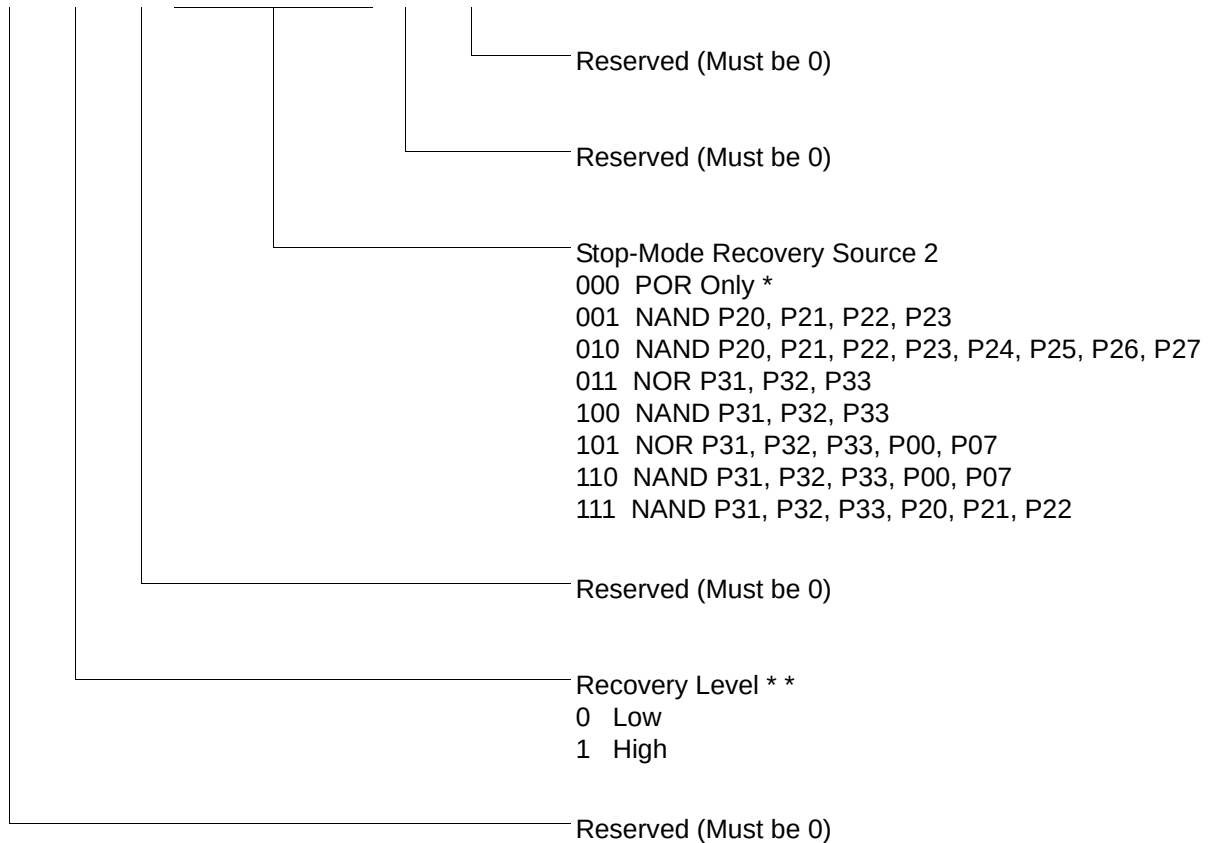


* Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)

SMR2(0F)0DH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

** At the XOR gate input

Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)

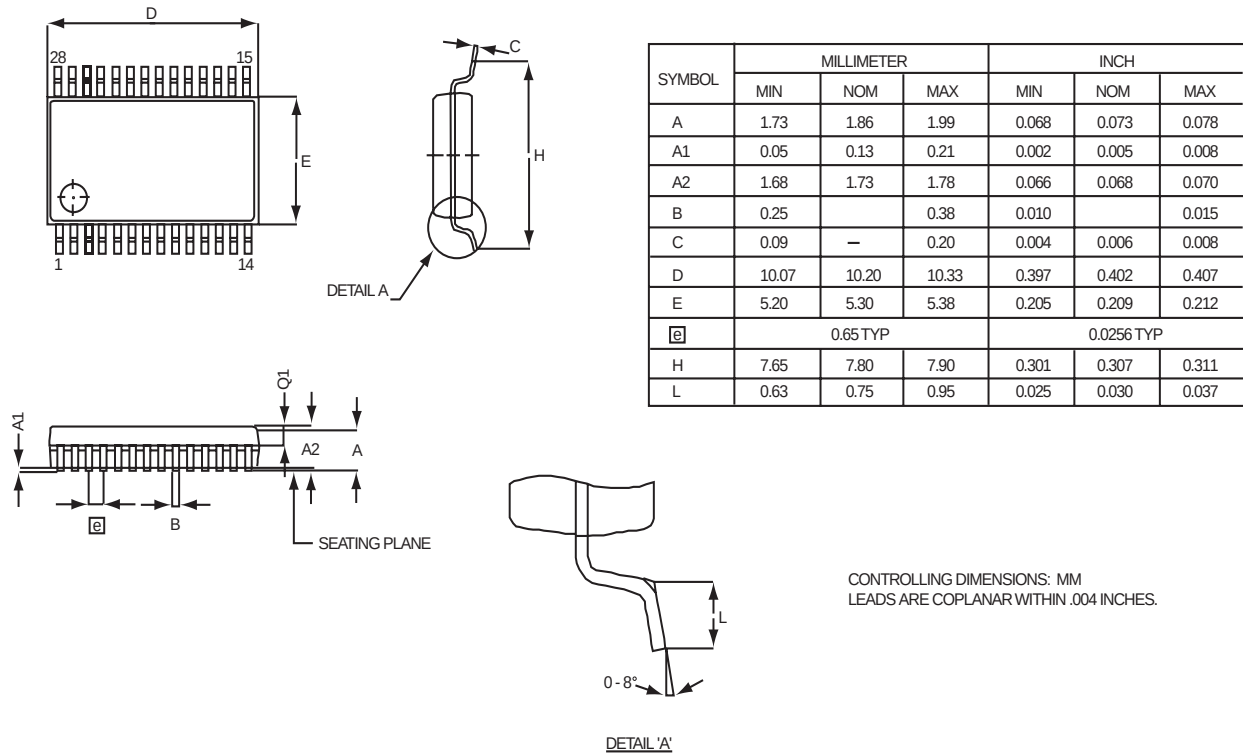


Figure 65. 28-Pin SSOP Package Diagram



16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4816C	48-pin SSOP 16K OTP	ZGP323LSS2816C	28-pin SOIC 16K OTP
ZGP323LSP4016C	40-pin PDIP 16K OTP	ZGP323LSH2016C	20-pin SSOP 16K OTP
ZGP323LSH2816C	28-pin SSOP 16K OTP	ZGP323LSP2016C	20-pin PDIP 16K OTP
ZGP323LSP2816C	28-pin PDIP 16K OTP	ZGP323LSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4816C	48-pin SSOP 16K OTP	ZGP323LES2816C	28-pin SOIC 16K OTP
ZGP323LEP4016C	40-pin PDIP 16K OTP	ZGP323LES2016C	20-pin SOIC 16K OTP
ZGP323LEH2816C	28-pin SSOP 16K OTP	ZGP323LEH2016C	20-pin SSOP 16K OTP
ZGP323LEP2816C	28-pin PDIP 16K OTP	ZGP323LEP2016C	20-pin PDIP 16K OTP

16KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4816C	48-pin SSOP 16K OTP	ZGP323LAS2816C	28-pin SOIC 16K OTP
ZGP323LAP4016C	40-pin PDIP 16K OTP	ZGP323LAH2016C	20-pin SSOP 16K OTP
ZGP323LAH2816C	28-pin SSOP 16K OTP	ZGP323LAP2016C	20-pin PDIP 16K OTP
ZGP323LAP2816C	28-pin PDIP 16K OTP	ZGP323LAS2016C	20-pin SOIC 16K OTP

Note: Replace C with G for Lead-Free Packaging



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