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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323les2032c

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Document Disclaimer

Absolute Maximum Ratings

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+70	C	
Storage temperature	−65	+150	C	
Voltage on any pin with respect to V_{SS}	−0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	−0.3	+3.6	V	
Maximum current on input and/or inactive output pin	−5	+5	µA	
Maximum output current from active output pin	−25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Notes:
This voltage applies to all pins except the following: V_{DD}, P32, P33 and $\overline{RESET}$.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).
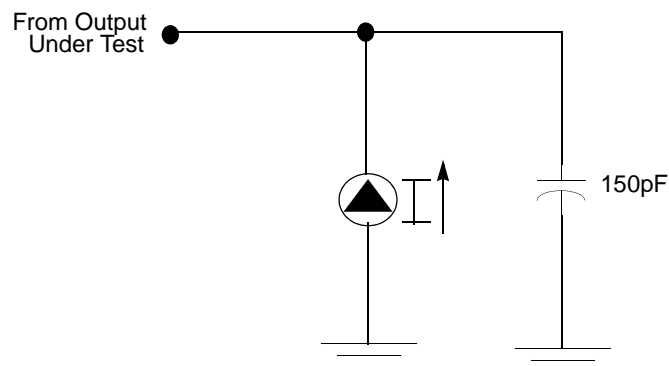
Figure 7.   Test Load Diagram

Table 8. DC Characteristics (Continued)

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units	Conditions	Notes
				T_A= 0°C to +70°C				
I_{CC1}	Standby Current	2.0			3	mA	V_{IN} = 0V, V_{CC} at 8.0MHz	1, 2
	(HALT Mode)	3.6			5		Same as above	1, 2
		2.0			2		Clock Divide-by-16 at 8.0MHz	1, 2
		3.6			4		Same as above	1, 2
I_{CC2}	Standby Current (Stop	2.0			8	μA	V_{IN} = 0 V, V_{CC} WDT is not Running	3
	Mode)	3.6			10	μA	Same as above	3
		2.0			500	μA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6			800	μA	Same as above	3
I_{LV}	Standby Current (Low Voltage)				10	μA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection				2.0	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	Vcc Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes:
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to the V_{DD} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

▶ **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to be input following an SMR.
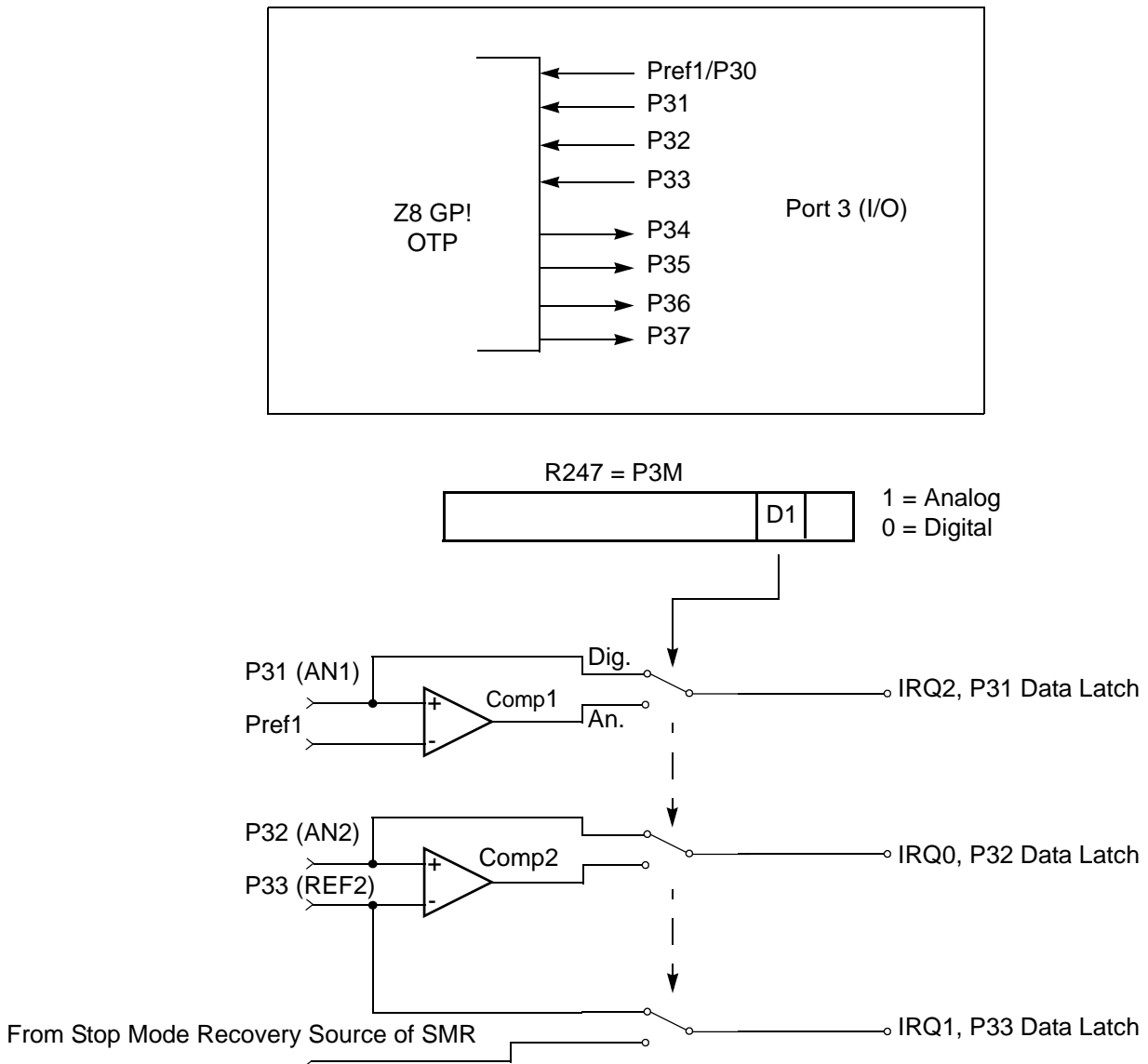
Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see "T8 and T16 Common Functions—

ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

▶ **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).

Z8® Standard Control Registers

Register Pointer

7	6	5	4	3	2	1	0

Working Register Group Pointer

Expanded Register Bank Pointer

Register File (Bank 0)**

Reset Condition

Expanded Reg. Bank 0/Group 15**

		D7	D6	D5	D4	D3	D2	D1	D0
FF	SPL	U	U	U	U	U	U	U	U
FE	SPH	U	U	U	U	U	U	U	U
FD	RP	0	0	0	0	0	0	0	0
FC	FLAGS	U	U	U	U	U	U	U	U
FB	IMR	U	U	U	U	U	U	U	U
FA	IRQ	0	0	0	0	0	0	0	0
F9	IPR	U	U	U	U	U	U	U	U
F8	P01M	1	1	0	0	1	1	1	1
* F7	P3M	0	0	0	0	0	0	0	0
* F6	P2M	1	1	1	1	1	1	1	1
F5	Reserved	U	U	U	U	U	U	U	U
F4	Reserved	U	U	U	U	U	U	U	U
F3	Reserved	U	U	U	U	U	U	U	U
F2	Reserved	U	U	U	U	U	U	U	U
F1	Reserved	U	U	U	U	U	U	U	U
F0	Reserved	U	U	U	U	U	U	U	U

Expanded Reg. Bank F/Group 0**

			D7	D6	D5	D4	D3	D2	D1	D0
*	(F) 0F	WDTMR	U	U	0	0	1	1	0	1
	(F) 0E	Reserved								
*	(F) 0D	SMR2	0	0	0	0	0	0	0	0
	(F) 0C	Reserved								
↑	(F) 0B	SMR	U	0	1	0	0	0	U	0
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
*	(F) 00	PCON	1	1	1	1	1	1	1	0

Expanded Reg. Bank 0/Group (0)

(0) 03 P3	0		U
(0) 02 P2	U		
* (0) 01 P1	U		
(0) 00 P0	U		

Expanded Reg. Bank D/Group 0

			D7	D6	D5	D4	D3	D2	D1	D0
	(D) 0C	LVD	U	U	U	U	U	U	U	0
*	(D) 0B	HI8	0	0	0	0	0	0	0	0
*	(D) 0A	LO8	0	0	0	0	0	0	0	0
*	(D) 09	HI16	0	0	0	0	0	0	0	0
*	(D) 08	LO16	0	0	0	0	0	0	0	0
*	(D) 07	TC16H	0	0	0	0	0	0	0	0
*	(D) 06	TC16L	0	0	0	0	0	0	0	0
*	(D) 05	TC8H	0	0	0	0	0	0	0	0
*	(D) 04	TC8L	0	0	0	0	0	0	0	0
↑↑	(D) 03	CTR3	0	0	0	1	1	1	1	1
↑↑↑	(D) 02	CTR2	0	0	0	0	0	0	0	0
↑↑↑↑	(D) 01	CTR1	0	0	0	0	0	0	0	0
↑↑↑↑↑	(D) 00	CTR0	0	0	0	0	0	0	0	0

U = Unknown

* Is not reset with a Stop-Mode Recovery

** All addresses are in hexadecimal

↑ Is not reset with a Stop-Mode Recovery, except Bit 0

↑↑ Bit 5 Is not reset with a Stop-Mode Recovery

↑↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery

↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery

↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery

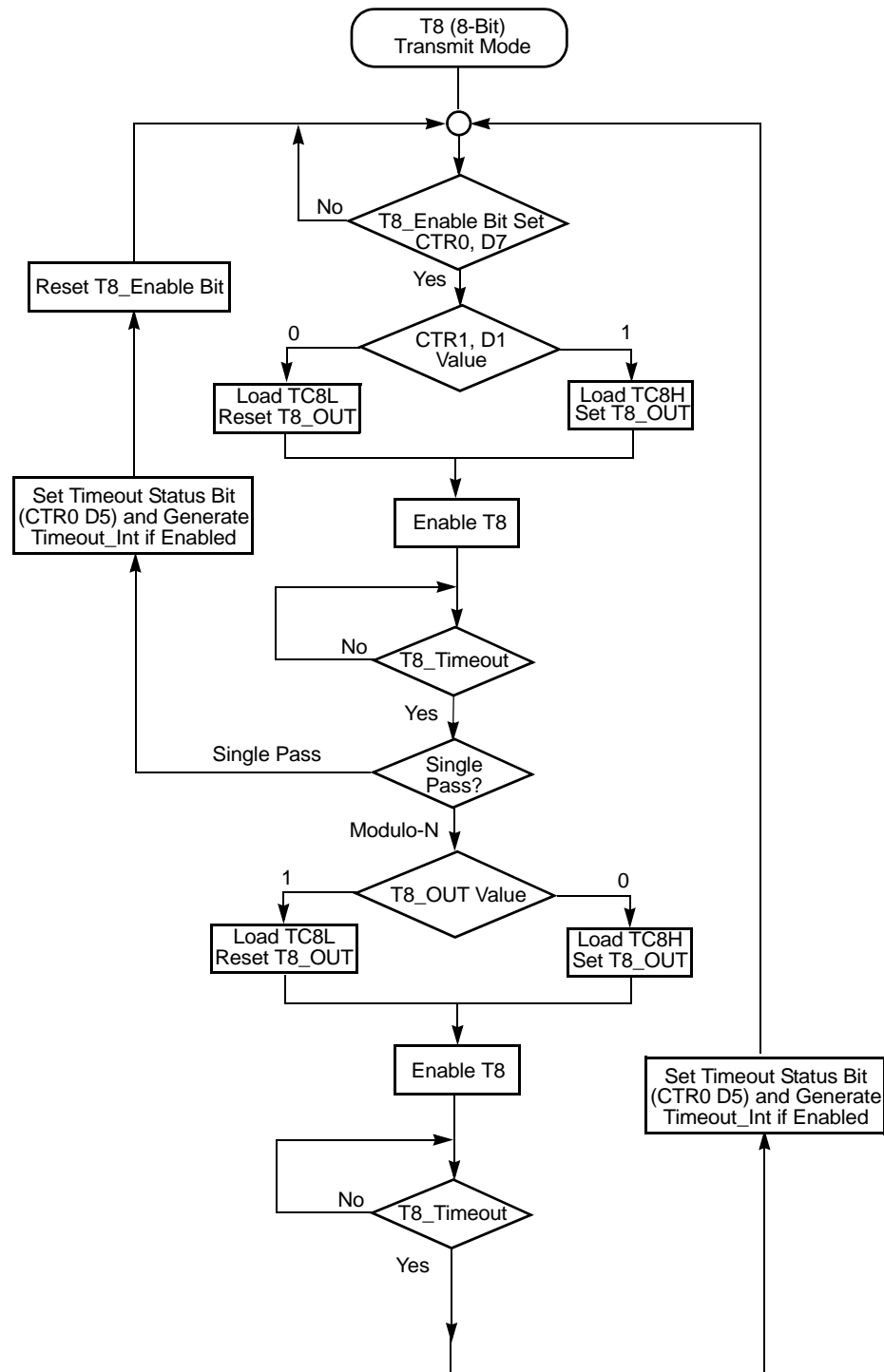**Figure 15. Expanded Register File Architecture**

Figure 19. Transmit Mode Flowchart

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).
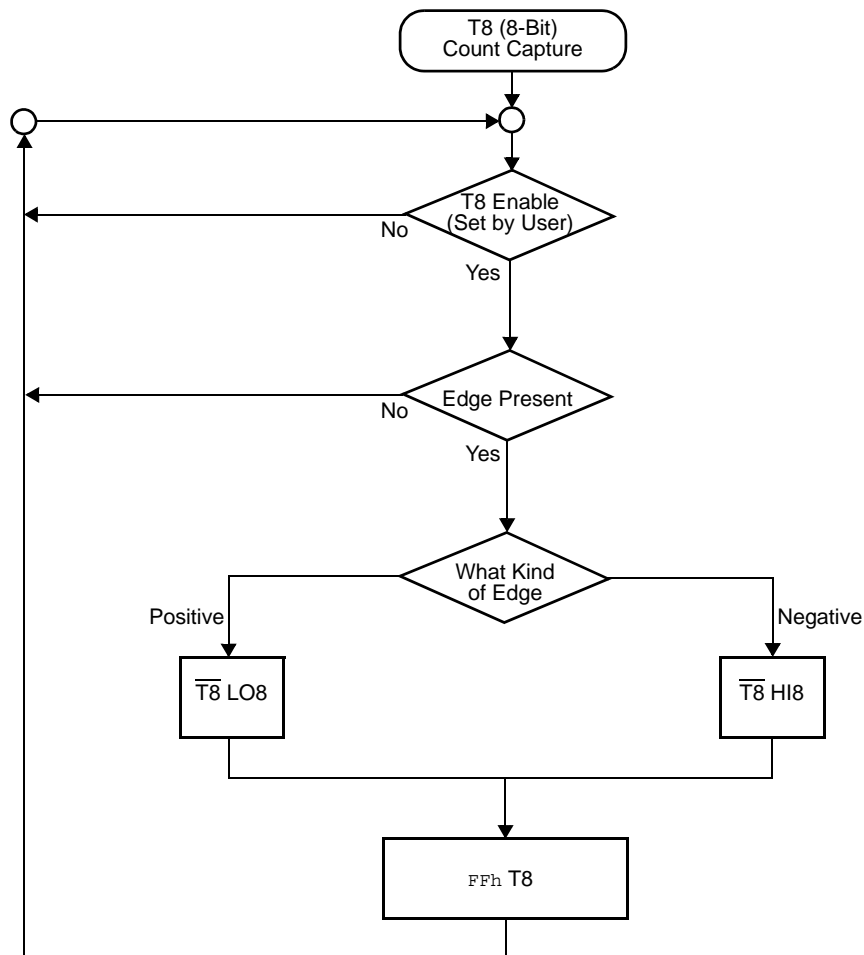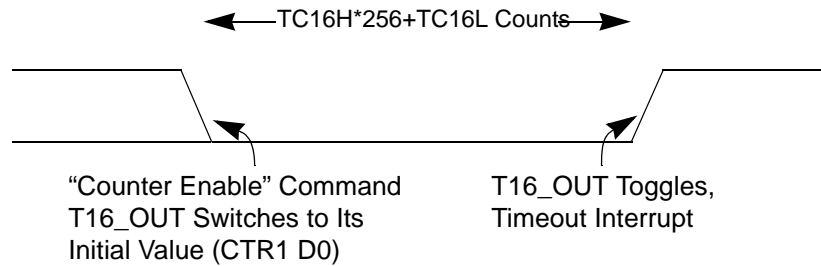

Figure 23. Demodulation Mode Count Capture Flowchart

⚠️ **Caution:** Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFEH. Transition from 0 to FFFFH is not a timeout condition.

Figure 26. T16_OUT in Single-Pass Mode
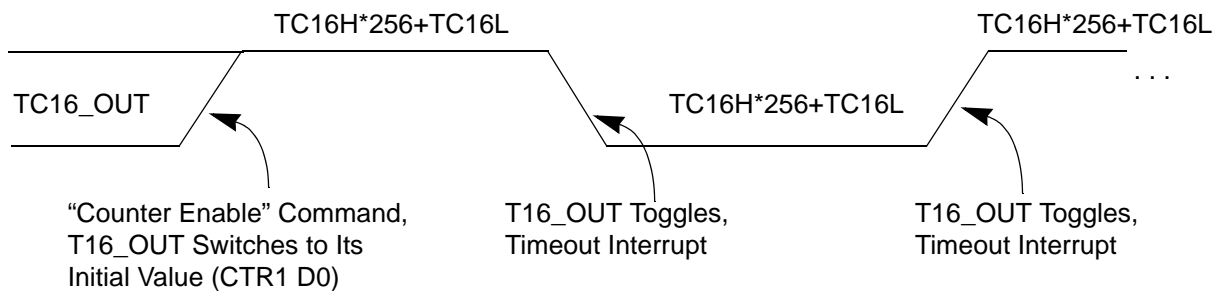
Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

▶ **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.
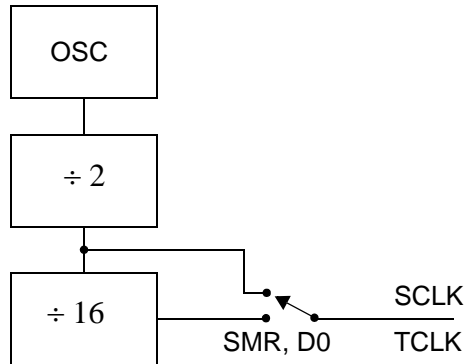
Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 19).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 18 lists and briefly describes the fields for this register.

Table 18. SMR2(F)0DH:Stop Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0[†]	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000[†]	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Port pins configured as outputs are ignored as a SMR recovery source.
[†] Indicates the value upon Power-On Reset

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

Table 21. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

0= P31, P32 Digital Mode*
1= P31, P32 Analog Mode

Reserved (Must be 0)
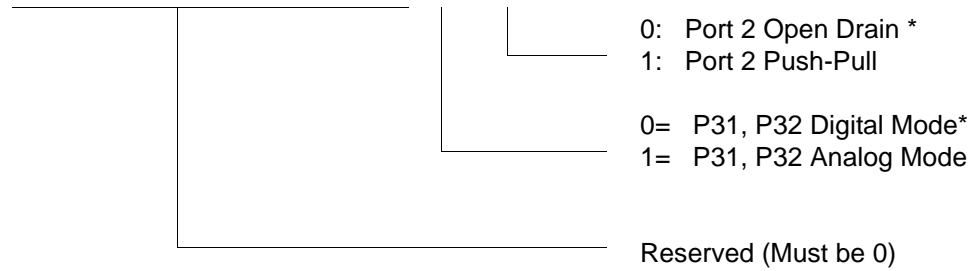
 * Default setting after reset. Not reset with Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

R250 IRQ(FAH)

D7	D6	D5	D4	D3	D2	D1	D0

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = T16
IRQ4 = T8
IRQ5 = LVD

Inter Edge
P31↓   P32↓ = 00
P31↓   P32↑ = 01
P31↑   P32↓ = 10
P31↑↓   P32↑↓ = 11
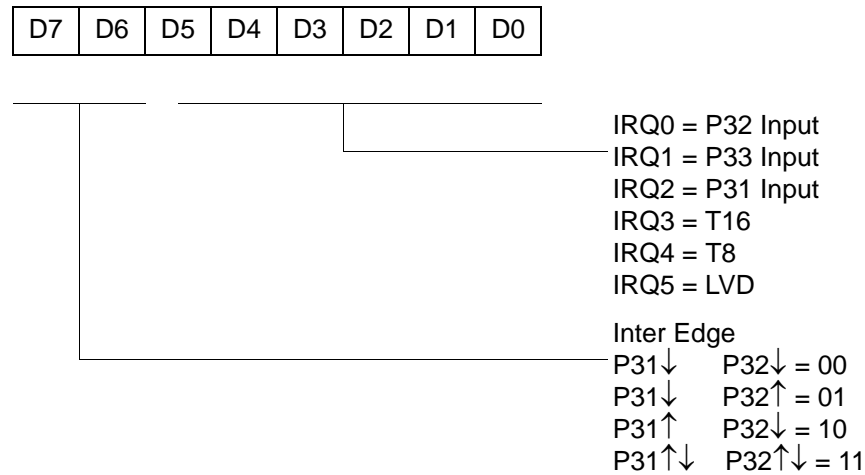
Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)

D7	D6	D5	D4	D3	D2	D1	D0

1 Enables IRQ5–IRQ0
   (D0 = IRQ0)

Reserved (Must be 0)

0   Master Interrupt Disable *
1   Master Interrupt Enable * *
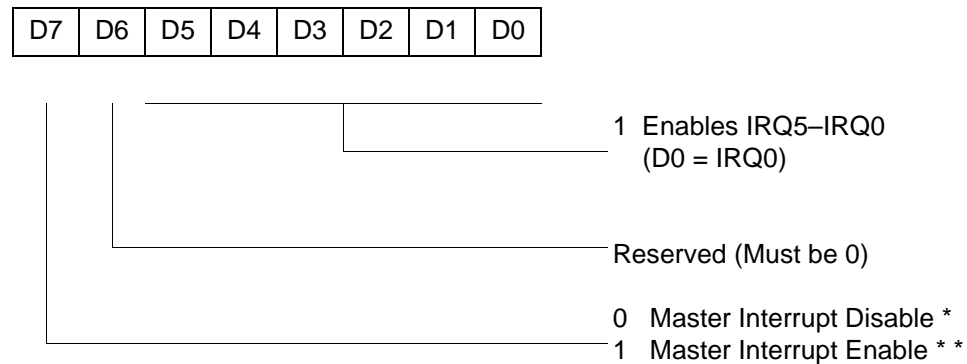
* Default setting after reset
* * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
℮	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram

Ordering Information

32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4832C	48-pin SSOP 32K OTP	ZGP323LSS2832C	28-pin SOIC 32K OTP
ZGP323LSP4032C	40-pin PDIP 32K OTP	ZGP323LSH2032C	20-pin SSOP 32K OTP
ZGP323LSH2832C	28-pin SSOP 32K OTP	ZGP323LSP2032C	20-pin PDIP 32K OTP
ZGP323LSP2832C	28-pin PDIP 32K OTP	ZGP323LSS2032C	20-pin SOIC 32K OTP
ZGP323LSK2032E	20-pin CDIP 32K OTP	ZGP323LSK4032E	40-pin CDIP 32K OTP
		ZGP323LSK2832E	28-pin CDIP 32K OTP

32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4832C	48-pin SSOP 32K OTP	ZGP323LES2832C	28-pin SOIC 32K OTP
ZGP323LEP4032C	40-pin PDIP 32K OTP	ZGP323LEH2032C	20-pin SSOP 32K OTP
ZGP323LEH2832C	28-pin SSOP 32K OTP	ZGP323LEP2032C	20-pin PDIP 32K OTP
ZGP323LEP2832C	28-pin PDIP 32K OTP	ZGP323LES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4832C	48-pin SSOP 32K OTP	ZGP323LAS2832C	28-pin SOIC 32K OTP
ZGP323LAP4032C	40-pin PDIP 32K OTP	ZGP323LAH2032C	20-pin SSOP 32K OTP
ZGP323LAH2832C	28-pin SSOP 32K OTP	ZGP323LAP2032C	20-pin PDIP 32K OTP
ZGP323LAP2832C	28-pin PDIP 32K OTP	ZGP323LAS2032C	20-pin SOIC 32K OTP

Note: Replace C with G for Lead-Free Packaging

4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4804C	48-pin SSOP 4K OTP	ZGP323LSS2804C	28-pin SOIC 4K OTP
ZGP323LSP4004C	40-pin PDIP 4K OTP	ZGP323LSH2004C	20-pin SSOP 4K OTP
ZGP323LSH2804C	28-pin SSOP 4K OTP	ZGP323LSP2004C	20-pin PDIP 4K OTP
ZGP323LSP2804C	28-pin PDIP 4K OTP	ZGP323LSS2004C	20-pin SOIC 4K OTP

4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4804C	48-pin SSOP 4K OTP	ZGP323LES2804C	28-pin SOIC 4K OTP
ZGP323LEP4004C	40-pin PDIP 4K OTP	ZGP323LEH2004C	20-pin SSOP 4K OTP
ZGP323LEH2804C	28-pin SSOP 4K OTP	ZGP323LEP2004C	20-pin PDIP 4K OTP
ZGP323LEP2804C	28-pin PDIP 4K OTP	ZGP323LES2004C	20-pin SOIC 4K OTP

4KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4804C	48-pin SSOP 4K OTP	ZGP323LAS2804C	28-pin SOIC 4K OTP
ZGP323LAP4004C	40-pin PDIP 4K OTP	ZGP323LAH2004C	20-pin SSOP 4K OTP
ZGP323LAH2804C	28-pin SSOP 4K OTP	ZGP323LAP2004C	20-pin PDIP 4K OTP
ZGP323LAP2804C	28-pin PDIP 4K OTP	ZGP323LAS2004C	20-pin SOIC 4K OTP

Note: Replace C with G for Lead-Free Packaging

Additional Components

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer	ZGP32300100ZPR	Programming System