E·XFL

Zilog - ZGP323LES2032C00TR Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323les2032c00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters 532 Race Street

San Jose, CA 95126-3432 Telephone: 408.558.8500 Fax: 408.558.8300 www.zilog.com

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

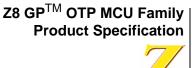
Document Disclaimer

©2004 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZILOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose. Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.



List of Tables

Table 1.	Features
Table 2.	Power Connections
Table 3.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification
Table 4.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification
Table 5.	40- and 48-Pin Configuration 8
Table 6.	Absolute Maximum Ratings 10
Table 7.	Capacitance
Table 8.	DC Characteristics 11
Table 9.	EPROM/OTP Characteristics 13
Table 10.	AC Characteristics 15
Table 11.	Port 3 Pin Function Summary 21
Table 12.	CTR0(D)00H Counter/Timer8 Control Register 31
Table 13.	CTR1(0D)01H T8 and T16 Common Functions
Table 14.	CTR2(D)02H: Counter/Timer16 Control Register
Table 15.	CTR3 (D)03H: T8/T16 Control Register 37
Table 16.	Interrupt Types, Sources, and Vectors
Table 17.	IRQ Register 50
Table 18.	SMR2(F)0DH:Stop Mode Recovery Register 2* 56
Table 19.	Stop Mode Recovery Source 58
Table 20.	Watch-Dog Timer Time Select 61
Table 21.	EPROM Selectable Options 62





		\bigcirc	
NC			40 ⊐ NC
P25			39 □ P24
P26			38 🗖 P23
P27	□ 4		37 🗖 P22
P04	□ 5		36 🗖 P21
P05	□ 6	40-Pin	35 🗖 P20
P06	– 7	PDIP	34 🗖 P03
P14	□ 8	CDIP*	33 🗖 P13
P15	□ 9	ODI	32 🗖 P12
P07	1 0		31 🗖 VSS
VDD	– 11		30 🗖 P02
P16	1 2		39 🗖 P11
P17	1 3		28 🗖 P10
XTAL2	□ 14		27 🗖 P01
XTAL1	□ 15		26 🗖 P00
P31	1 6		25 🗖 Pref1/P30
P32	17		24 🗖 P36
P33	1 8		23 🗖 P37
P34	□ 19		22 🗖 P35
NC	20		21 🗖 RESET

Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.



40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC

Table 5. 40- and 48-Pin Configuration (Continued)

13

Table 9. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	25			Cycles	1

Notes:

1. For windowed cerdip package only.

2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

AF = exp[(Ea/k)*(1/Tuse - 1/TStress)] Where: Ea is the intrinsic activation energy (eV; typ. 0.8) k is Boltzman's constant (8.67 x 10-5 eV/°K) °K = -273.16°C Tuse = Use Temperature in °K TStress = Stress Temperature in °K 3. At a stable UV Lamp output of 20mW/CM²



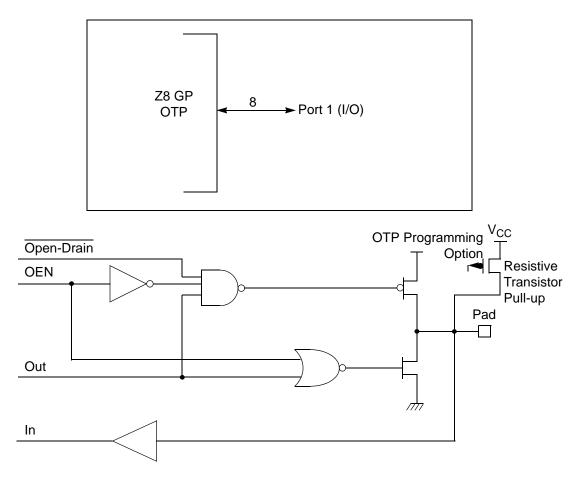


Figure 10. Port 1 Configuration

Port 2 (P27-P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.



Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP^{TM} asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP^{TM} does not assert the RESET pin when under VBO.



Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®], functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

>

Note: An expanded register bank is also referred to as an expanded register group (see Figure 15).



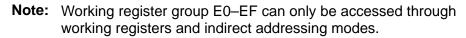
The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTRL0
LD	1, #xx	;	load CTRL1
LD	R1, 2	;	$CTRL2 \rightarrow CTRL1$
LD	RP, #0Dh	;	Select ERF D
for access to bank D	,	,	
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 \rightarrow register 71h			
LD	R1, 2		
; CTRL2 \rightarrow register 71h			

Register File

>

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.





Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data



When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.

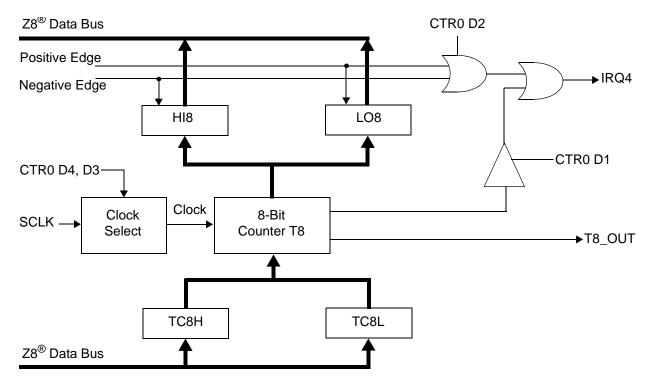


Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Ca

Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.

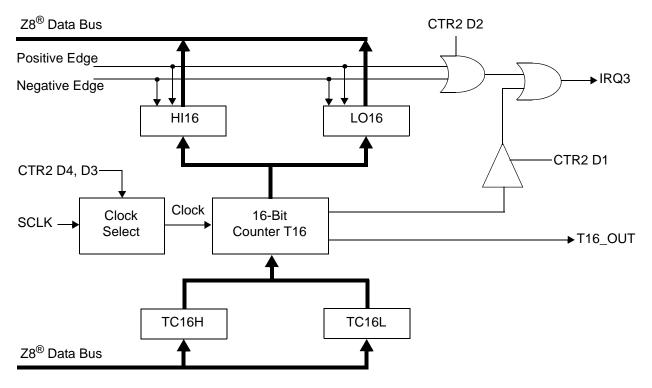


Figure 25. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in "Interrupts" on page 48.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.



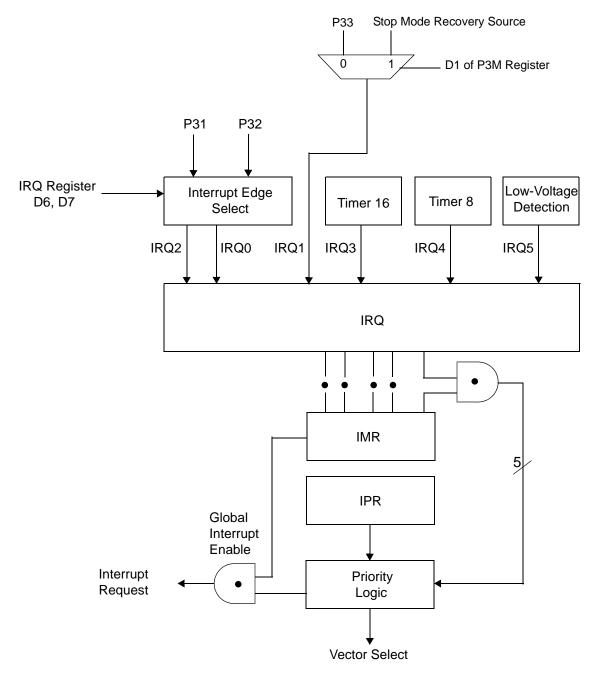


Figure 30. Interrupt Block Diagram



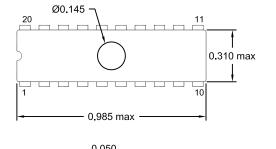
CTR1(0D)01H D7 D6 D5 D3 D1 D0 D4 D2 Transmit Mode* R/W 0 T16_OUT is 0 initially* 1 T16_OUT is 1 initially **Demodulation Mode** R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially **Demodulation Mode** R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 **Demodulation Mode** 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 1 Reserved Transmit Mode/T8/T16 Logic 0 0 AND** 0 1 OR 1 0 NOR 1 1 NAND **Demodulation Mode** 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 1 Reserved Transmit Mode 0 P36 as Port Output * 1 P36 as T8/T16_OUT **Demodulation Mode** 0 P31 as Demodulator Input 1 P20 as Demodulator Input Transmit/Demodulation Mode 0 Transmit Mode * * Default setting after reset **Default setting after reset. Not reset with Stop Mode 1 Demodulation Mode recovery

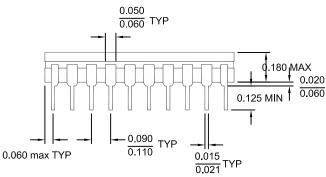




Package Information

Package information for all versions of Z8 GPTM OTP MCU Family are depicted in Figures 58 through Figure 68.





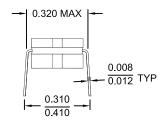
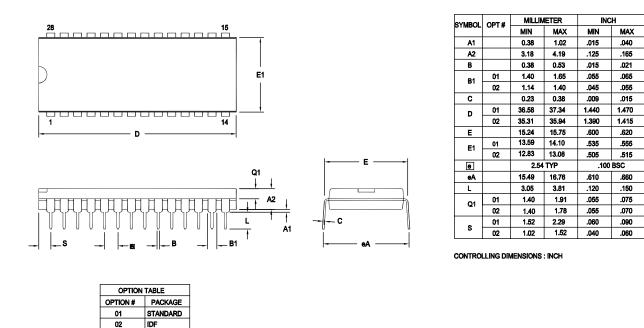


Figure 58. 20-Pin CDIP Package





Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 64. 28-Pin PDIP Package Diagram

INCH

NOM

0.073

0.005

0.068

0.006

0.402

0.209

0.307

0.030

0.0256 TYP



MAX

0.078

0.008

0.070

0.015

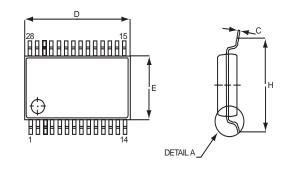
0.008

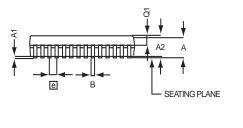
0.407

0.212

0.311

0.037





0-8°

DETAIL 'A'

SYMBOL

А

A1

A2

В

С

D

Е

е

Н

L

MIN

1.73

0.05

1.68

0.25

0.09

10.07

5.20

7.65

0.63

CONTROLLING DIMENSIONS: MM LEADS ARE COPLANAR WITHIN .004 INCHES.

MILLIMETER

NOM

1.86

0.13

1.73

_

10.20

5.30

0.65 TYP

7.80

0.75

MAX

1.99

0.21

1.78

0.38

0.20

10.33

5.38

7.90

0.95

MIN

0.068

0.002

0.066

0.010

0.004

0.397

0.205

0.301

0.025

Figure 65. 28-Pin SSOP Package Diagram



Ordering Information

32KB Standard Temperature: 0° to +70°C

	•		
Part Number	Description	Part Number	Description
ZGP323LSH4832C	48-pin SSOP 32K OTP	ZGP323LSS2832C	28-pin SOIC 32K OTP
ZGP323LSP4032C	40-pin PDIP 32K OTP	ZGP323LSH2032C	20-pin SSOP 32K OTP
ZGP323LSH2832C	28-pin SSOP 32K OTP	ZGP323LSP2032C	20-pin PDIP 32K OTP
ZGP323LSP2832C	28-pin PDIP 32K OTP	ZGP323LSS2032C	20-pin SOIC 32K OTP
ZGP323LSK2032E	20-pin CDIP 32K OTP	ZGP323LSK4032E	40-pin CDIP 32K OTP
		ZGP323LSK2832E	28-pin CDIP 32K OTP

32KB Extended Temperature: -40° to +105°C

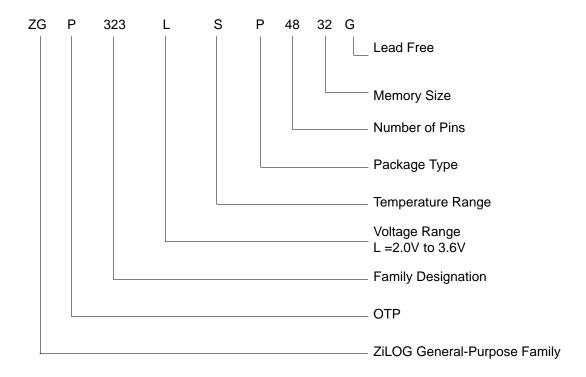
Part Number	Description	Part Number	Description
ZGP323LEH4832C	48-pin SSOP 32K OTP	ZGP323LES2832C	28-pin SOIC 32K OTP
ZGP323LEP4032C	40-pin PDIP 32K OTP	ZGP323LEH2032C	20-pin SSOP 32K OTP
ZGP323LEH2832C	28-pin SSOP 32K OTP	ZGP323LEP2032C	20-pin PDIP 32K OTP
ZGP323LEP2832C	28-pin PDIP 32K OTP	ZGP323LES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C

	•	1		
Part Number	Description	Part Number	Description	
ZGP323LAH4832C	48-pin SSOP 32K OTP	ZGP323LAS2832C	28-pin SOIC 32K OTP	
ZGP323LAP4032C	40-pin PDIP 32K OTP	ZGP323LAH2032C	20-pin SSOP 32K OTP	
ZGP323LAH2832C	28-pin SSOP 32K OTP	ZGP323LAP2032C	20-pin PDIP 32K OTP	
ZGP323LAP2832C	28-pin PDIP 32K OTP	ZGP323LAS2032C	20-pin SOIC 32K OTP	
Note: Replace C with G for Lead-Free Packaging				



Example





Index

Numerics

16-bit counter/timer circuits 44 20-pin DIP package diagram 81 20-pin SSOP package diagram 82 28-pin DIP package diagram 85 28-pin SOICpackage diagram 84 28-pin SSOP package diagram 86 40-pin DIP package diagram 87 48-pin SSOP package diagram 88 8-bit counter/timer circuits 40

Α

absolute maximum ratings 10 AC characteristics 14 timing diagram 14 address spaces, basic 2 architecture 2 expanded register file 26

В

basic address spaces 2 block diagram, ZLP32300 functional 3

С

capacitance 11 characteristics AC 14 DC 11 clock 51 comparator inputs/outputs 23 configuration port 0 17 port 1 18 port 2 19 port 3 20 port 3 counter/timer 22 counter/timer 16-bit circuits 44 8-bit circuits 40 brown-out voltage/standby 62 clock 51 demodulation mode count capture flowchart 42 demodulation mode flowchart 43 EPROM selectable options 62 glitch filter circuitry 38 halt instruction 52 input circuit 38 interrupt block diagram 49 interrupt types, sources and vectors 50 oscillator configuration 51 output circuit 47 ping-pong mode 46 port configuration register 53 resets and WDT 61 SCLK circuit 56 stop instruction 52 stop mode recovery register 55 stop mode recovery register 2 59 stop mode recovery source 57 T16 demodulation mode 45 T16 transmit mode 44 T16_OUT in modulo-N mode 45 T16 OUT in single-pass mode 45 T8 demodulation mode 41 T8 transmit mode 38 T8 OUT in modulo-N mode 41 T8 OUT in single-pass mode 41 transmit mode flowchart 39 voltage detection and flags 63 watch-dog timer mode register 60 watch-dog timer time select 61 CTR(D)01h T8 and T16 Common Functions 33