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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323les2032g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR
- **Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 K $\Omega$  ±50% at V<sub>CC</sub>=3 V and 450 K $\Omega$  ±50% at  $V_{CC}=2$  V.

## **General Description**

The Z8 GP<sup>TM</sup> OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG<sup>®</sup>'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z8 GP<sup>TM</sup> OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to registermapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8<sup>®</sup> offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of userselectable modes and two on-board comparators to process analog signals with separate reference voltages.

**Note:** All signals with an overline, "", are active Low. For example,  $B/\overline{W}$ , in which WORD is active Low, and  $\overline{B}/W$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.





#### Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 3.	20-Pin PDIP/SOIC/SSOP/CDIP*	Pin	Identification
			achtinoution

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20-P24	Port 2, Bits 0,1,2,3,4	Input/Output

**Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

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## Z8 GP<sup>TM</sup> OTP MCU Family Product Specification



	1		1 7			
NC		1	$\bigcirc$	18	_	NC
DOF		2		40		NC
P20		2		47		NC DO4
P26		3		40		P24
P27		4		45		P23
P04	E	5		44		P22
N/C		6		43		P21
P05		7		42		P20
P06		8		41		P03
P14		9		40		P13
P15		10		39		P12
P07	E	11	40 D'	38		VSS
VDD	E	12	48-PIN	37		VSS
VDD		13	330P	36		N/C
N/C	C	14		35		P02
P16		15		34		P11
P17		16		33		P10
XTAL2		17		32		P01
XTAL1		18		31		P00
P31		19		30		N/C
P32		20		29		PREF1/P30
P33		21		28		P36
P34		22		27		P37
NC		23		26	_	P35
VSS	H	20		20	_	RESET
.00	_	24		20		

Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



## **Absolute Maximum Ratings**

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

#### Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximu	m Units	Notes
Ambient temperature under bias	0	+70	С	
Storage temperature	-65	+150	С	
Voltage on any pin with respect to V <sub>SS</sub>	-0.3	+5.5	V	1
Voltage on $V_{DD}$ pin with respect to $V_{SS}$	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into $V_{DD}$ or out of $V_{SS}$		75	mA	
Notes:				

This voltage applies to all pins except the following: V<sub>DD</sub>, P32, P33 and RESET.

## **Standard Test Conditions**

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).



Figure 7. Test Load Diagram



CTR1(0D)01H" on page 33). Other edge detect and IRQ modes are described in Table 11.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

#### Table 11. Port 3 Pin Function Summary

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Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.



#### **Comparator Inputs**

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

#### **Comparator Outputs**

These channels can be programmed to be output on P34 and P37 through the PCON register.

## **RESET (Input, Active Low)**

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8  $GP^{TM}$  asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8  $GP^{TM}$  does not assert the RESET pin when under VBO.



**Note:** The external Reset does not initiate an exit from STOP mode.

## **Functional Description**

This device incorporates special functions to enhance the Z8<sup>®</sup>, functionality in consumer and battery-operated applications.

#### **Program Memory**

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

#### RAM

This device features 256B of RAM. See Figure 14.



#### Timers

#### T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description	
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect	

#### T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description	
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect	

#### T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description	
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect	

#### T16\_Capture\_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

#### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field Bit Position			Description
T16_Data_HI	[7:0]	R/W	Data

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#### T8/T16\_Logic/Edge \_Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

#### Transmit\_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to "NORMAL OPERATION Mode" terminates the "PING-PONG Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

#### Initial\_T8\_Out/Rising\_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

#### Initial\_T16 Out/Falling \_Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

**Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16\_OUT.

#### CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 14 lists and briefly describes the fields for this register.



into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).



Figure 23. Demodulation Mode Count Capture Flowchart



#### **During PING-PONG Mode**

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

#### **Timer Output**

The output logic for the timers is illustrated in Figure 29. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

#### Interrupts

The Z8 GP<sup>TM</sup> OTP MCU Family features six different interrupts (Table 16). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/ timers (Table 16) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 57.

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#### Table 20. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

#### WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



\* CLR1 and CLR2 enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

#### Figure 38. Resets and WDT



#### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

#### **EPROM Selectable Options**

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

#### Table 21. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

#### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V<sub>DD</sub> is at the required level for correct operation of the device. Reset is globally driven when V<sub>DD</sub> falls below V<sub>BO</sub>. A small drop in V<sub>DD</sub> causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V<sub>DD</sub> is allowed to stay above V<sub>RAM</sub>, the RAM content is preserved. When the power level is returned to above V<sub>BO</sub>, the device performs a POR and functions normally.



#### SMR(0F)0BH



- \* Default setting after Reset
- \* \* Set after STOP Mode Recovery
- \* \* \* At the XOR gate input
- \*\*\*\* Default setting after Reset. Must be 1 if using a crystal or resonator clock source.
- \* \* \* \* \* Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

# Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)



#### WDTMR(0F)0FH



\* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

## **Standard Control Registers**

#### R246 P2M(F6H)



\* Default setting after reset

#### Figure 48. Port 2 Mode Register (F6H: Write Only)



#### R254 SPH(FEH)



General-Purpose Register

#### Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

D7 D6 D5 D4	D3	D2	D1	D0
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Stack Pointer Low Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)









Figure 62. 28-Pin CDIP Package





![](_page_17_Figure_2.jpeg)

Figure 63. 28-Pin SOIC Package Diagram

![](_page_18_Picture_1.jpeg)

#### 16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4816C	48-pin SSOP 16K OTP	ZGP323LSS2816C	28-pin SOIC 16K OTP
ZGP323LSP4016C	40-pin PDIP 16K OTP	ZGP323LSH2016C	20-pin SSOP 16K OTP
ZGP323LSH2816C	28-pin SSOP 16K OTP	ZGP323LSP2016C	20-pin PDIP 16K OTP
ZGP323LSP2816C	28-pin PDIP 16K OTP	ZGP323LSS2016C	20-pin SOIC 16K OTP

#### 16KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4816C	48-pin SSOP 16K OTP	ZGP323LES2816C	28-pin SOIC 16K OTP
ZGP323LEP4016C	40-pin PDIP 16K OTP	ZGP323LES2016C	20-pin SOIC 16K OTP
ZGP323LEH2816C	28-pin SSOP 16K OTP	ZGP323LEH2016C	20-pin SSOP 16K OTP
ZGP323LEP2816C	28-pin PDIP 16K OTP	ZGP323LEP2016C	20-pin PDIP 16K OTP

#### 16KB Automotive Temperature: -40° to +125°C

Dort Number	Description	Dort Number	Description
Part Number	Description	Part Number	Description
ZGP323LAH4816C	48-pin SSOP 16K OTP	ZGP323LAS2816C	28-pin SOIC 16K OTP
ZGP323LAP4016C	40-pin PDIP 16K OTP	ZGP323LAH2016C	20-pin SSOP 16K OTP
ZGP323LAH2816C	28-pin SSOP 16K OTP	ZGP323LAP2016C	20-pin PDIP 16K OTP
ZGP323LAP2816C	28-pin PDIP 16K OTP	ZGP323LAS2016C	20-pin SOIC 16K OTP
Note: Replace C with G for Lead-Free Packaging			

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#### 4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4804C	48-pin SSOP 4K OTP	ZGP323LSS2804C	28-pin SOIC 4K OTP
ZGP323LSP4004C	40-pin PDIP 4K OTP	ZGP323LSH2004C	20-pin SSOP 4K OTP
ZGP323LSH2804C	28-pin SSOP 4K OTP	ZGP323LSP2004C	20-pin PDIP 4K OTP
ZGP323LSP2804C	28-pin PDIP 4K OTP	ZGP323LSS2004C	20-pin SOIC 4K OTP

#### 4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4804C	48-pin SSOP 4K OTP	ZGP323LES2804C	28-pin SOIC 4K OTP
ZGP323LEP4004C	40-pin PDIP 4K OTP	ZGP323LEH2004C	20-pin SSOP 4K OTP
ZGP323LEH2804C	28-pin SSOP 4K OTP	ZGP323LEP2004C	20-pin PDIP 4K OTP
ZGP323LEP2804C	28-pin PDIP 4K OTP	ZGP323LES2004C	20-pin SOIC 4K OTP

#### 4KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4804C	48-pin SSOP 4K OTP	ZGP323LAS2804C	28-pin SOIC 4K OTP
ZGP323LAP4004C	40-pin PDIP 4K OTP	ZGP323LAH2004C	20-pin SSOP 4K OTP
ZGP323LAH2804C	28-pin SSOP 4K OTP	ZGP323LAP2004C	20-pin PDIP 4K OTP
ZGP323LAP2804C	28-pin PDIP 4K OTP	ZGP323LAS2004C	20-pin SOIC 4K OTP

#### Note: Replace C with G for Lead-Free Packaging

#### **Additional Components**

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer	ZGP32300100ZPR	Programming System

## Z8 GP<sup>™</sup> OTP MCU Family Product Specification

![](_page_20_Picture_1.jpeg)

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