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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 16 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323lsh2016g |

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## Document Disclaimer

# Table of Contents

- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

**Note:** The mask option pull-up transistor has a *typical* equivalent resistance of 200 KΩ ±50% at $V_{CC}$=3 V and 450 KΩ ±50% at $V_{CC}$=2 V.

## General Description

The Z8 GP™ OTP MCU Family is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z8 GP™ OTP MCU Family architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP MCU offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

**Note:** All signals with an overline, "$\overline{\ }$", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.

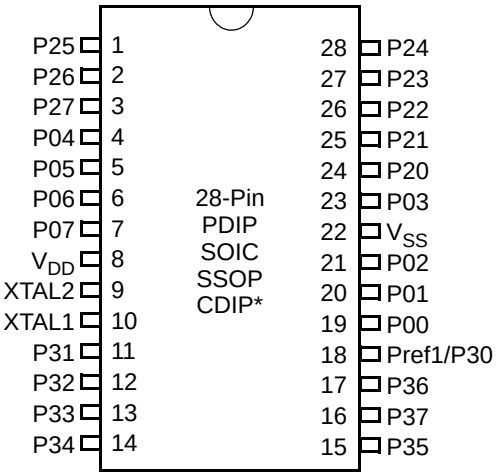



**Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration**

**Table 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification**

| Pin | Symbol | Direction | Description |
|---|---|---|---|
| 1-3 | P25-P27 | Input/Output | Port 2, Bits 5,6,7 |
| 4-7 | P04-P07 | Input/Output | Port 0, Bits 4,5,6,7 |
| 8 | $V_{DD}$ | | Power supply |
| 9 | XTAL2 | Output | Crystal, oscillator clock |
| 10 | XTAL1 | Input | Crystal, oscillator clock |
| 11-13 | P31-P33 | Input | Port 3, Bits 1,2,3 |
| 14 | P34 | Output | Port 3, Bit 4 |
| 15 | P35 | Output | Port 3, Bit 5 |
| 16 | P37 | Output | Port 3, Bit 7 |
| 17 | P36 | Output | Port 3, Bit 6 |
| 18 | Pref1/P30<br>Port 3 Bit 0 | Input | Analog ref input; connect to $V_{CC}$ if not used<br>Input for Pref1/P30 |
| 19-21 | P00-P02 | Input/Output | Port 0, Bits 0,1,2 |
| 22 | $V_{SS}$ | | Ground |
| 23 | P03 | Input/Output | Port 0, Bit 3 |
| 24-28 | P20-P24 | Input/Output | Port 2, Bits 0-4 |

**Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

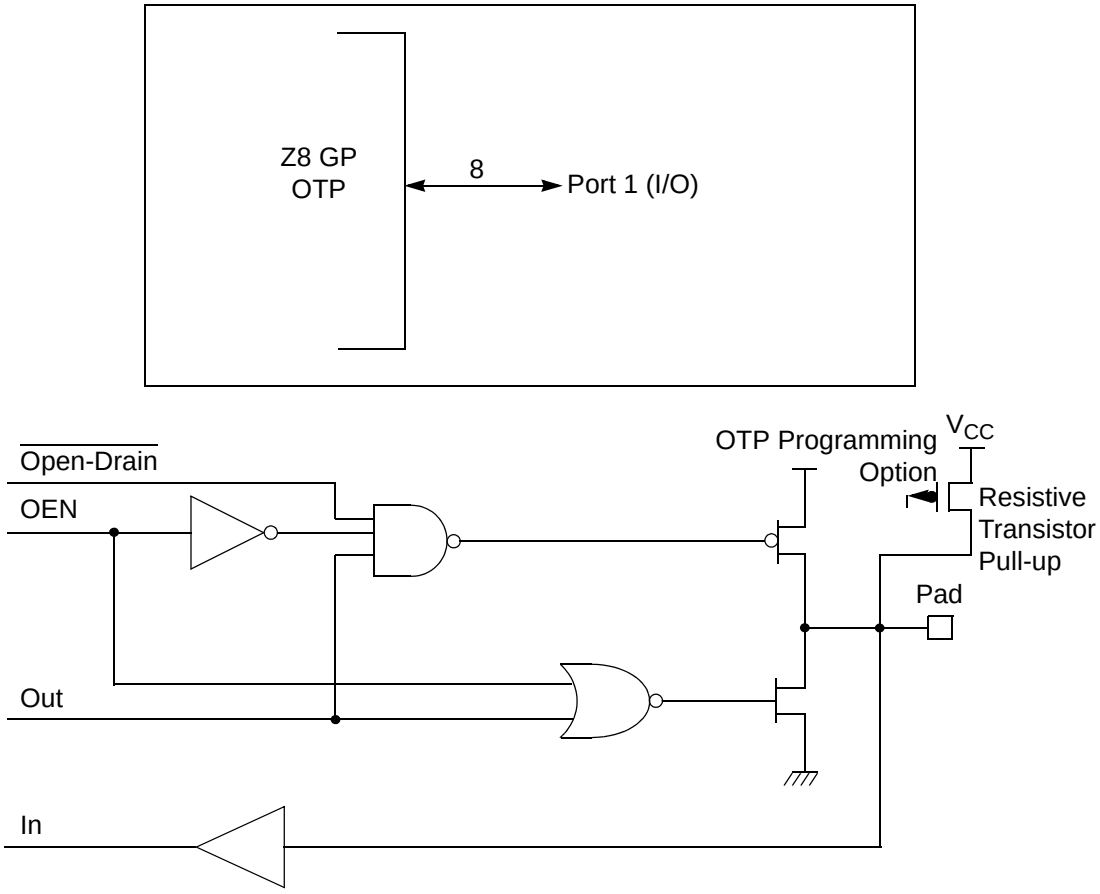



**Figure 10. Port 1 Configuration**

## Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

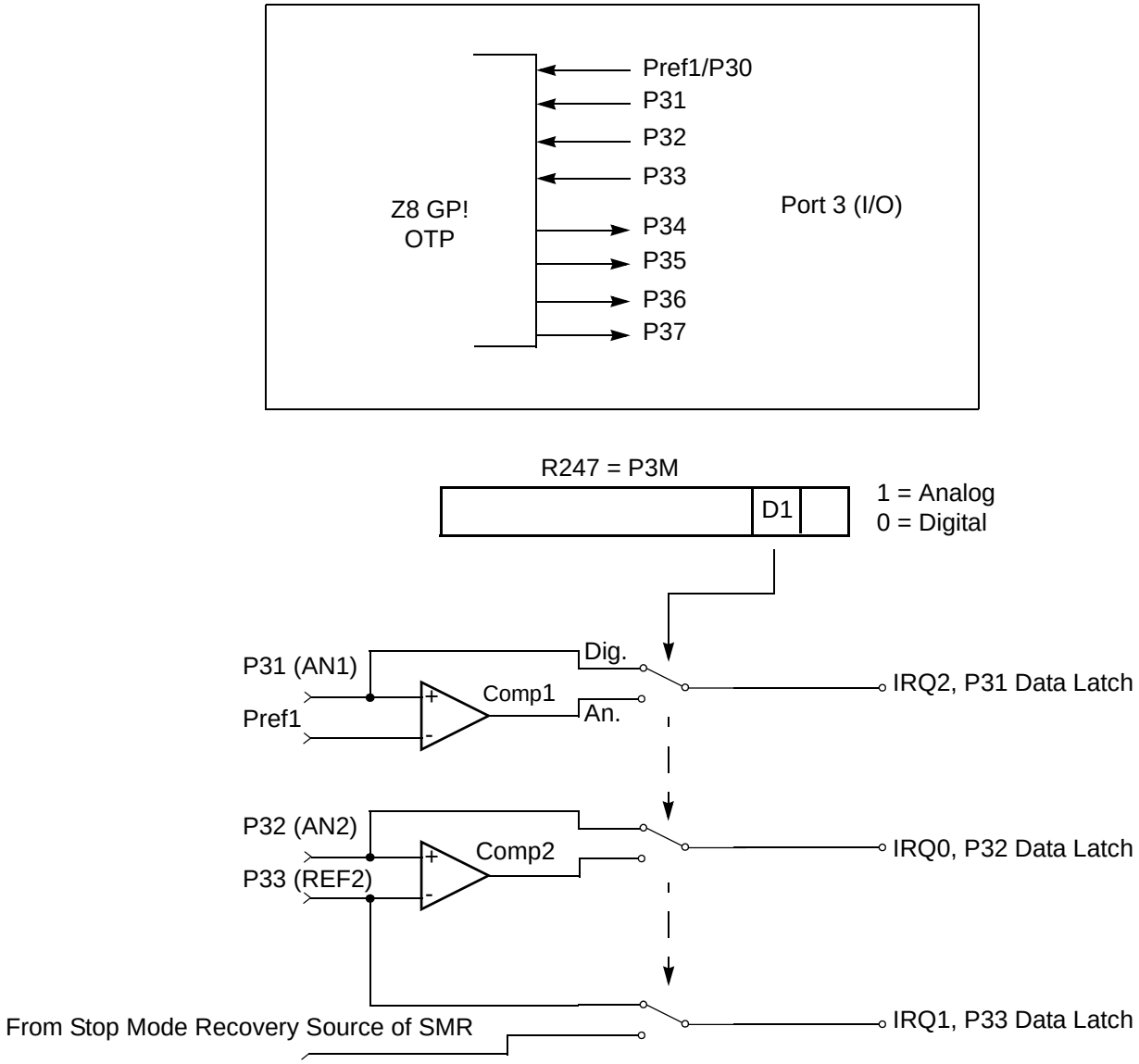



**Figure 12. Port 3 Configuration**

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—

### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## $\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP™ asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP™ does not assert the $\overline{\text{RESET}}$ pin when under VBO.

**Note:** The external Reset does not initiate an exit from STOP mode.

# Functional Description

This device incorporates special functions to enhance the Z8®, functionality in consumer and battery-operated applications.

## Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

## RAM

This device features 256B of RAM. See Figure 14.

**Table 12. CTR0(D)00H Counter/Timer8 Control Register (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Counter_INT_Mask | ------1- | R/W | 0<br>1 | Disable Time-Out Interrupt<br>Enable Time-Out Interrupt |
| P34_Out | -------0 | R/W | 0*<br>1 | P34 as Port Output<br>T8 Output on P34 |

**Note:**
*Indicates the value upon Power-On Reset.

### T8 Enable

This field enables T8 when set (written) to 1.

### Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

### Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.

**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

**Note:** Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

### T8 Clock

This bit defines the frequency of the input signal to T8.

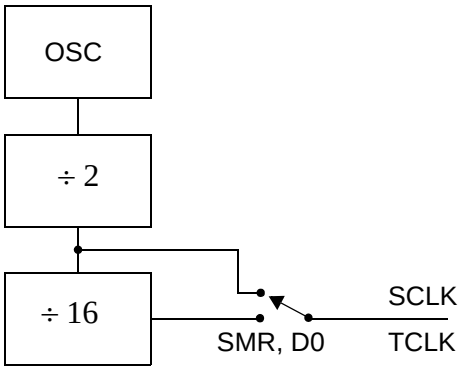



**Figure 34. SCLK Circuit**

### Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 19).

### Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 18 lists and briefly describes the fields for this register.

**Table 18. SMR2(F)0DH:Stop Mode Recovery Register 2***

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Reserved | 7------- | | 0 | Reserved (Must be 0) |
| Recovery Level | -6------ | W | 0†<br>1 | Low<br>High |
| Reserved | --5----- | | 0 | Reserved (Must be 0) |
| Source | ---432-- | W | 000†<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | A. POR Only<br>B. NAND of P23–P20<br>C. NAND of P27–P20<br>D. NOR of P33–P31<br>E. NAND of P33–P31<br>F. NOR of P33–P31, P00, P07<br>G. NAND of P33–P31, P00, P07<br>H. NAND of P33–P31, P22–P20 |
| Reserved | ------10 | | 00 | Reserved (Must be 0) |

**Notes:**
* Port pins configured as outputs are ignored as a SMR recovery source.
† Indicates the value upon Power-On Reset

### Low-Voltage Detection Register—LVD(D)0Ch

**Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

| Field | Bit Position | | | Description |
|---|---|---|---|---|
| LVD | 76543--- | | | Reserved<br>No Effect |
| | -----2-- | R | 1<br>0* | HVD flag set<br>HVD flag reset |
| | ------1- | R | 1<br>0* | LVD flag set<br>LVD flag reset |
| | -------0 | R/W | 1<br>0* | Enable VD<br>Disable VD |

***Default after POR

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the $V_{CC}$ voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the $V_{CC}$ level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if $V_{CC}$ is higher than $V_{HVD.}$ The LVD flag (bit 1 of the LVD register) is set only if $V_{CC}$ is lower than the $V_{LVD}$. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

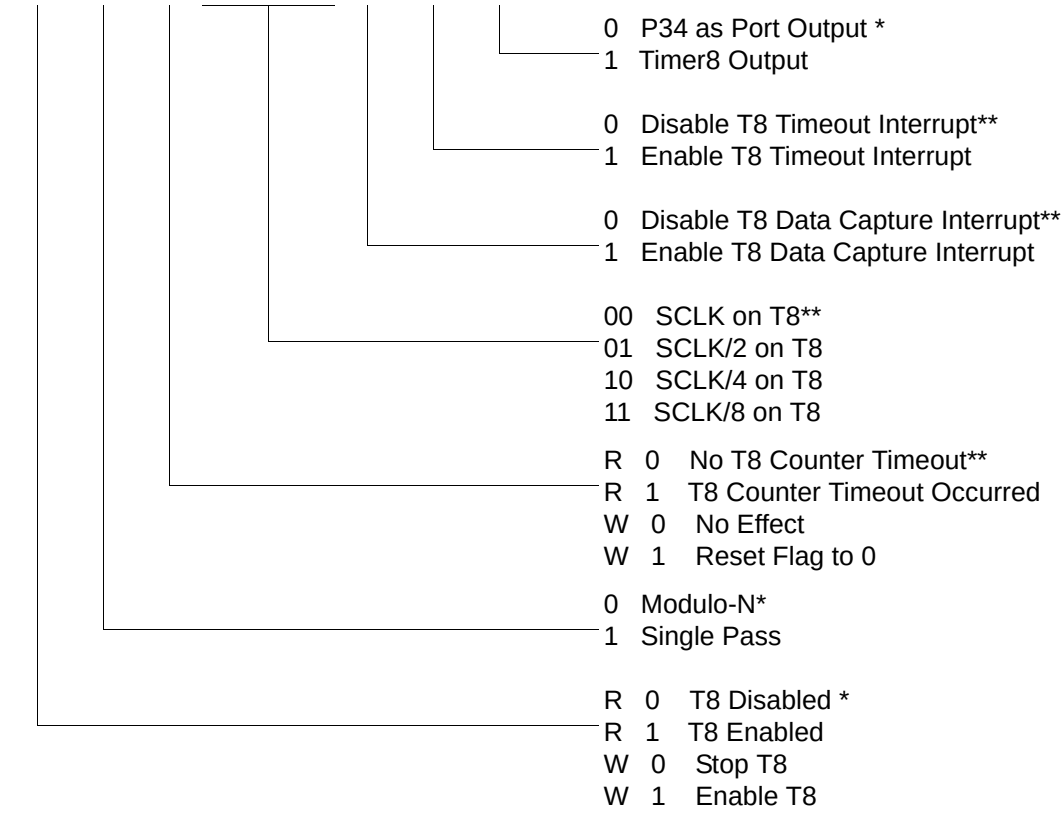
**Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

# Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|




* Default setting after reset
**Default setting after reset. Not reset with Stop Mode recovery.

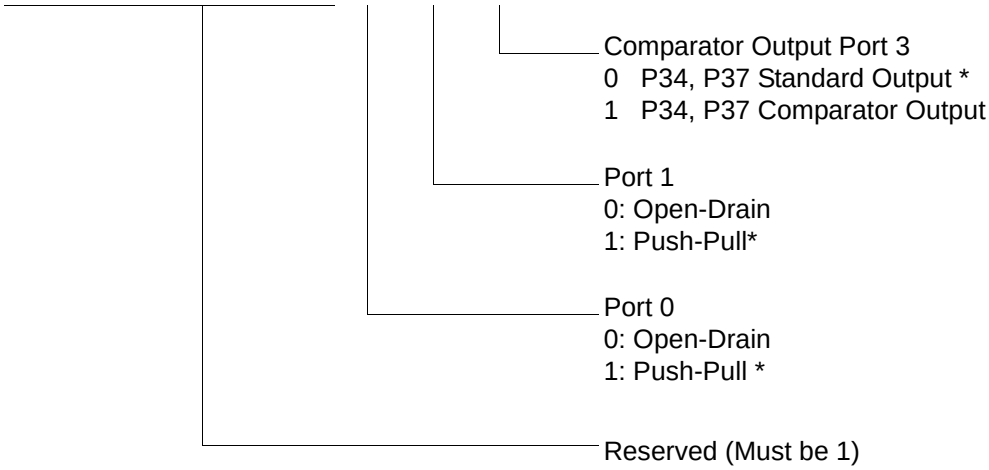
**Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)**

**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

PCON(0F)00H

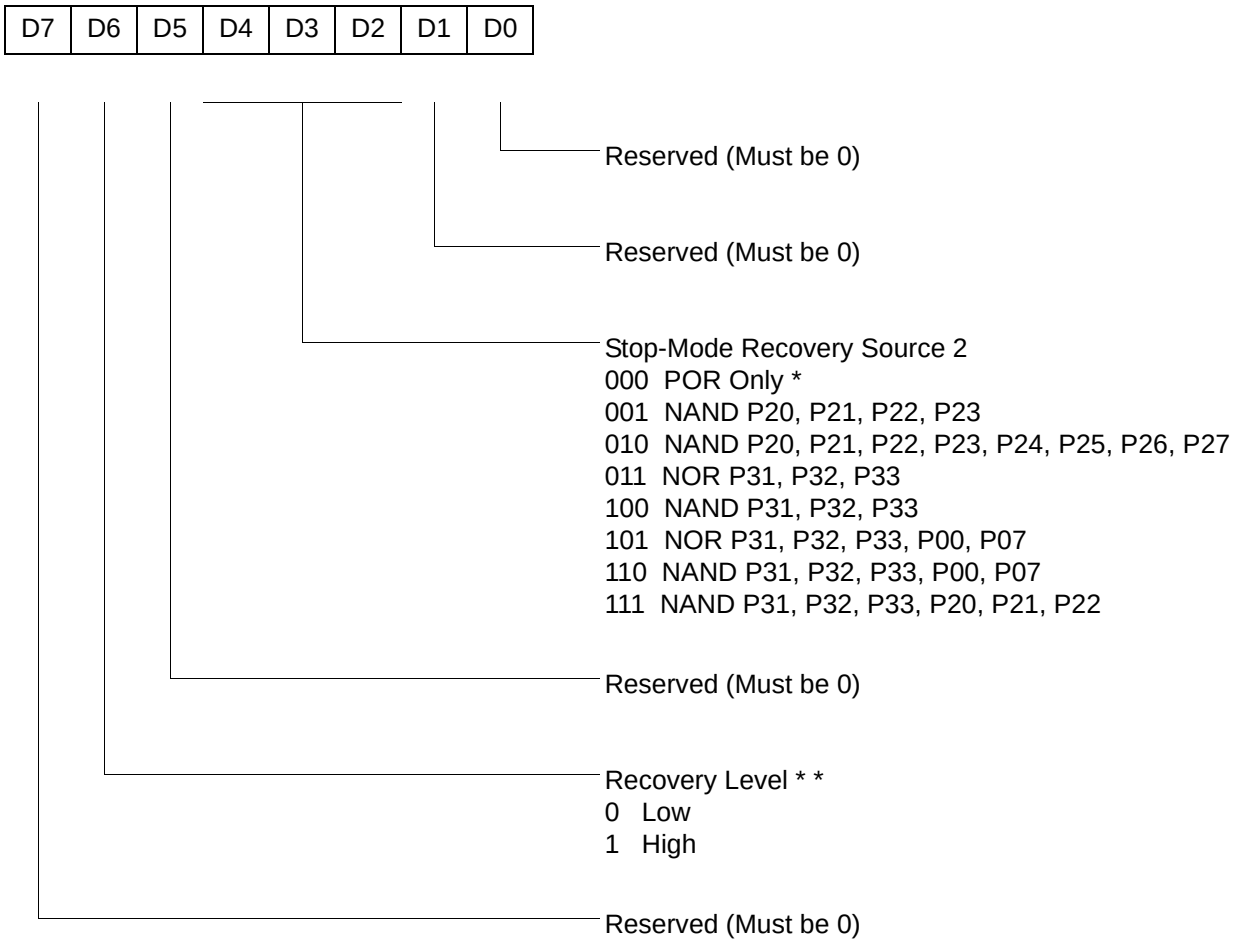
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|




* Default setting after reset

**Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)**

SMR2(0F)0DH




Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.
* Default setting after reset
* * At the XOR gate input

**Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)**

R249 IPR(F9H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

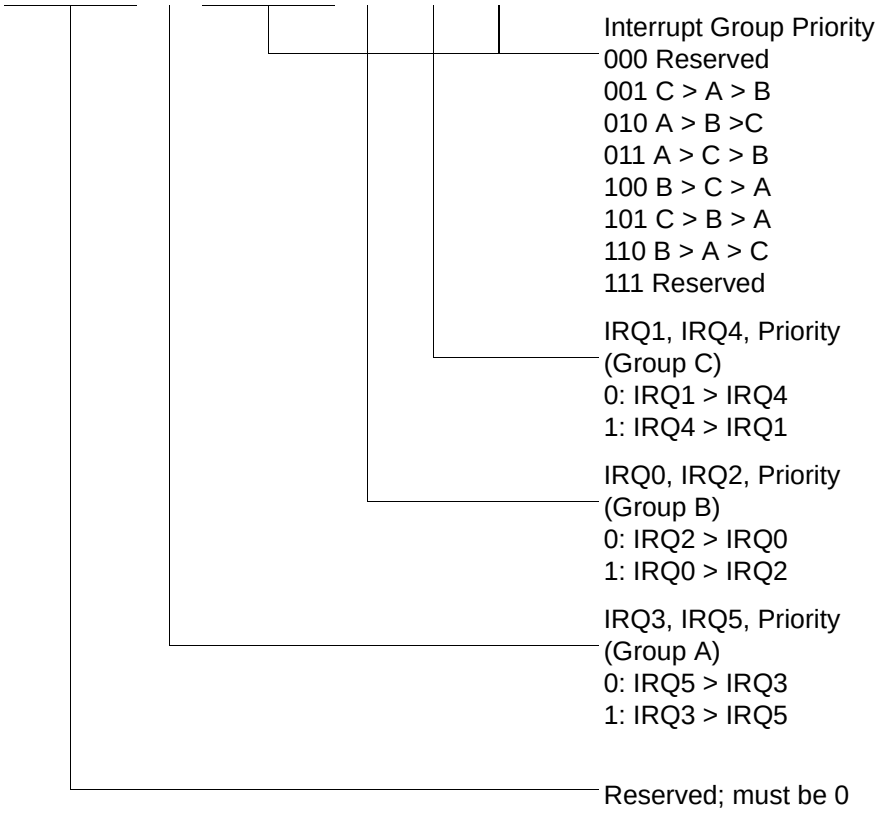



**Figure 51. Interrupt Priority Register (F9H: Write Only)**

R252 Flags(FCH)

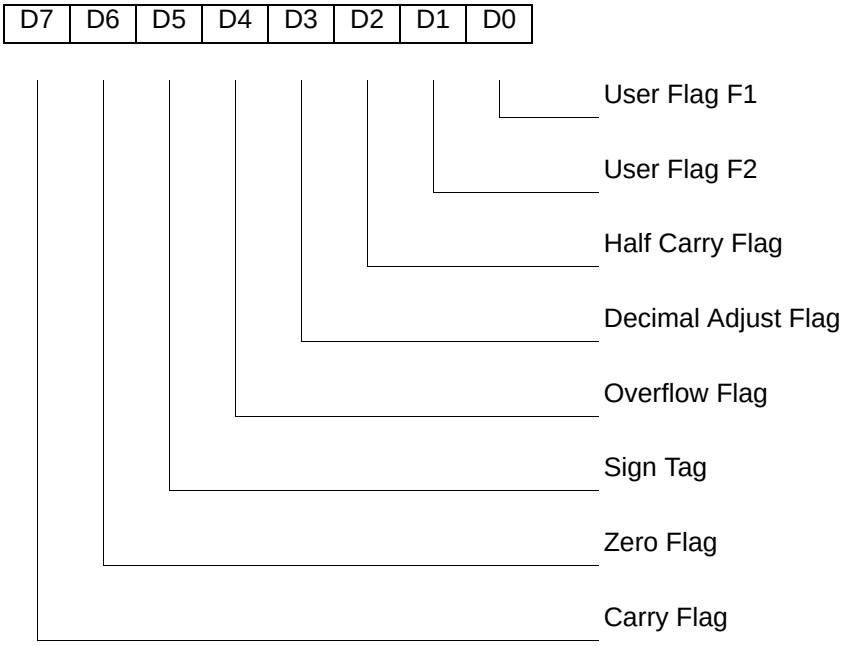
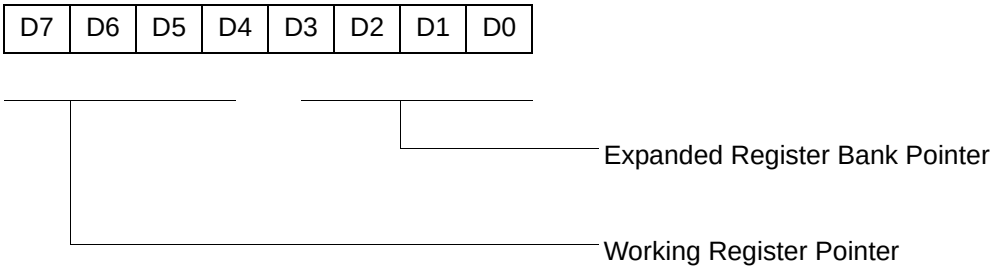


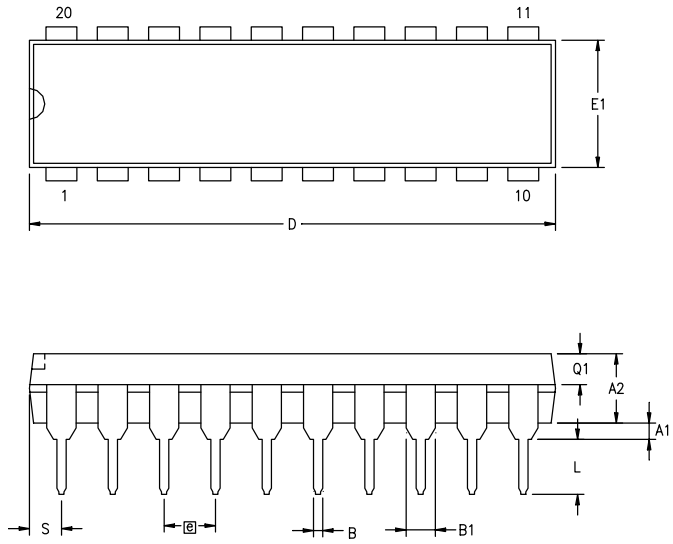

**Figure 54. Flag Register (FCH: Read/Write)**

R253 RP(FDH)




Default setting after reset = 0000 0000

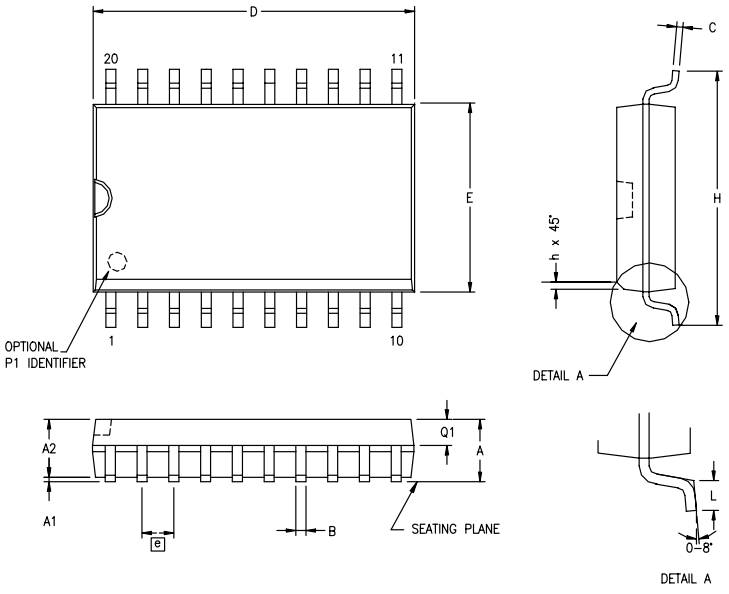
**Figure 55. Register Pointer (FDH: Read/Write)**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.38 | 0.81 | .015 | .032 |
| A2 | 3.25 | 3.68 | .128 | .145 |
| B | 0.41 | 0.51 | .016 | .020 |
| B1 | 1.47 | 1.57 | .058 | .062 |
| C | 0.20 | 0.30 | .008 | .012 |
| D | 25.65 | 26.16 | 1.010 | 1.030 |
| E | 7.49 | 8.26 | .295 | .325 |
| E1 | 6.10 | 6.65 | .240 | .262 |
| e | 2.54 BSC | | .100 BSC | |
| eA | 7.87 | 9.14 | .310 | .360 |
| L | 3.18 | 3.43 | .125 | .135 |
| Q1 | 1.42 | 1.65 | .056 | .065 |
| S | 1.52 | 1.65 | .060 | .065 |

CONTROLLING DIMENSIONS : INCH

**Figure 59. 20-Pin PDIP Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.65 | .094 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.24 | 2.44 | .088 | .096 |
| B | 0.36 | 0.46 | .014 | .018 |
| C | 0.23 | 0.30 | .009 | .012 |
| D | 12.60 | 12.95 | **.496** | .510 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 BSC | | .050 BSC | |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.30 | 0.40 | .012 | .016 |
| L | 0.60 | 1.00 | .024 | .039 |
| Q1 | 0.97 | 1.07 | .038 | .042 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 60. 20-Pin SOIC Package Diagram**

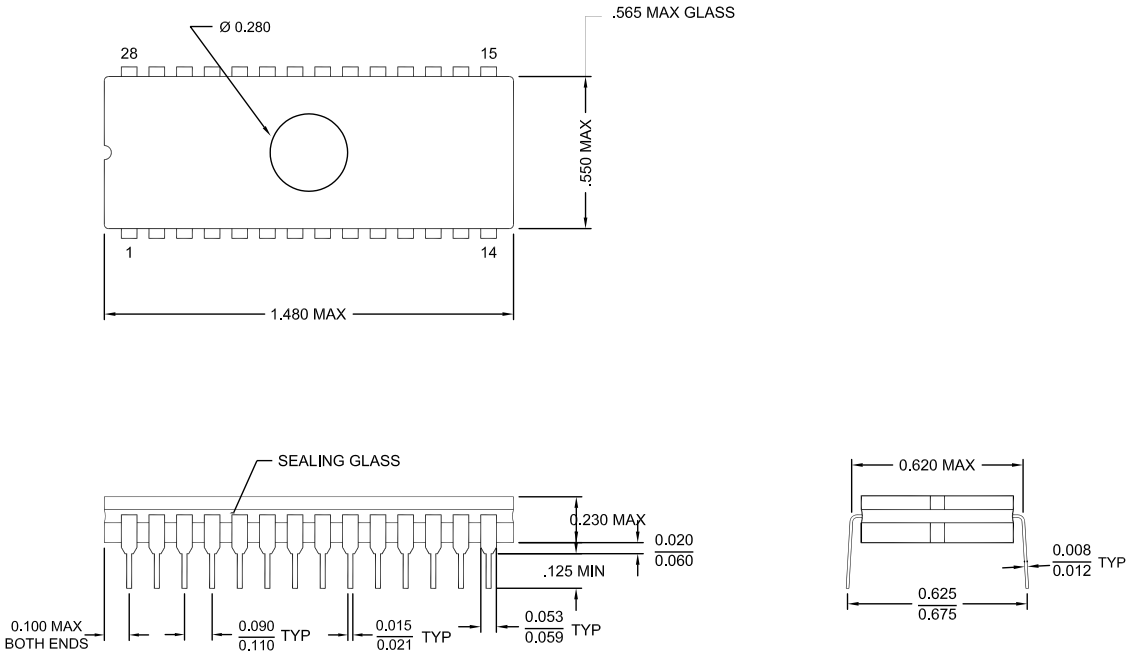



**Figure 62. 28-Pin CDIP Package**

| 4KB Standard Temperature: 0° to +70°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LSH4804C | 48-pin SSOP 4K OTP | ZGP323LSS2804C | 28-pin SOIC 4K OTP |
| ZGP323LSP4004C | 40-pin PDIP 4K OTP | ZGP323LSH2004C | 20-pin SSOP 4K OTP |
| ZGP323LSH2804C | 28-pin SSOP 4K OTP | ZGP323LSP2004C | 20-pin PDIP 4K OTP |
| ZGP323LSP2804C | 28-pin PDIP 4K OTP | ZGP323LSS2004C | 20-pin SOIC 4K OTP |

| 4KB Extended Temperature: -40° to +105°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LEH4804C | 48-pin SSOP 4K OTP | ZGP323LES2804C | 28-pin SOIC 4K OTP |
| ZGP323LEP4004C | 40-pin PDIP 4K OTP | ZGP323LEH2004C | 20-pin SSOP 4K OTP |
| ZGP323LEH2804C | 28-pin SSOP 4K OTP | ZGP323LEP2004C | 20-pin PDIP 4K OTP |
| ZGP323LEP2804C | 28-pin PDIP 4K OTP | ZGP323LES2004C | 20-pin SOIC 4K OTP |

| 4KB Automotive Temperature: -40° to +125°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323LAH4804C | 48-pin SSOP 4K OTP | ZGP323LAS2804C | 28-pin SOIC 4K OTP |
| ZGP323LAP4004C | 40-pin PDIP 4K OTP | ZGP323LAH2004C | 20-pin SSOP 4K OTP |
| ZGP323LAH2804C | 28-pin SSOP 4K OTP | ZGP323LAP2004C | 20-pin PDIP 4K OTP |
| ZGP323LAP2804C | 28-pin PDIP 4K OTP | ZGP323LAS2004C | 20-pin SOIC 4K OTP |

Note: Replace C with G for Lead-Free Packaging

| Additional Components | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323ICE01ZEM | Emulator/programmer | ZGP32300100ZPR | Programming System |

## Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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