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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

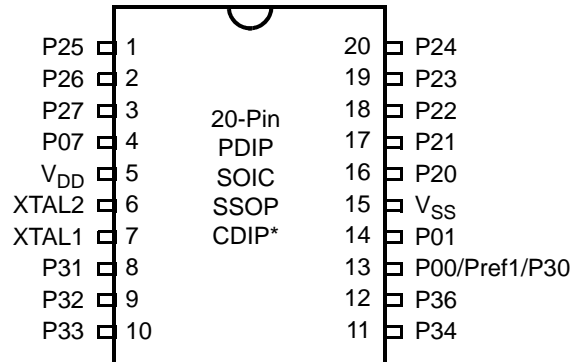
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323lsh2816g">https://www.e-xfl.com/product-detail/zilog/zgp323lsh2816g</a>



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**Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration**

**Table 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Identification**

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Table 10. AC Characteristics

T <sub>A</sub> =0°C to +70°C 8.0MHz							Watch-Dog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V <sub>CC</sub>	Minimum	Maximum	Units	Notes
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1
3	TwC	Input Clock Width	2.0–3.6	37		ns	1
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2
10	Twsm	Stop-Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1
13	T <sub>POR</sub>	Power-On Reset	2.0–3.6	2.5	10	ms	

Notes:

1. Timing Reference uses 0.9 V<sub>CC</sub> for a logic 1 and 0.1 V<sub>CC</sub> for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

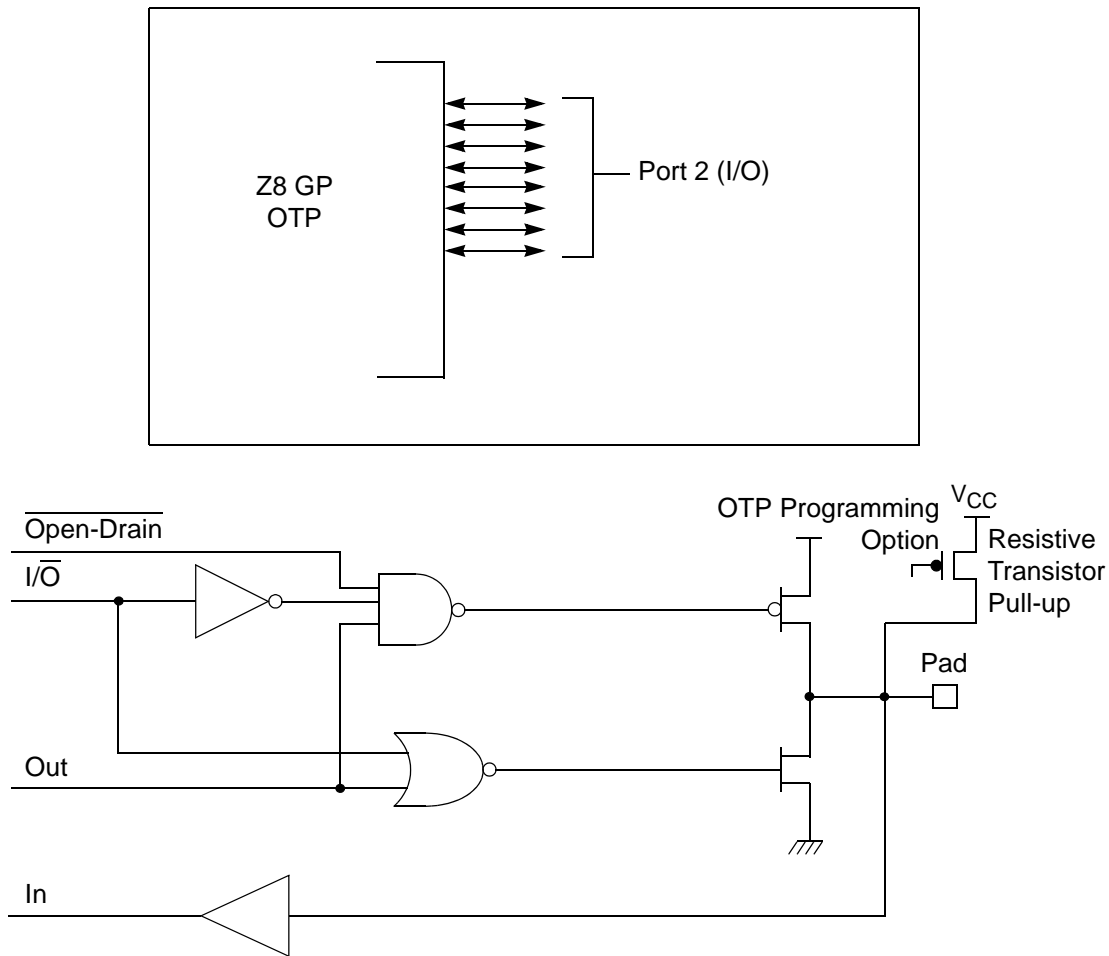


Figure 11. Port 2 Configuration

### Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

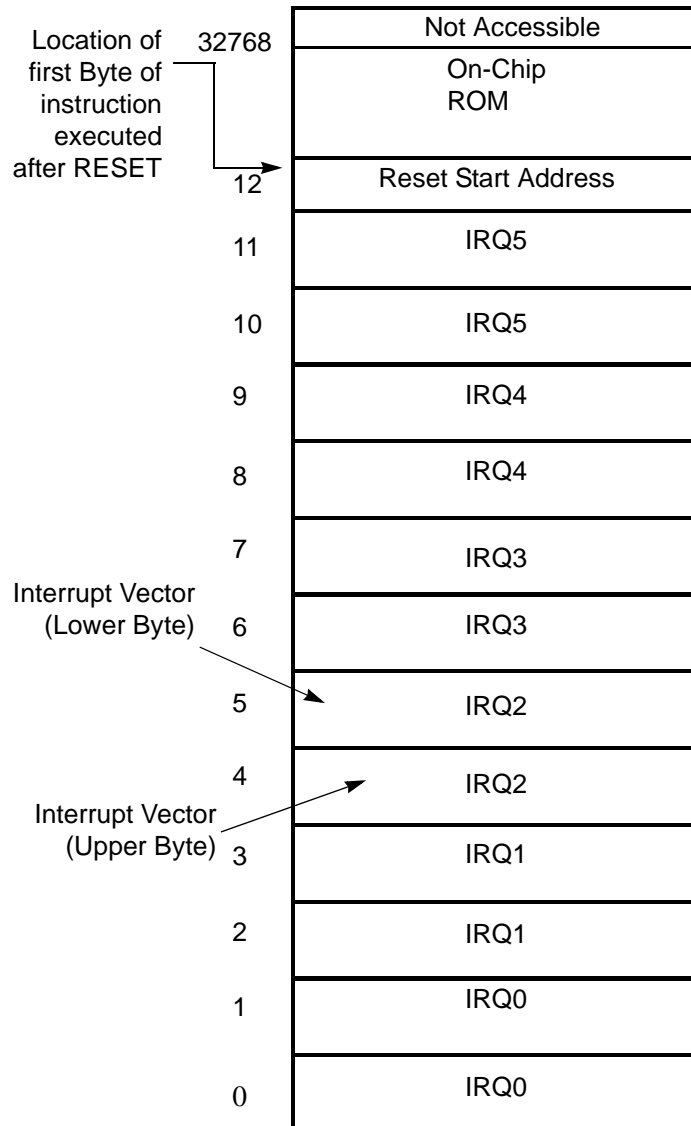
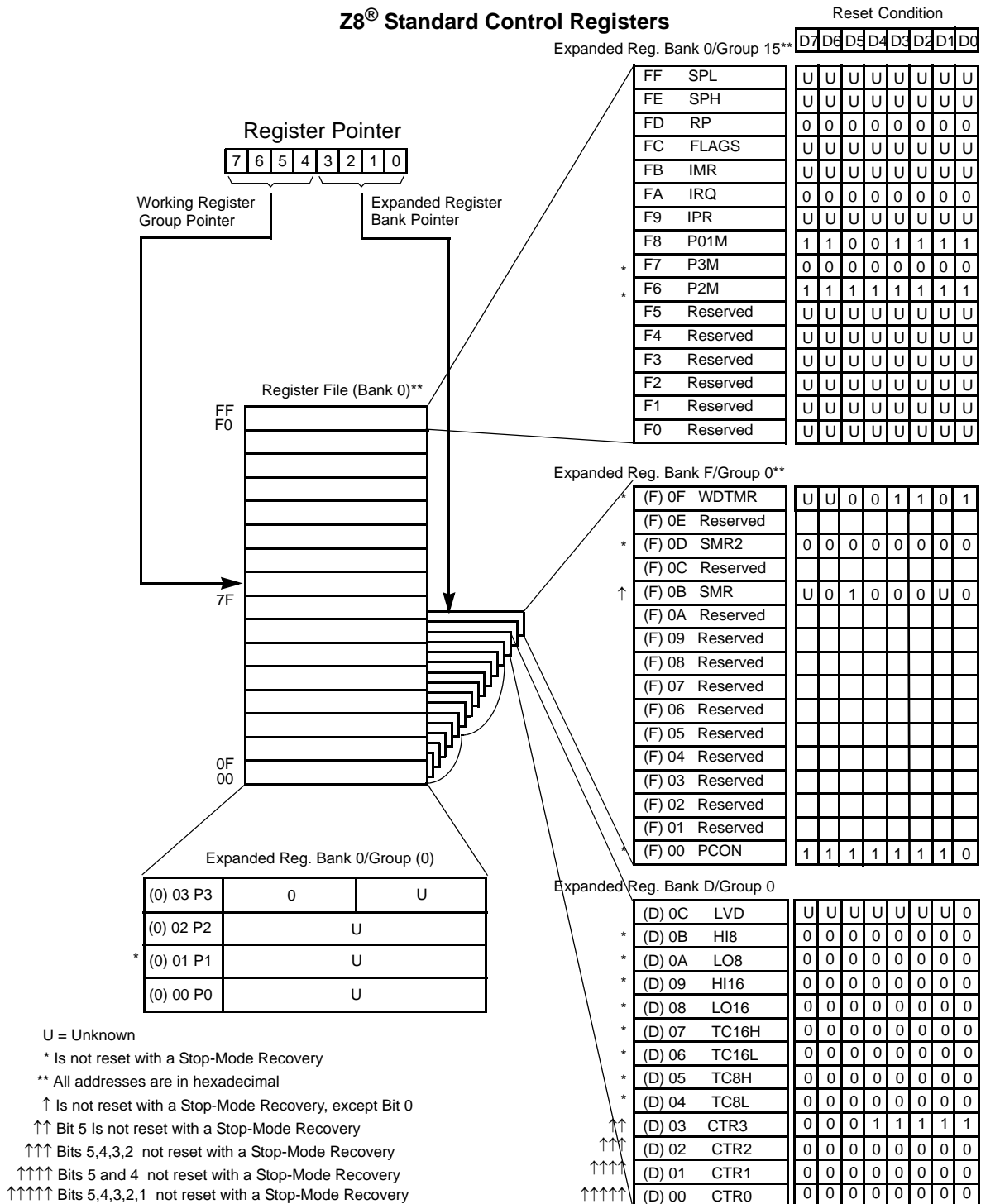


Figure 14. Program Memory Map (32K OTP)

## Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8® register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the

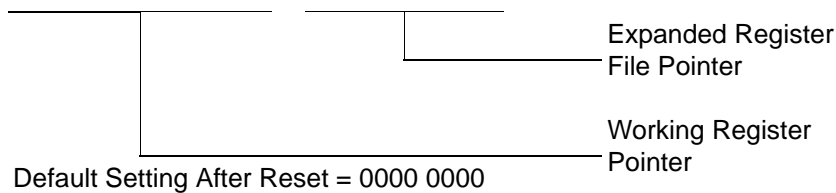


**Figure 15. Expanded Register File Architecture**

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



**Figure 16. Register Pointer**

**Example: Z8 GP: (See Figure 15 on page 26)**

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTRL0

R1 = CTRL1

R2 = CTRL2

R3 = Reserved



### Capture\_INT\_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter\_INT\_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

### T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 13 lists and briefly describes the fields for this register.

**Table 13. CTR1(0D)01H T8 and T16 Common Functions**

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0* 1  0 1	Transmit Mode Port Output T8/T16 Output Demodulation Mode P31 P20
T8/T16_Logic/ Edge_Detect	--54----	R/W	00** 01 10 11  00** 01 10 11	Transmit Mode AND OR NOR NAND Demodulation Mode Falling Edge Rising Edge Both Edges Reserved

Table 13. CTR1(0D)01H T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/ Glitch_Filter	----32--	R/W		Transmit Mode
			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/ Rising Edge	-----1-	R/W	0*	Transmit Mode
			1	T8_OUT is 0 Initially
		R	0*	T8_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Rising Edge
			1	Rising Edge Detected
			0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-----0	R/W	0*	Transmit Mode
			1	T16_OUT is 0 Initially
		R	0*	T16_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Falling Edge
			1	Falling Edge Detected
			0	No Effect
			1	Reset Flag to 0

**Note:**

\*Default at Power-On Reset.

\*\*Default at Power-On Reset. Not reset with Stop Mode recovery.

**Mode**

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

**P36\_Out/Demodulator\_Input**

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 45.

#### Time\_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

#### T16\_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

#### Capture\_INT\_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

#### Counter\_INT\_Mask

Set this bit to allow an interrupt when T16 times out.

#### P35\_Out

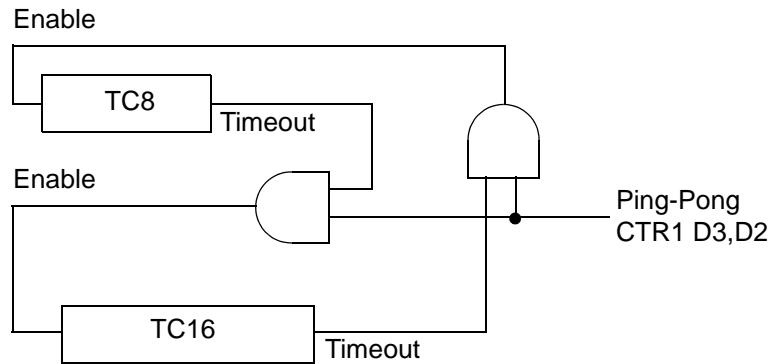
This bit defines whether P35 is used as a normal output pin or T16 output.

#### CTR3 T8/T16 Control Register—CTR3(D)03H

Table 15 lists and briefly describes the fields for this register. This register allows the T<sub>8</sub> and T<sub>16</sub> counters to be synchronized.

**Table 15. CTR3 (D)03H: T8/T16 Control Register**

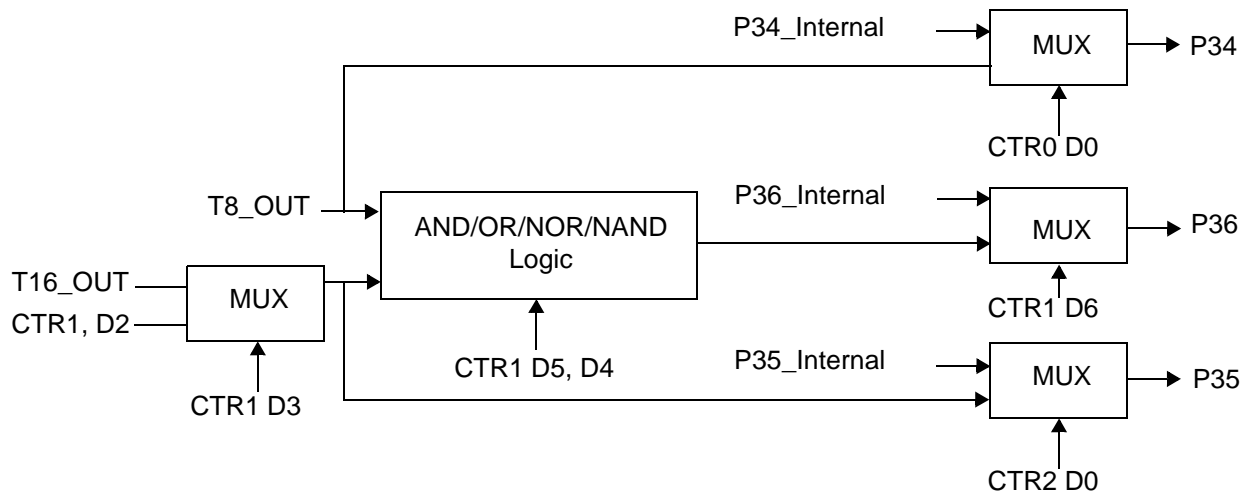
Field	Bit Position		Value	Description
T <sub>16</sub> Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T <sub>8</sub> Enable	-6-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode



**Figure 28. Ping-Pong Mode Diagram**

### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.



**Figure 29. Output Circuit**

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

### During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

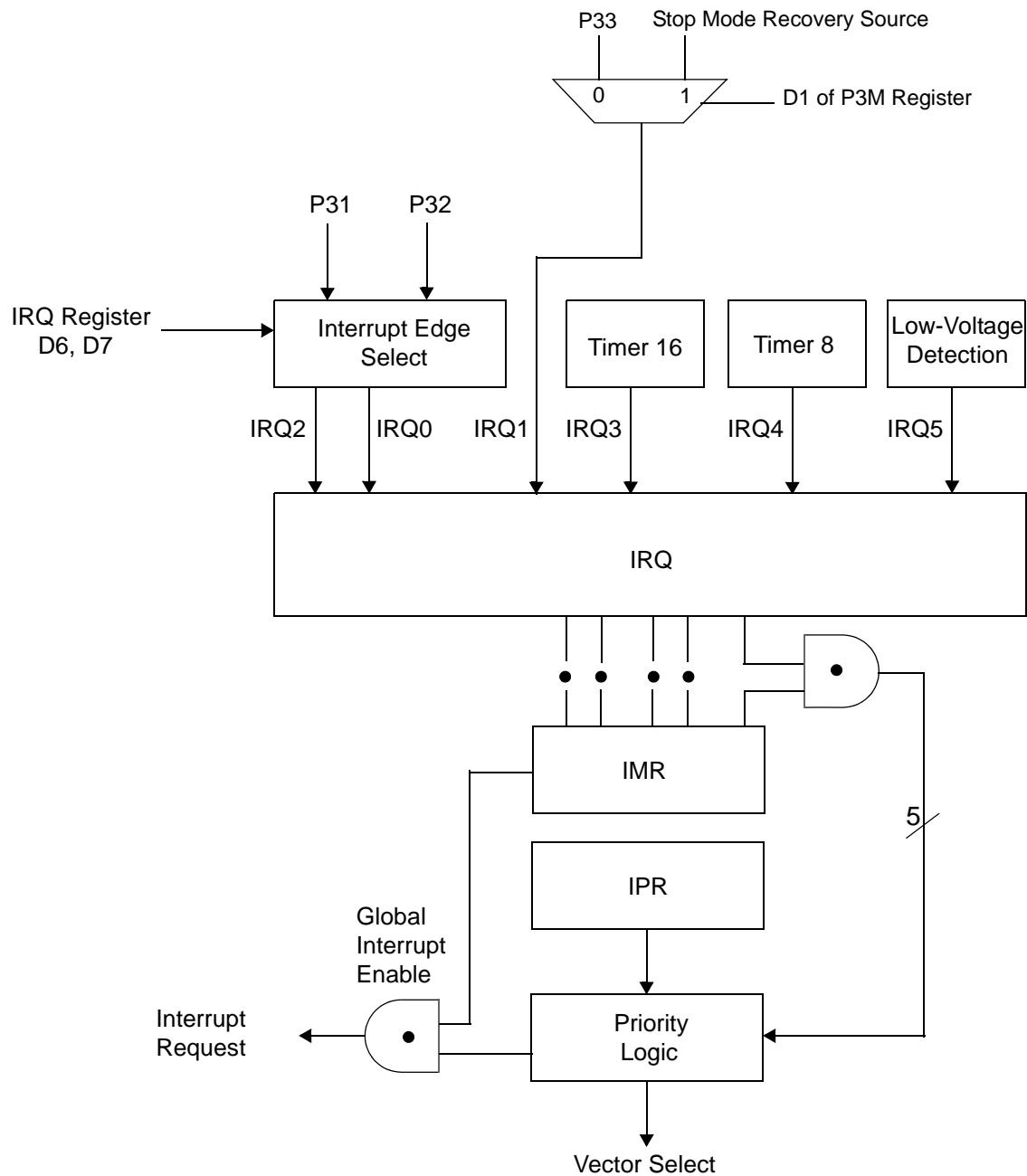
### Timer Output

The output logic for the timers is illustrated in Figure 29. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of T16-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

### Interrupts

The Z8 GP™ OTP MCU Family features six different interrupts (Table 16). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 16) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 57.



**Figure 30. Interrupt Block Diagram**

```
FF      NOP      ; clear the pipeline
6F      Stop     ; enter Stop Mode
```

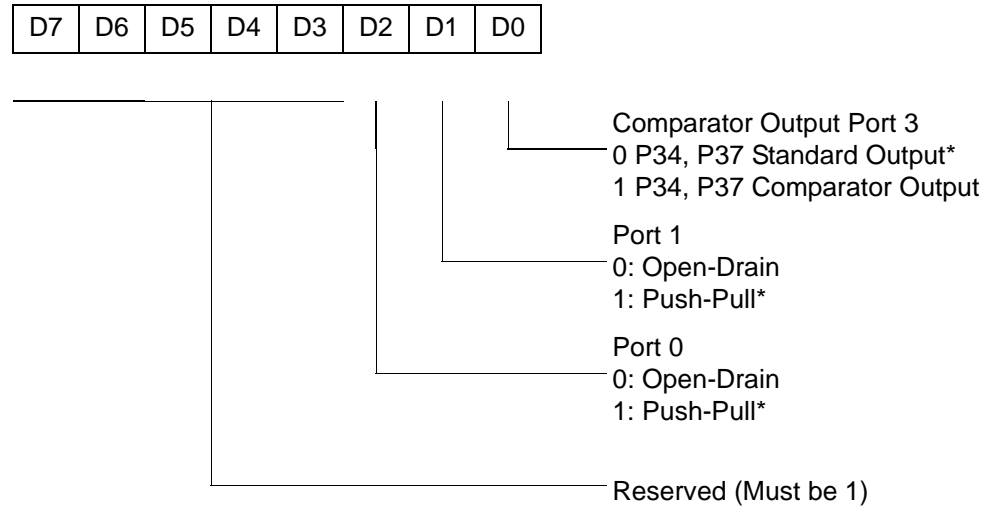
or

```
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

### Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H



\* Default setting after reset

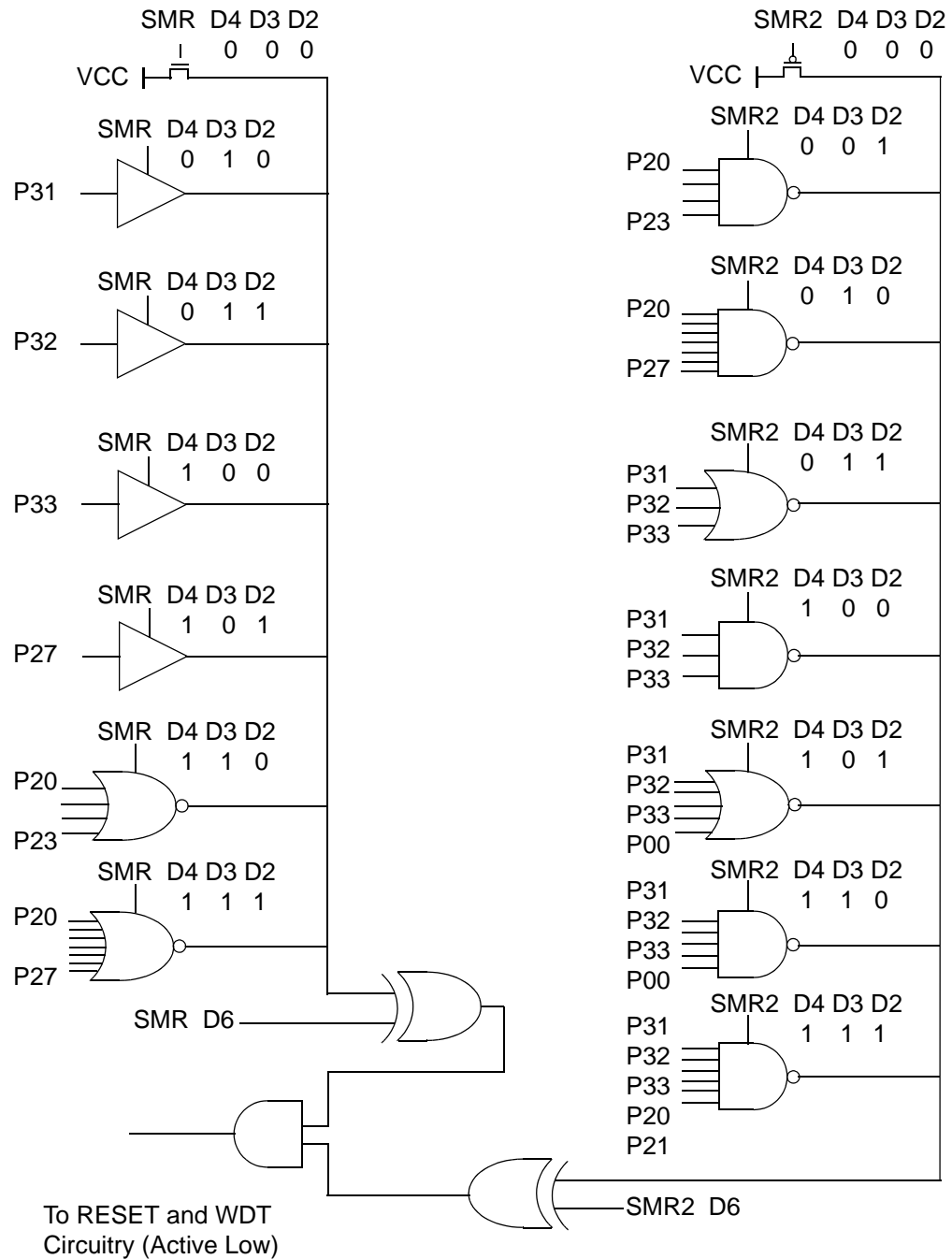
**Figure 32. Port Configuration Register (PCON) (Write Only)**

#### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

#### Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.



**Figure 35. Stop Mode Recovery Source**



### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

**Table 21. EPROM Selectable Options**

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

### Voltage Brown-Out/Standby

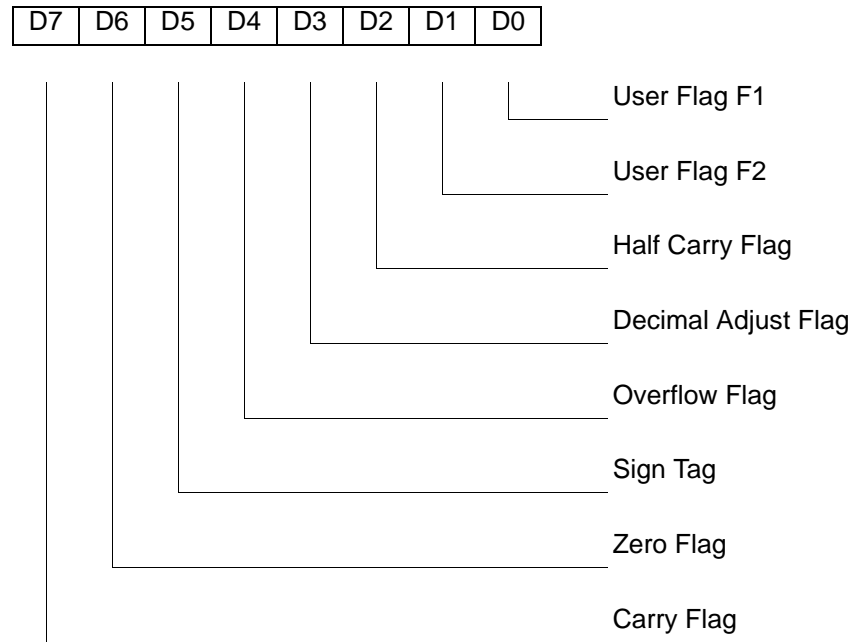
An on-chip Voltage Comparator checks that the  $V_{DD}$  is at the required level for correct operation of the device. Reset is globally driven when  $V_{DD}$  falls below  $V_{BO}$ . A small drop in  $V_{DD}$  causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the  $V_{DD}$  is allowed to stay above  $V_{RAM}$ , the RAM content is preserved. When the power level is returned to above  $V_{BO}$ , the device performs a POR and functions normally.



- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

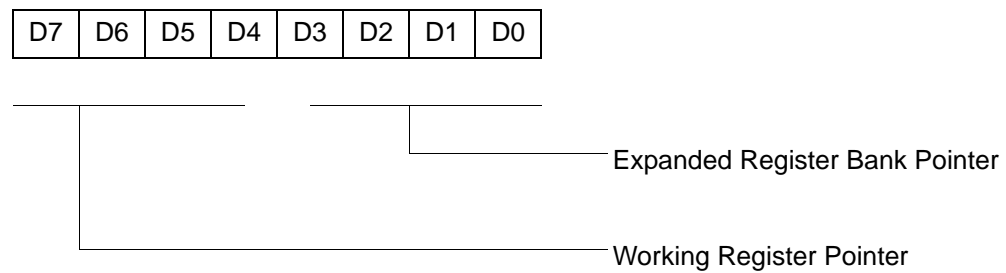
Changing from one mode to another cannot be performed without disabling the counter/timers.

### R252 Flags(FCH)



**Figure 54. Flag Register (FCH: Read/Write)**

### R253 RP(FDH)



Default setting after reset = 0000 0000

**Figure 55. Register Pointer (FDH: Read/Write)**

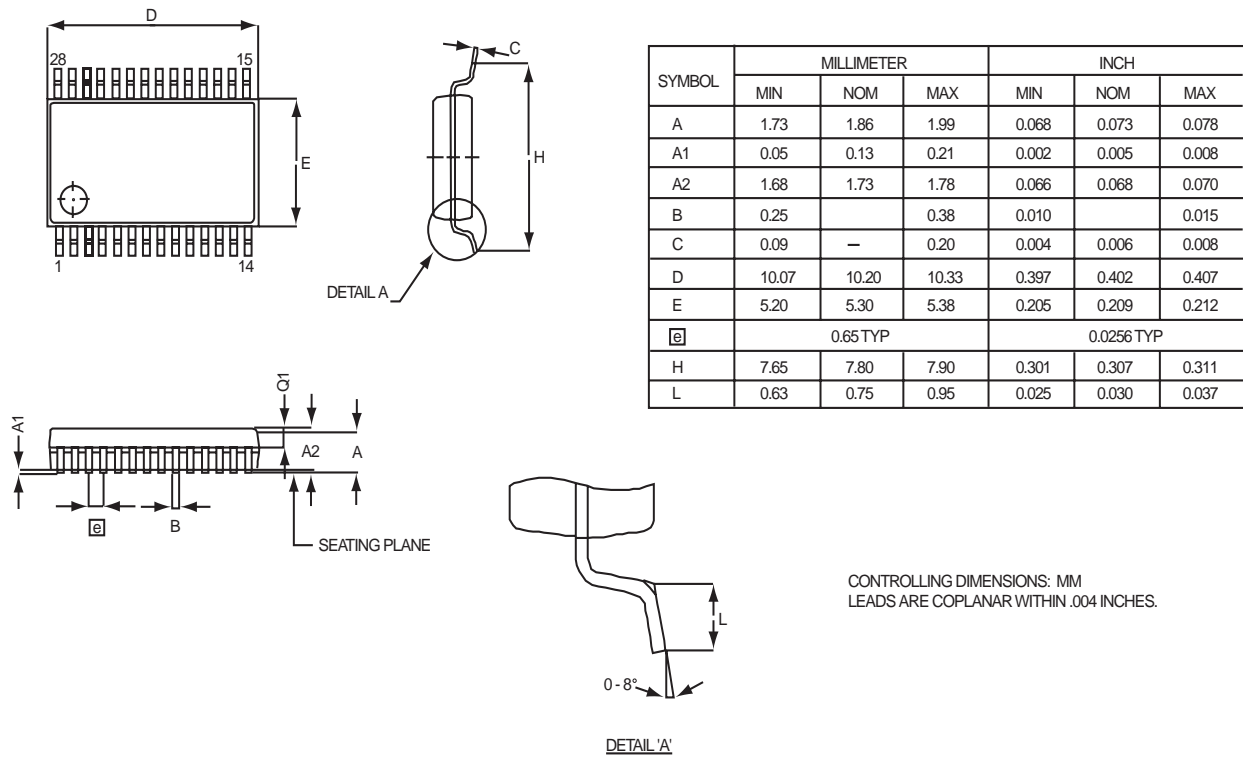


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