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Zilog - ZGP323LSH4804C00TR Datasheet



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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lsh4804c00tr

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List of Tables

Table 1.	Features
Table 2.	Power Connections
Table 3.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification
Table 4.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification
Table 5.	40- and 48-Pin Configuration 8
Table 6.	Absolute Maximum Ratings 10
Table 7.	Capacitance
Table 8.	DC Characteristics 11
Table 9.	EPROM/OTP Characteristics 13
Table 10.	AC Characteristics 15
Table 11.	Port 3 Pin Function Summary 21
Table 12.	CTR0(D)00H Counter/Timer8 Control Register 31
Table 13.	CTR1(0D)01H T8 and T16 Common Functions
Table 14.	CTR2(D)02H: Counter/Timer16 Control Register
Table 15.	CTR3 (D)03H: T8/T16 Control Register
Table 16.	Interrupt Types, Sources, and Vectors
Table 17.	IRQ Register 50
Table 18.	SMR2(F)0DH:Stop Mode Recovery Register 2* 56
Table 19.	Stop Mode Recovery Source 58
Table 20.	Watch-Dog Timer Time Select 61
Table 21.	EPROM Selectable Options 62





Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 5.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.





		\bigcirc	
NC			40 🗖 NC
P25			39 🗖 P24
P26			38 🗖 P23
P27	□ 4		37 🗖 P22
P04	□ 5		36 🗖 P21
P05	□ 6	40-Pin	35 🗖 P20
P06	– 7	PDIP	34 🗖 P03
P14	□ 8	CDIP*	33 🗖 P13
P15	□ 9	ODII	32 🗖 P12
P07	1 0		31 🗖 VSS
VDD	– 11		30 🗖 P02
P16	12		39 🗖 P11
P17	□ 13		28 🗖 P10
XTAL2	□ 14		27 🗖 P01
XTAL1	1 5		26 🗖 P00
P31	1 6		25 🗖 Pref1/P30
P32	1 7		24 🗖 P36
P33	□ 18		23 🗖 P37
P34	□ 19		22 🗖 P35
NC	20		21 🗖 RESET
	1		

Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.



Absolute Maximum Ratings

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximun	n Units	Notes
Ambient temperature under bias	0	+70	С	
Storage temperature	-65	+150	С	
Voltage on any pin with respect to V_{SS}	-0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	
Notes:				

This voltage applies to all pins except the following: V_{DD}, P32, P33 and RESET.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

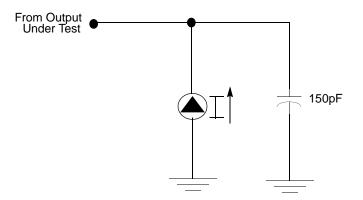


Figure 7. Test Load Diagram

11

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Capacitance

Table 7 lists the capacitances.

Table 7. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ C$, $V_{CC} = GND = 0^\circ$	V, $f = 1.0$ MHz, unmeasured pins returned to GND

DC Characteristics

			T _A = 0°C	to +7	′0°C			
Symbol	Parameter	V _{CC}	Min	Тур	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-3.6	0.8		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-3.6	V _{SS} -0.3		0.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-3.6	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-3.6	V _{SS} -0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-3.6	V _{CC} -0.4			V	I _{OH} = -0.5mA	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 1.0 \text{mA}$ $I_{OL} = 4.0 \text{mA}$	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-3.6	0		V _{DD} -1.75	V		
۱ _{IL}	Input Leakage	2.0-3.6	-1		1	μΑ	V _{IN} = 0V, V _{CC} Pull-ups disabled	
IOL	Output Leakage	2.0-3.6	-1		1	μΑ	$V_{IN} = 0V, V_{CC}$	
ICC	Supply Current	2.0 3.6			10 15	mA mA	at 8.0 MHz at 8.0 MHz	1, 2 1, 2

				Watch-Dog Timer				
No Symbol		Parameter	v _{cc}	Minimum	Maximum	Units	Notes	[⁻] Mode Register (D1, D0)
1	ТрС	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3ТрС			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width	2.0–3.6	12		ns	3	
		Spec		10TpC			4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watch-Dog Timer	2.0–3.6	5		ms		0, 0
		Delay Time	2.0–3.6	10		ms		0, 1
			2.0–3.6	20		ms		1, 0
			2.0–3.6	80		ms		1, 1
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms		

Table 10. AC Characteristics

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0. 2. Interrupt request through Port 3 (P33–P31).

3. SMR – D5 = 1.

4. SMR - D5 = 0.



Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP^{TM} asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP^{TM} does not assert the RESET pin when under VBO.



Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®], functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.



Z8 [®] Standard (Control Registers	Reset Condition
	Expanded Reg. Bank 0/Group 15*	* D7 D6 D5 D4 D3 D2 D1 D0
	FF SPL	
	FE SPH	U U U U U U U U
Register Pointer	FD RP	0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	FC FLAGS	U U U U U U U U
	FB IMR	U U U U U U U U
Working Register Expanded Regist	er FA IRQ	0 0 0 0 0 0 0 0
Group Pointer Bank Pointer	F9 IPR	U U U U U U U U
	F8 P01M	1 1 0 0 1 1 1 1
	* F7 P3M	00000000
	* F6 P2M	1 1 1 1 1 1 1 1
	F5 Reserved	U U U U U U U U
	F4 Reserved	U U U U U U U U
	F3 Reserved	$\cup \cup \cup \cup \cup \cup \cup \cup \cup$
Register File (Bank 0)** /	F2 Reserved	$\cup \cup \cup \cup \cup \cup \cup \cup \cup$
FF F0	F1 Reserved	$\cup \cup \cup \cup \cup \cup \cup \cup \cup$
FU	F0 Reserved	U U U U U U U U
	Expanded Reg. Bank F/Group 0**	
	(F) OF WDTMR	UU001101
	(F) 0E Reserved	
	* (F) 0D SMR2	0 0 0 0 0 0 0 0
	(F) 0C Reserved	
7F	↑ (F) 0B SMR	U 0 1 0 0 0 U 0
/F	(F) 0A Reserved	
	(F) 09 Reserved	
	(F) 08 Reserved	
	(F) 07 Reserved	
	(F) 06 Reserved	
	(F) 05 Reserved	
	(F) 04 Reserved	
	(F) 03 Reserved	
	(F) 02 Reserved	
	(F) 01 Reserved	
Expanded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1 1 1 1 1 0
(0) 03 P3 0 U	Expanded Reg. Bank D/Group 0	
	(D) 0C LVD	$\cup \cup \cup \cup \cup \cup \cup 0$
(0) 02 P2 U	* (D) 0B HI8	000000000
* (0) 01 P1 U	* (D) 0A LO8	000000000
(0) 00 D0	* (D) 09 HI16	0 0 0 0 0 0 0 0
(0) 00 P0 U	* (D) 08 LO16	0 0 0 0 0 0 0 0
U = Unknown	* (D) 07 TC16H	0 0 0 0 0 0 0 0
* Is not reset with a Stop-Mode Recovery	* (D) 06 TC16L	0 0 0 0 0 0 0
** All addresses are in hexadecimal	* (D) 05 TC8H	0 0 0 0 0 0 0
↑ Is not reset with a Stop-Mode Recovery, except Bit 0	* (D) 04 TC8L	0 0 0 0 0 0 0
↑↑ Bit 5 Is not reset with a Stop-Mode Recovery	1↑ (D) 03 CTR3	0 0 0 1 1 1 1 1
$\uparrow\uparrow\uparrow$ Bits 5,4,3,2 not reset with a Stop-Mode Recovery	↑↑↑ (D) 02 CTR2	0 0 0 0 0 0 0
↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0 0 0 0 0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	00000000
	B	·

Figure 15. Expanded Register File Architecture





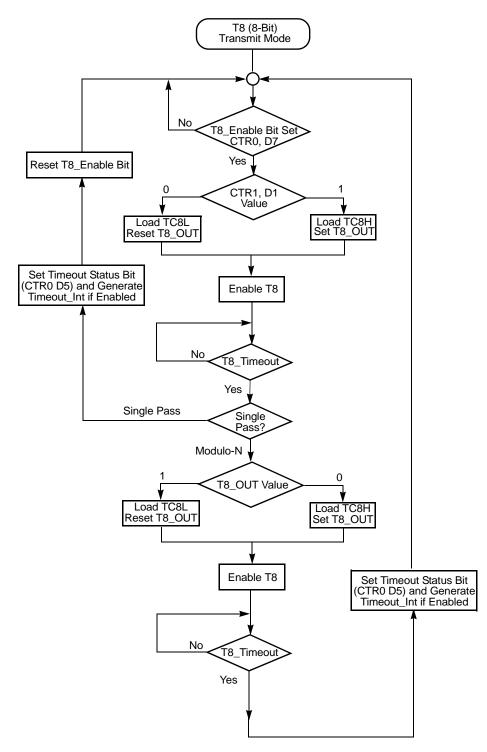


Figure 19. Transmit Mode Flowchart



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

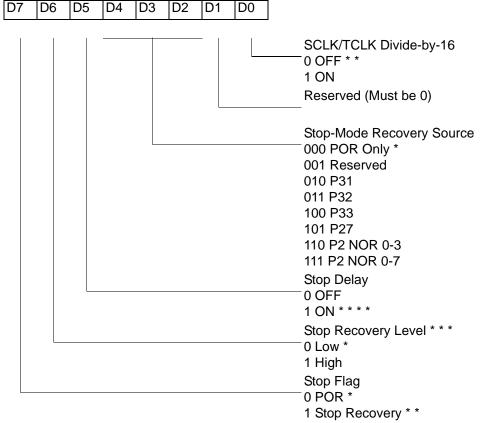
STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:





SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

- * * Set after STOP Mode Recovery
- * * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



Low-Voltage Detection Register—LVD(D)0Ch

Note: Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543			Reserved No Effect
	2	R	1 0*	HVD flag set HVD flag reset
	1-	R	1 0*	LVD flag set LVD flag reset
	0	R/W	1 0*	Enable VD Disable VD
*Default	after POR			

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD}. The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

Notes: If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.



Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H



* Default setting after reset

**Default setting after reset. Not reset with Stop Mode recovery.

Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)



WDTMR(0F)0FH



* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

R246 P2M(F6H)

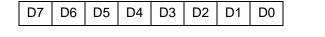


* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)



R250 IRQ(FAH)



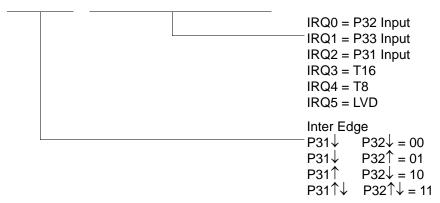
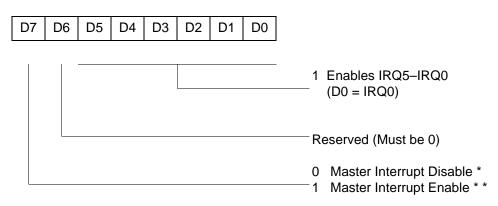


Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset

* * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



R252 Flags(FCH)

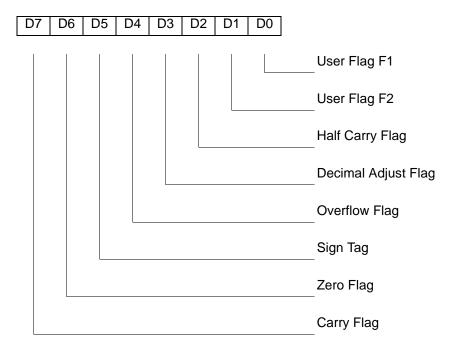
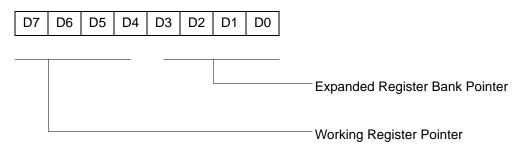


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)









Figure 62. 28-Pin CDIP Package

INCH

NOM

0.073

0.005

0.068

0.006

0.402

0.209

0.307

0.030

0.0256 TYP



MAX

0.078

0.008

0.070

0.015

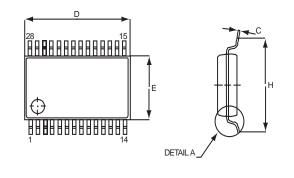
0.008

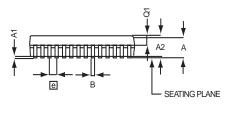
0.407

0.212

0.311

0.037





0-8°

DETAIL 'A'

SYMBOL

А

A1

A2

В

С

D

Е

е

Н

L

MIN

1.73

0.05

1.68

0.25

0.09

10.07

5.20

7.65

0.63

CONTROLLING DIMENSIONS: MM LEADS ARE COPLANAR WITHIN .004 INCHES.

MILLIMETER

NOM

1.86

0.13

1.73

_

10.20

5.30

0.65 TYP

7.80

0.75

MAX

1.99

0.21

1.78

0.38

0.20

10.33

5.38

7.90

0.95

MIN

0.068

0.002

0.066

0.010

0.004

0.397

0.205

0.301

0.025

Figure 65. 28-Pin SSOP Package Diagram



T8 and T16 common control functions 65 T8/T16 control 68 TC16H(D)07h 30 TC16L(D)06h 31 TC8 control 64 TC8H(D)05h 31 TC8L(D)04h 31 voltage detection 69 watch-dog timer 73 register description Counter/Timer2 LS-Byte Hold 31 Counter/Timer2 MS-Byte Hold 30 Counter/Timer8 Control 31 Counter/Timer8 High Hold 31 Counter/Timer8 Low Hold 31 CTR2 Counter/Timer 16 Control 35 CTR3 T8/T16 Control 37 Stop Mode Recovery2 38 T16 Capture LO 30 T8 and T16 Common functions 33 T8_Capture_HI 30 T8 Capture LO 30 register file 28 expanded 24 register pointer 27 detail 29 reset pin function 23 resets and WDT 61

S

SCLK circuit 56 single-pass mode T16_OUT 45 T8_OUT 41 stack 29 standard test conditions 10 standby modes 1 stop instruction, counter/timer 52 stop mode recovery 2 register 59 source 57 stop mode recovery 2 59 stop mode recovery register 55

Т

T16 transmit mode 44 T16_Capture_HI 30 T8 transmit mode 38 T8_Capture_HI 30 test conditions, standard 10 test load diagram 10 timing diagram, AC 14 transmit mode flowchart 39

V

VCC 5 voltage brown-out/standby 62 detection and flags 63 voltage detection register 69

W

watch-dog timer mode registerwatch-dog timer mode register 60 time select 61

Χ

XTAL1 5 XTAL1 pin function 16 XTAL2 5 XTAL2 pin function 16