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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lsp2004g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# **Table of Contents**

Development Features 1
General Description
Pin Description
Absolute Maximum Ratings 10
Standard Test Conditions 10
DC Characteristics
AC Characteristics
Pin Functions 16   XTAL1 Crystal 1 (Time-Based Input) 16   XTAL2 Crystal 2 (Time-Based Output) 16   Port 0 (P07–P00) 16   Port 1 (P17–P10) 17   Port 2 (P27–P20) 18   Port 3 (P37–P30) 19   RESET (Input, Active Low) 23
Functional Description23Program Memory23RAM23Expanded Register File24Register File28Stack29Timers30Counter/Timer Functional Blocks38
Expanded Register File Control Registers (0D) 64
Expanded Register File Control Registers (0F) 69
Standard Control Registers
Package Information
Ordering Information
Precharacterization Product





Figure 2. Counter/Timers Diagram

## **Pin Description**

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 5.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.



40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V <sub>DD</sub>
31	24, 37, 38	V <sub>SS</sub>
25	29	Pref1/P30
	48	NC

### Table 5. 40- and 48-Pin Configuration (Continued)



# **Absolute Maximum Ratings**

Stresses greater than those listed in Table 7 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

#### Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximu	m Units	Notes
Ambient temperature under bias	0	+70	С	
Storage temperature	-65	+150	С	
Voltage on any pin with respect to V <sub>SS</sub>	-0.3	+5.5	V	1
Voltage on $V_{DD}$ pin with respect to $V_{SS}$	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into $V_{DD}$ or out of $V_{SS}$		75	mA	
Notes:				

This voltage applies to all pins except the following: V<sub>DD</sub>, P32, P33 and RESET.

## **Standard Test Conditions**

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).



Figure 7. Test Load Diagram

13

#### Table 9. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	25			Cycles	1

Notes:

1. For windowed cerdip package only.

2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

AF = exp[(Ea/k)\*(1/Tuse - 1/TStress)] Where: Ea is the intrinsic activation energy (eV; typ. 0.8) k is Boltzman's constant (8.67 x 10-5 eV/°K) °K = -273.16°C Tuse = Use Temperature in °K TStress = Stress Temperature in °K 3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>



### **Pin Functions**

### XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

### XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

### Port 0 (P07-P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

**Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to be input following an SMR.





Figure 9. Port 0 Configuration

### Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.



**Note:** The Port 1 direction is reset to be input following an SMR.



CTR1(0D)01H" on page 33). Other edge detect and IRQ modes are described in Table 11.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

#### Table 11. Port 3 Pin Function Summary

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Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTRL0
LD	1, #xx	;	load CTRL1
LD	R1, 2	;	$CTRL2 \rightarrow CTRL1$
LD	RP. #0Dh	;	Select ERF D
for access to bank D	,	,	
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 $\rightarrow$ register 71h			
LD	R1, 2		
; CTRL2→register 71h			

### **Register File**

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The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.





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Figure 24. Demodulation Mode Flowchart



Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16\_OUT in Modulo-N Mode

#### **T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

#### If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).



#### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

#### **Ping-Pong Mode**

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1, D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16\_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

**Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.





Figure 28. Ping-Pong Mode Diagram

#### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.





The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.



#### Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

#### Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 57) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address <code>0BH</code>.





#### SMR(0F)0BH



\* Default after Power On Reset or Watch-Dog Reset

- \* \* Set after STOP Mode Recovery
- \* \* \* At the XOR gate input

\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

#### Figure 33. STOP Mode Recovery Register

#### SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.





**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



#### R247 P3M(F7H)



\* Default setting after reset. Not reset with Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

93

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

#### Codes

ZG = ZiLOG General Purpose Family

P = OTP

- 323 = Family Designation
- L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

- E = -40 to +105 degrees C (Extended)
- A = -40 to +125 degrees C (Automotive)
- P = Package Type:
  - K = Windowed Cerdip
  - P = PDIP
  - H = SSOP
  - S = SOIC
- ## = Number of Pins
- CC = Memory Size
- M = Packaging Options
  - C = Non Lead-Free
  - G = Lead-Free
  - E = CDIP



# D

DC characteristics 11 demodulation mode count capture flowchart 42 flowchart 43 T16 45 T8 41 description functional 23 general 2 pin 4

# Ε

**EPROM** selectable options 62 expanded register file 24 expanded register file architecture 26 expanded register file control registers 69 flag 78 interrupt mask register 77 interrupt priority register 76 interrupt request register 77 port 0 and 1 mode register 75 port 2 configuration register 73 port 3 mode register 74 port configuration register 73 register pointer 78 stack pointer high register 79 stack pointer low register 79 stop-mode recovery register 71 stop-mode recovery register 2 72 T16 control register 67 T8 and T16 common control functions register 65 T8/T16 control register 68 TC8 control register 64 watch-dog timer register 73

### F

features standby modes 1 functional description counter/timer functional blocks 38 CTR(D)01h register 33 CTR0(D)00h register 31 CTR2(D)02h register 35 CTR3(D)03h register 37 expanded register file 24 expanded register file architecture 26 HI16(D)09h register 30 HI8(D)0Bh register 30 L08(D)0Ah register 30 L0I6(D)08h register 30 program memory map 24 **RAM 23** register description 63 register file 28 register pointer 27 register pointer detail 29 SMR2(F)0D1h register 38 stack 29 TC16H(D)07h register 30 TC16L(D)06h register 31 TC8H(D)05h register 31 TC8L(D)04h register 31

## G

glitch filter circuitry 38

# Η

halt instruction, counter/timer 52

## I

input circuit 38 interrupt block diagram, counter/timer 49 interrupt types, sources and vectors 50

### L

low-voltage detection register 63



T8 and T16 common control functions 65 T8/T16 control 68 TC16H(D)07h 30 TC16L(D)06h 31 TC8 control 64 TC8H(D)05h 31 TC8L(D)04h 31 voltage detection 69 watch-dog timer 73 register description Counter/Timer2 LS-Byte Hold 31 Counter/Timer2 MS-Byte Hold 30 Counter/Timer8 Control 31 Counter/Timer8 High Hold 31 Counter/Timer8 Low Hold 31 CTR2 Counter/Timer 16 Control 35 CTR3 T8/T16 Control 37 Stop Mode Recovery2 38 T16 Capture LO 30 T8 and T16 Common functions 33 T8\_Capture\_HI 30 T8 Capture LO 30 register file 28 expanded 24 register pointer 27 detail 29 reset pin function 23 resets and WDT 61

### S

SCLK circuit 56 single-pass mode T16\_OUT 45 T8\_OUT 41 stack 29 standard test conditions 10 standby modes 1 stop instruction, counter/timer 52 stop mode recovery 2 register 59 source 57 stop mode recovery 2 59 stop mode recovery register 55

## Т

T16 transmit mode 44 T16\_Capture\_HI 30 T8 transmit mode 38 T8\_Capture\_HI 30 test conditions, standard 10 test load diagram 10 timing diagram, AC 14 transmit mode flowchart 39

# V

VCC 5 voltage brown-out/standby 62 detection and flags 63 voltage detection register 69

## W

watch-dog timer mode registerwatch-dog timer mode register 60 time select 61

# Χ

XTAL1 5 XTAL1 pin function 16 XTAL2 5 XTAL2 pin function 16