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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323lsp2032g">https://www.e-xfl.com/product-detail/zilog/zgp323lsp2032g</a>

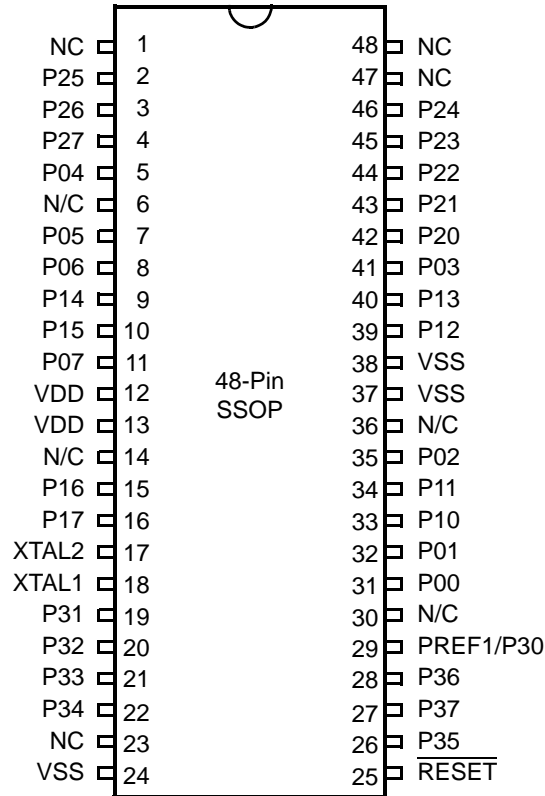
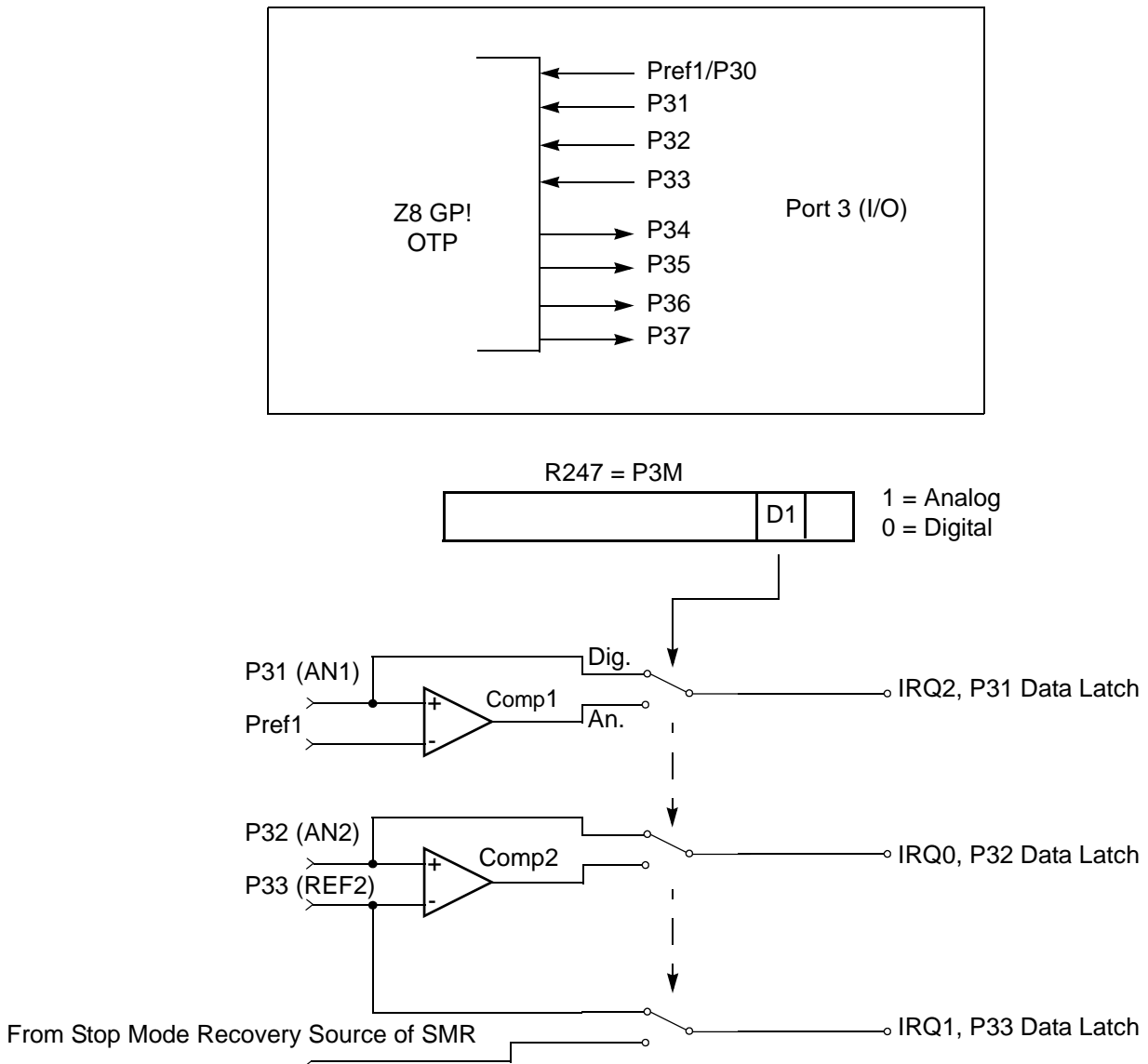


Figure 6. 48-Pin SSOP Pin Configuration

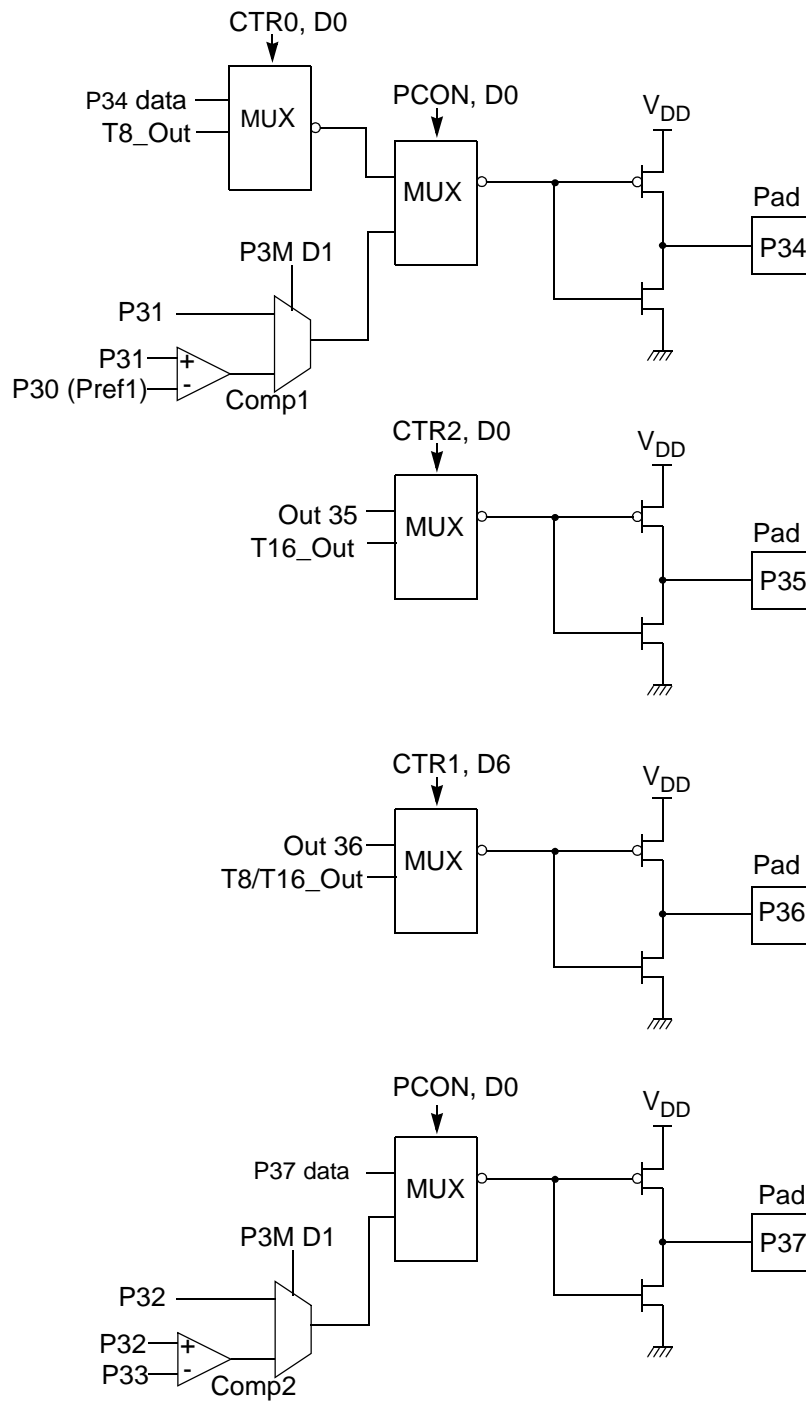
Table 5. 40- and 48-Pin Configuration

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



**Figure 12. Port 3 Configuration**

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—



**Figure 13. Port 3 Counter/Timer Output Configuration**

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          R0, #xx           ; load CTRL0
LD          1, #xx            ; load CTRL1
LD          R1, 2              ; CTRL2→CTRL1

LD          RP, #0Dh          ; Select ERF D
for access to bank D

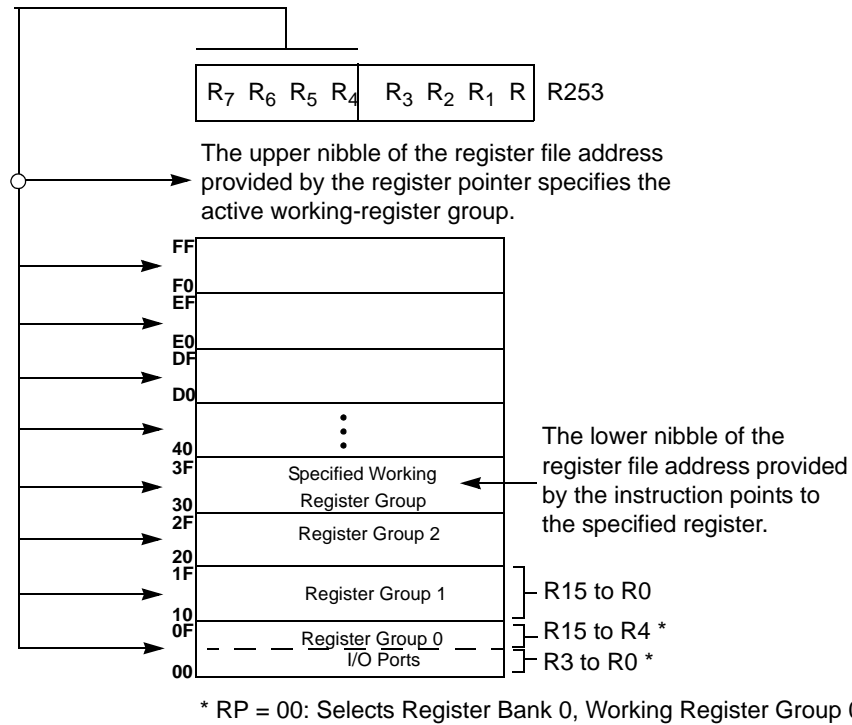
                                ; (working
                                ; register group 0)
LD          RP, #7Dh          ; Select
expanded register bank D and working ; register
group 7 of bank 0 for access.
LD          71h, 2
; CTRL2→register 71h
LD          R1, 2
; CTRL2→register 71h

```

## Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.



**Figure 17. Register Pointer—Detail**

## Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

## Timers

### T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

**T8/T16\_Logic/Edge \_Detect**

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

**Transmit\_Submode/Glitch Filter**

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

**Initial\_T8\_Out/Rising\_Edge**

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

**Initial\_T16 Out/Falling \_Edge**

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16\_OUT.

**CTR2 Counter/Timer 16 Control Register—CTR2(D)02H**

Table 14 lists and briefly describes the fields for this register.



**Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)**

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

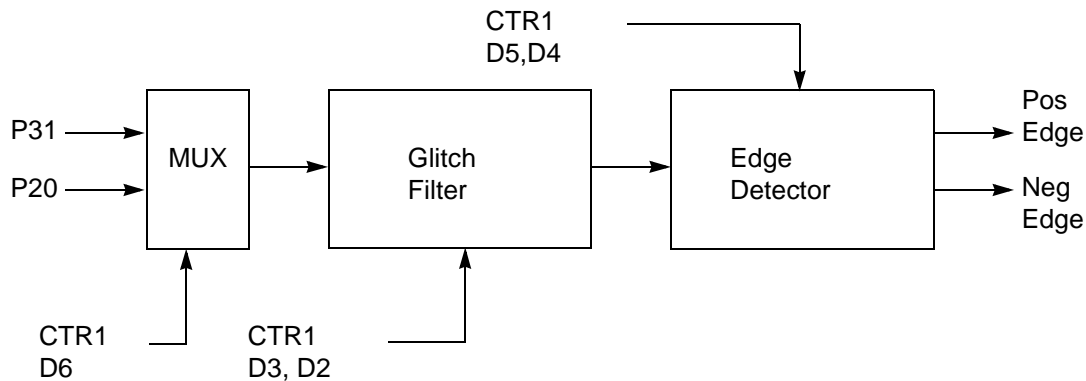
Note: \*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

## Counter/Timer Functional Blocks

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).



**Figure 18. Glitch Filter Circuitry**

### T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8\_OUT is 1; if it is 1, T8\_OUT is 0. See Figure 19.

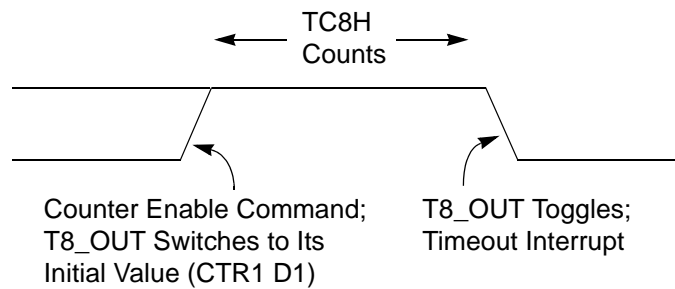
► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF<sub>h</sub> is not a timeout condition.

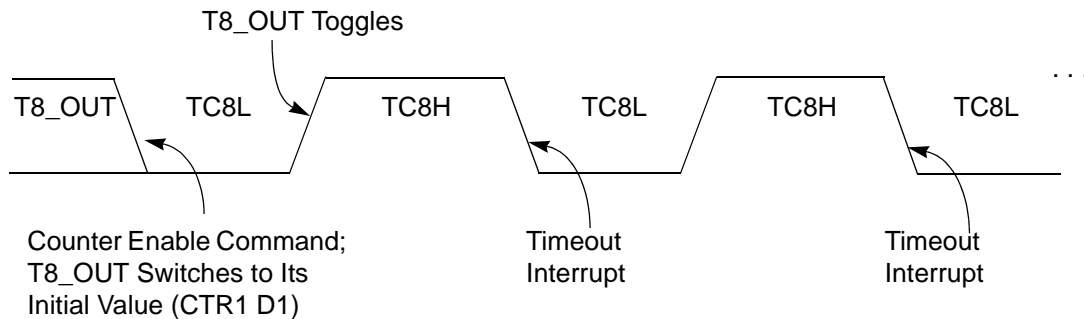


**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.



**Figure 21. T8\_OUT in Single-Pass Mode**



**Figure 22. T8\_OUT in Modulo-N Mode**

### T8 Demodulation Mode

The user must program TC8L and TC8H to FF<sub>h</sub>. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

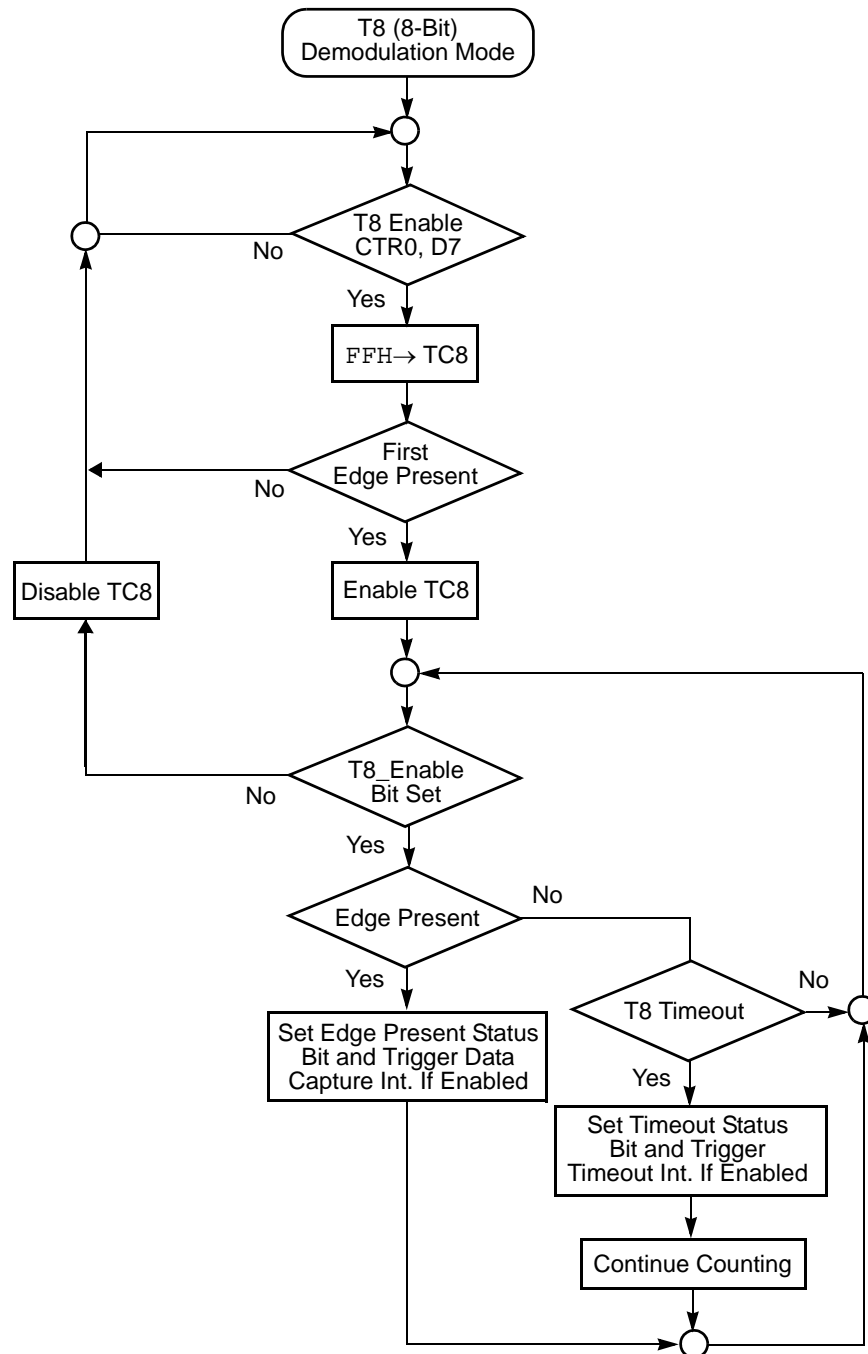


Figure 24. Demodulation Mode Flowchart

### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

### Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1, D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16\_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

### Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### Stop-Mode Recovery Register (SMR)

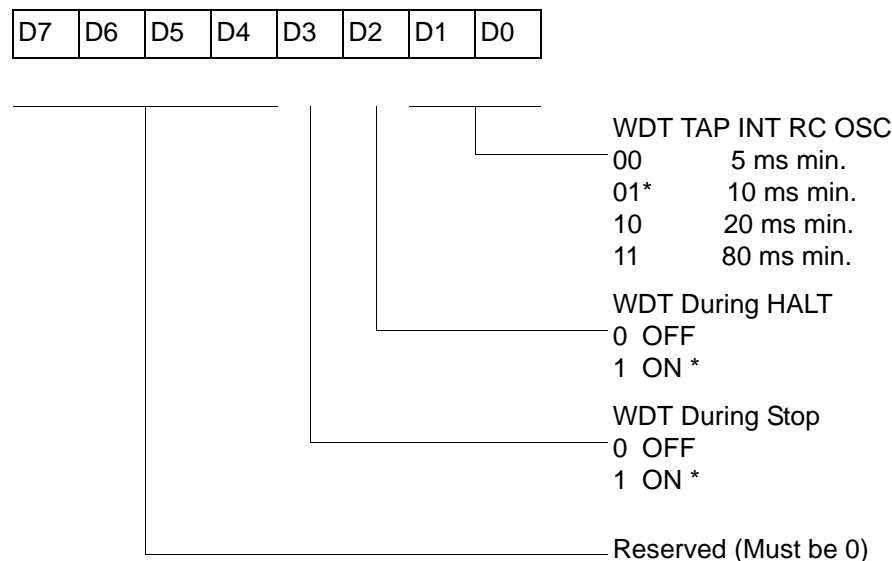
This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 57) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

### Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8® CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh

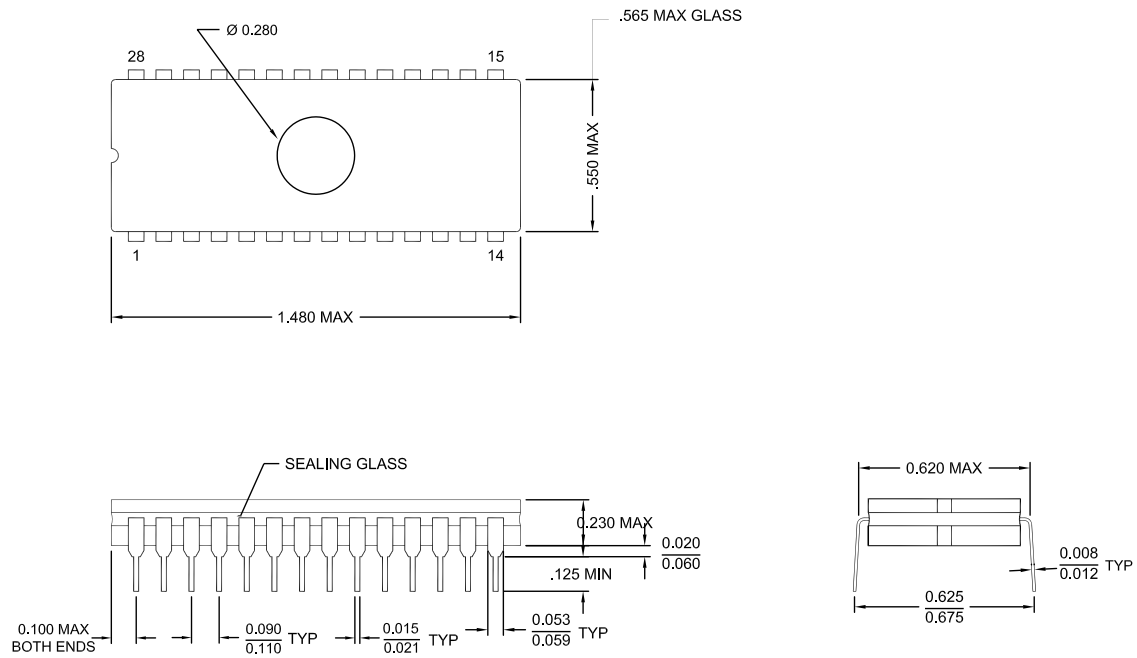


\* Default setting after reset

**Figure 37. Watch-Dog Timer Mode Register (Write Only)**

### WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 20.



**Figure 62. 28-Pin CDIP Package**

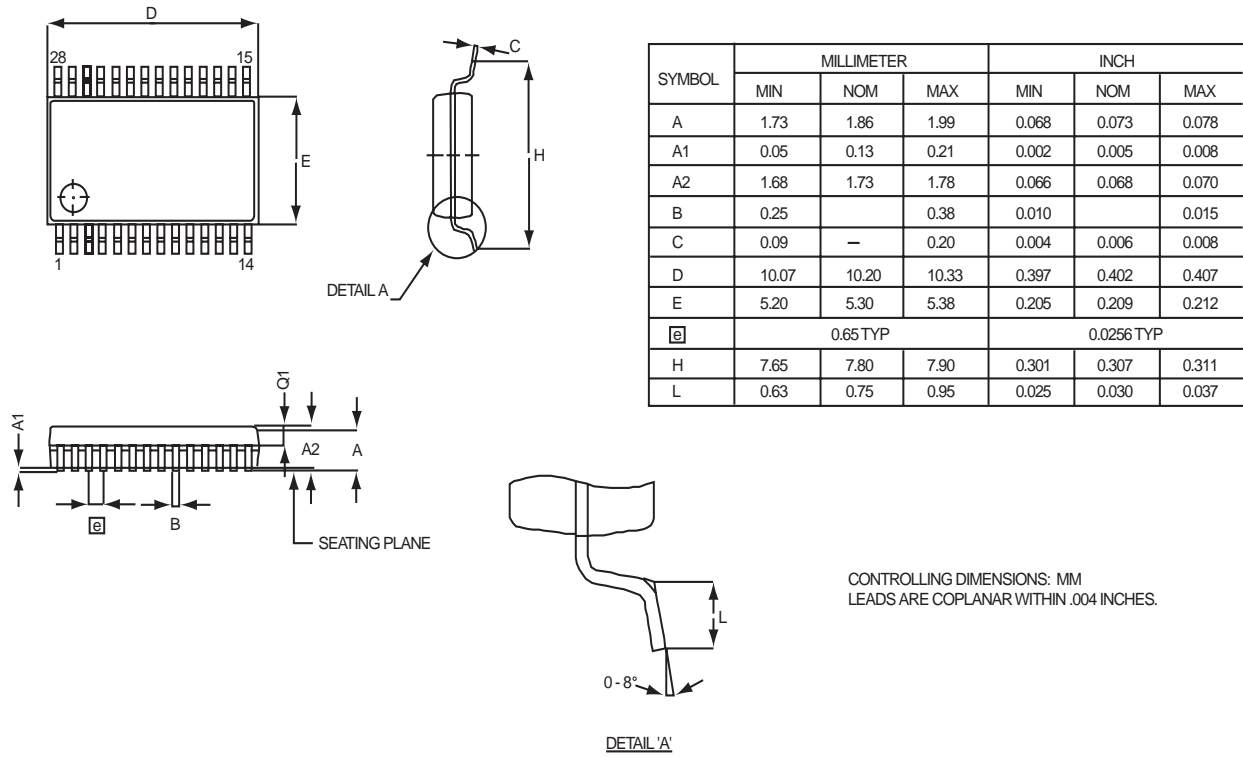
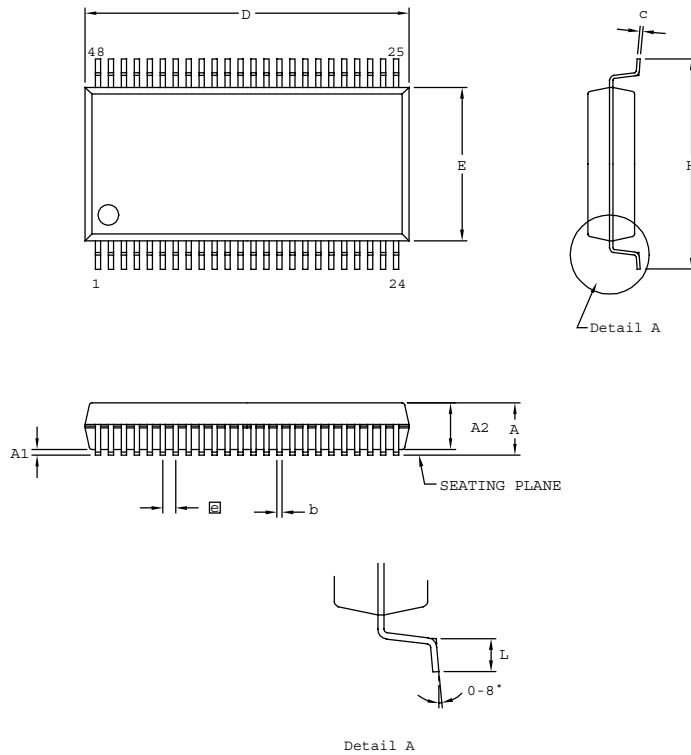


Figure 65. 28-Pin SSOP Package Diagram





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
ⓐ	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM  
LEADS ARE COPLANAR WITHIN .004 INCH

**Figure 68. 48-Pin SSOP Package Design**

- **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.




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**8KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323LSH4808C	48-pin SSOP 8K OTP	ZGP323LSS2808C	28-pin SOIC 8K OTP
ZGP323LSP4008C	40-pin PDIP 8K OTP	ZGP323LSH2008C	20-pin SSOP 8K OTP
ZGP323LSH2808C	28-pin SSOP 8K OTP	ZGP323LSP2008C	20-pin PDIP 8K OTP
ZGP323LSP2808C	28-pin PDIP 8K OTP	ZGP323LSS2008C	20-pin SOIC 8K OTP

---



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**8KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323LEH4808C	48-pin SSOP 8K OTP	ZGP323LES2808C	28-pin SOIC 8K OTP
ZGP323LEP4008C	40-pin PDIP 8K OTP	ZGP323LEH2008C	20-pin SSOP 8K OTP
ZGP323LEH2808C	28-pin SSOP 8K OTP	ZGP323LEP2008C	20-pin PDIP 8K OTP
ZGP323LEP2808C	28-pin PDIP 8K OTP	ZGP323LES2008C	20-pin SOIC 8K OTP

---



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**8KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323LAH4808C	48-pin SSOP 8K OTP	ZGP323LAS2808C	28-pin SOIC 8K OTP
ZGP323LAP4008C	40-pin PDIP 8K OTP	ZGP323LAH2008C	20-pin SSOP 8K OTP
ZGP323LAH2808C	28-pin SSOP 8K OTP	ZGP323LAP2008C	20-pin PDIP 8K OTP
ZGP323LAP2808C	28-pin PDIP 8K OTP	ZGP323LAS2008C	20-pin SOIC 8K OTP

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Note: Replace C with G for Lead-Free Packaging

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For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

**Codes**

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

E = -40 to +105 degrees C (Extended)

A = -40 to +125 degrees C (Automotive)

P = Package Type:

K = Windowed Cerdip

P = PDIP

H = SSOP

S = SOIC

## = Number of Pins

CC = Memory Size

M = Packaging Options

C = Non Lead-Free

G = Lead-Free

E = CDIP



## **Precharacterization Product**

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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