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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323lsp2804c">https://www.e-xfl.com/product-detail/zilog/zgp323lsp2804c</a>



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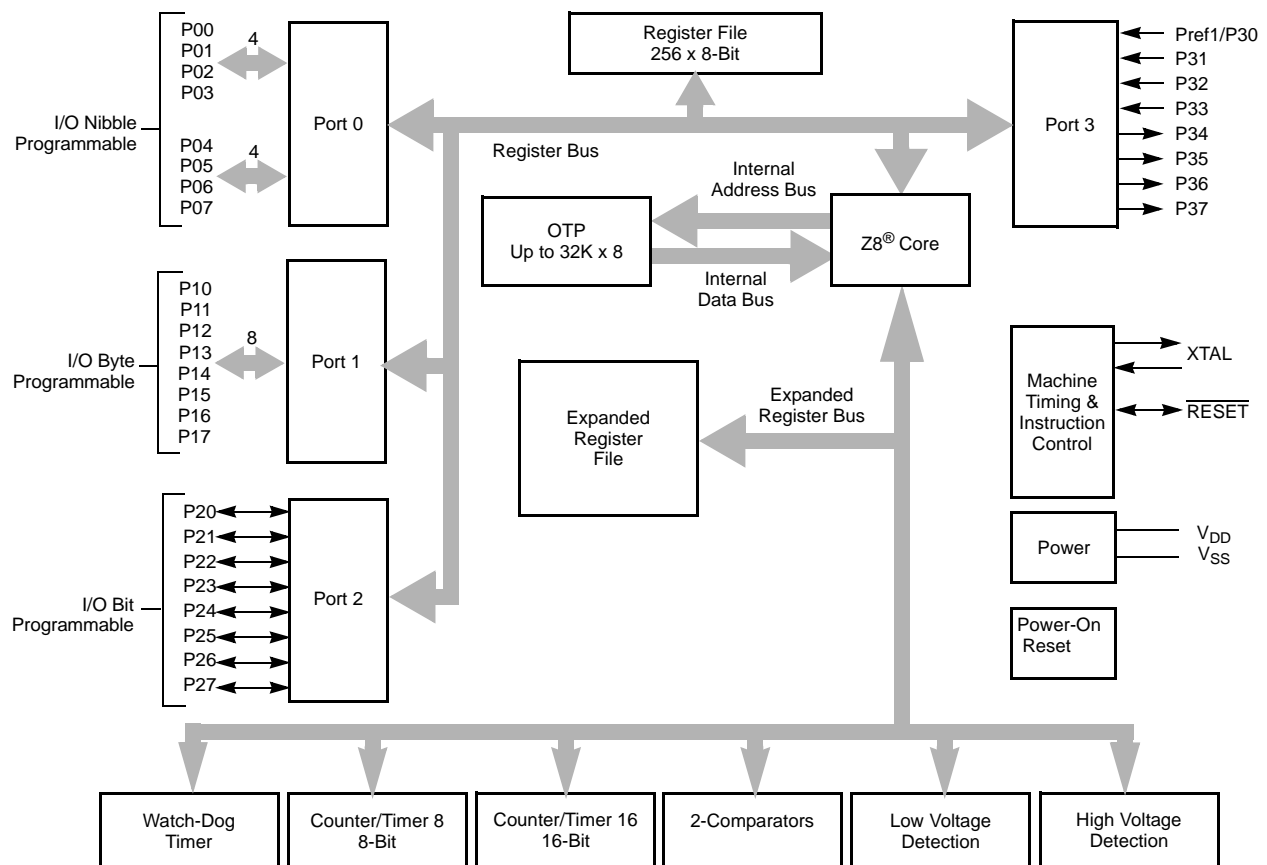
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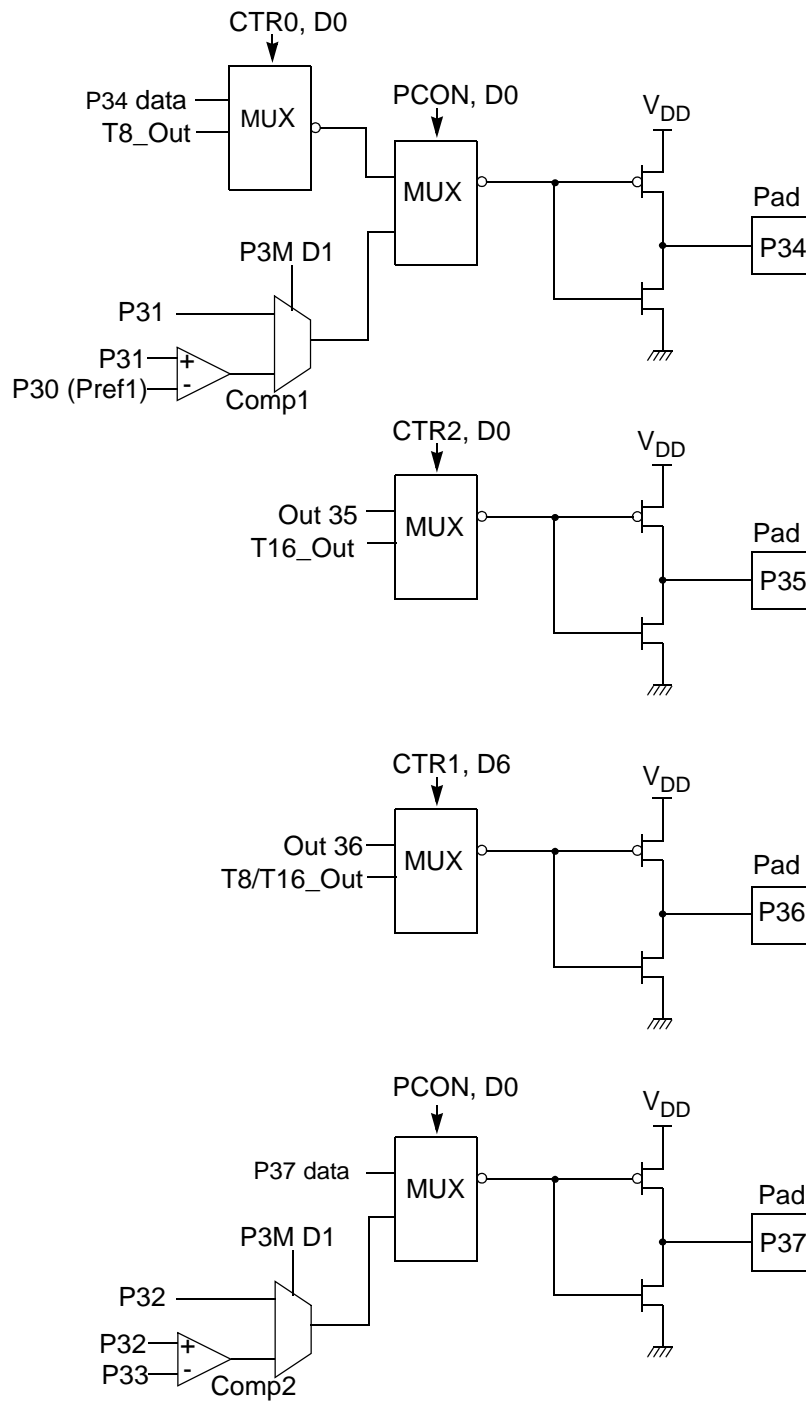
**Table 2. Power Connections**

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>



Note: Refer to the specific package for available pins.

**Figure 1. Functional Block Diagram**



**Figure 13. Port 3 Counter/Timer Output Configuration**

### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 20. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

- **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP™ asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP™ does not assert the RESET pin when under VBO.

- **Note:** The external Reset does not initiate an exit from STOP mode.

## Functional Description

This device incorporates special functions to enhance the Z8®, functionality in consumer and battery-operated applications.

### Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

### RAM

This device features 256B of RAM. See Figure 14.

## Timers

### T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_LO—L016(D)08H

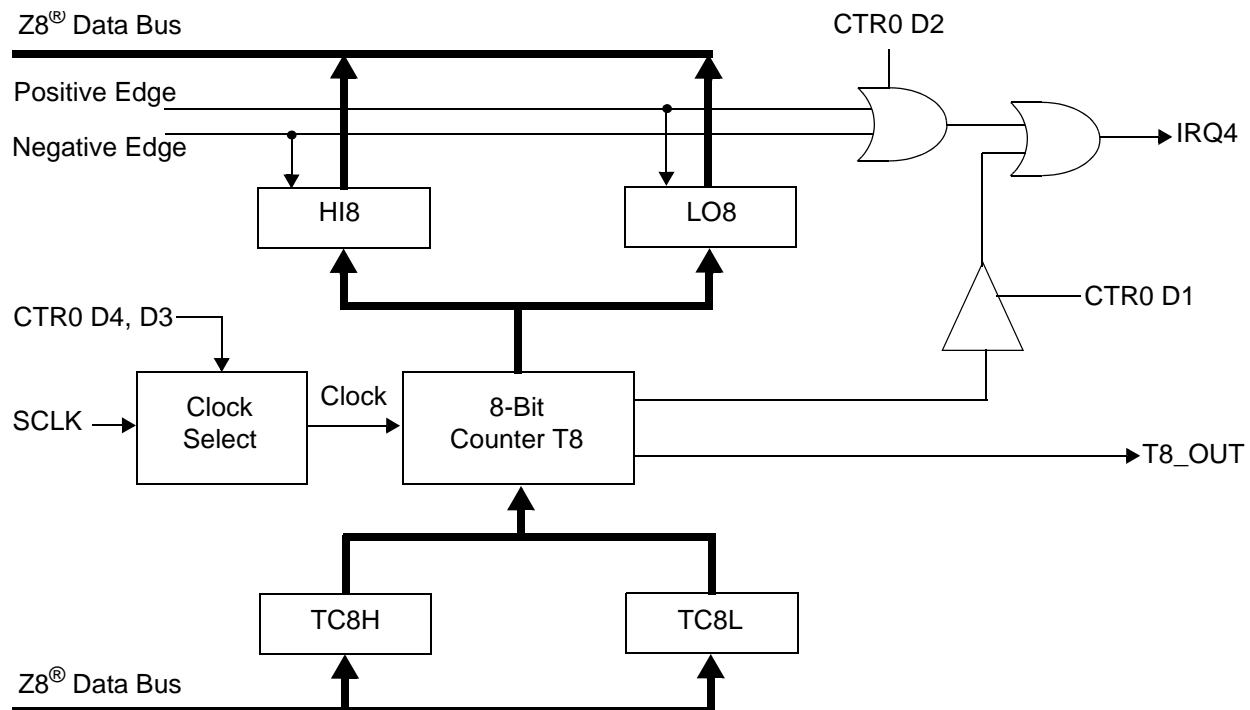
This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8\_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8\_OUT level and repeats the cycle. See Figure 20.



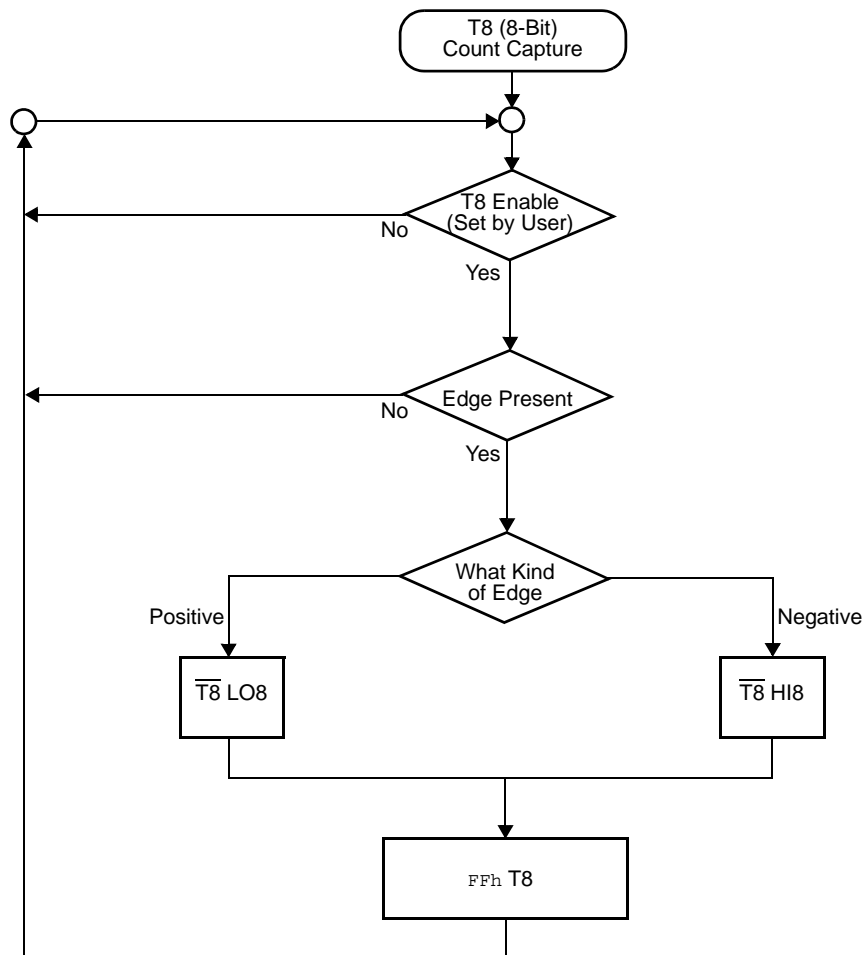
**Figure 20. 8-Bit Counter/Timer Circuits**

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



**Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).



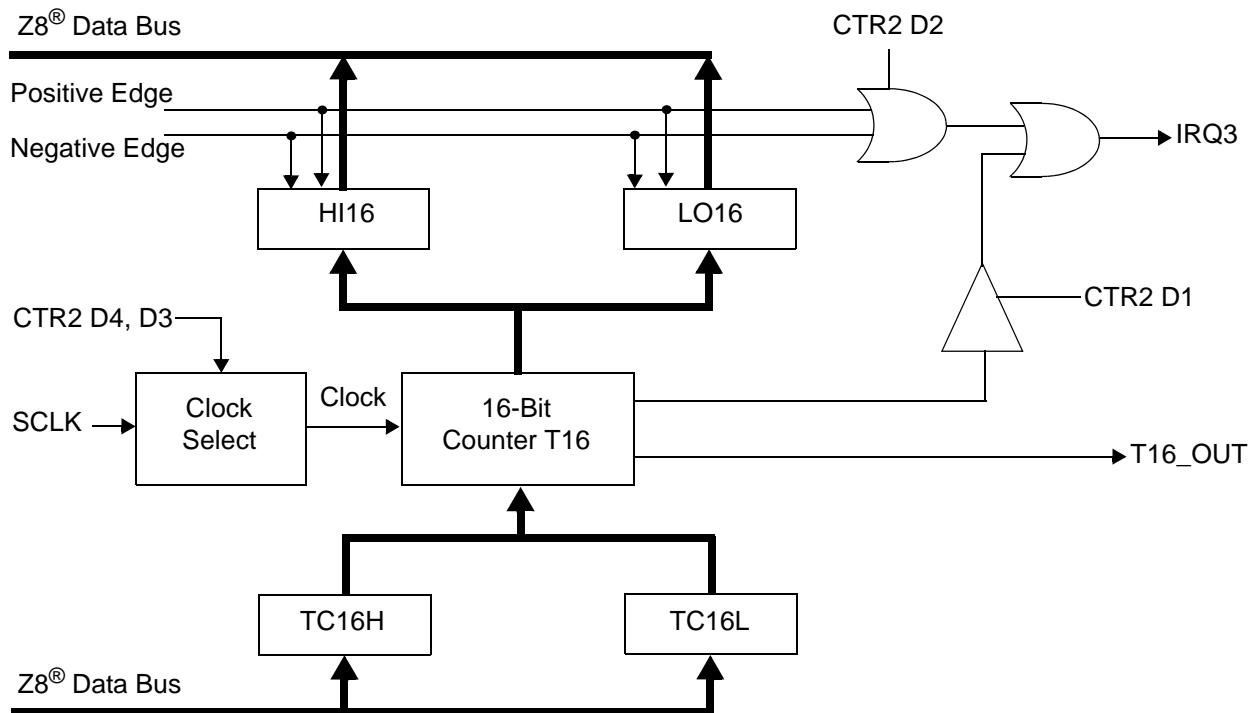
**Figure 23. Demodulation Mode Count Capture Flowchart**



### T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16\_OUT is a 1; if it is a 1, T16\_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H \* 256 + TC16L is loaded, and T16\_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16\_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



**Figure 25. 16-Bit Counter/Timer Circuits**

► **Note:** Global interrupts override this function as described in “Interrupts” on page 48.

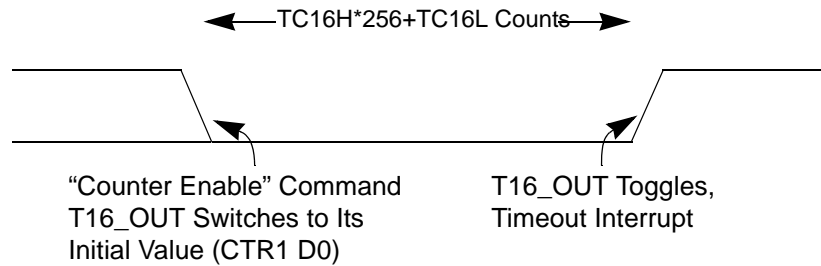
If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H \* 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

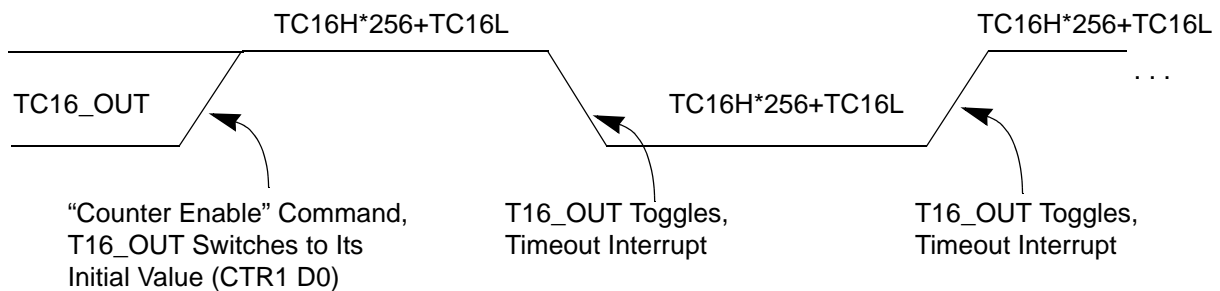


**Caution:**

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE<sub>H</sub>. Transition from 0 to FFFF<sub>H</sub> is not a timeout condition.



**Figure 26. T16\_OUT in Single-Pass Mode**



**Figure 27. T16\_OUT in Modulo-N Mode**

**T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FF<sub>H</sub>. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

**If D6 of CTR2 Is 0**

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF<sub>H</sub> and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

```
FF      NOP      ; clear the pipeline
6F      Stop     ; enter Stop Mode
```

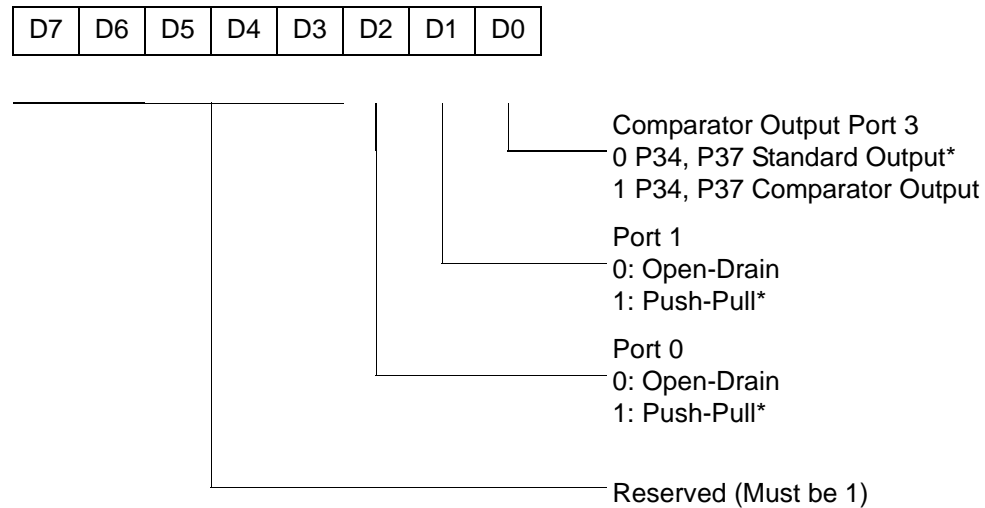
or

```
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

### Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H



\* Default setting after reset

**Figure 32. Port Configuration Register (PCON) (Write Only)**

#### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

#### Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

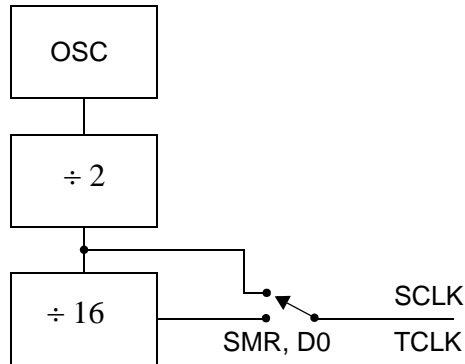


Figure 34. SCLK Circuit

### Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 19).

### Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 18 lists and briefly describes the fields for this register.

Table 18. SMR2(F)0DH:Stop Mode Recovery Register 2\*

Field	Bit Position	Value	Description
Reserved	7-----	0	Reserved (Must be 0)
Recovery Level	-6-----	W 0 <sup>†</sup> 1	Low High
Reserved	--5-----	0	Reserved (Must be 0)
Source	---432--	W 000 <sup>†</sup> 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND of P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	-----10	00	Reserved (Must be 0)

**Notes:**

\* Port pins configured as outputs are ignored as a SMR recovery source.

<sup>†</sup> Indicates the value upon Power-On Reset

Table 19. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 59 for other recover sources.

#### Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the  $T_{POR}$  delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5  $T_{pC}$ .

- **Note:** It is recommended that this bit be set to 1 if using a crystal or resonator clock source. The  $T_{POR}$  delay allows the clock source to stabilize before executing instructions.

#### Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

#### Cold or Warm Start (D7)

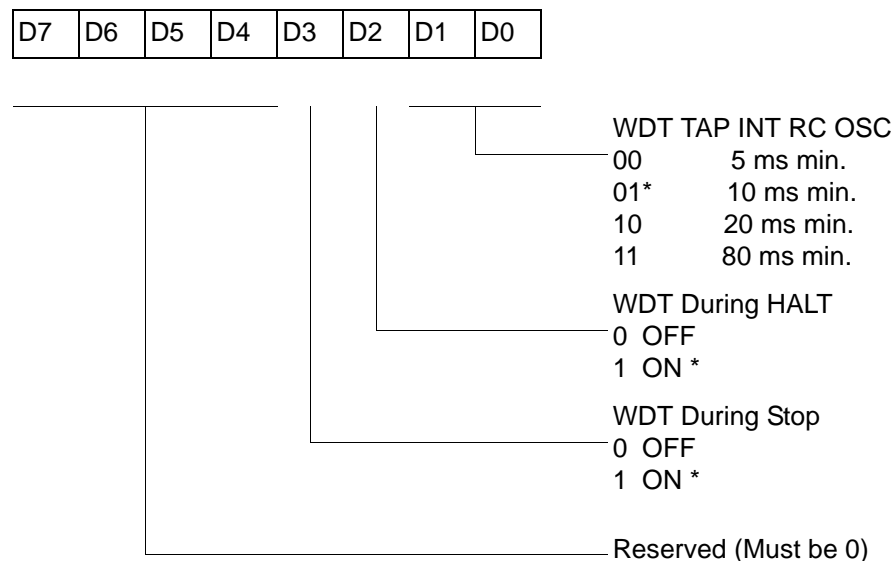
This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

### Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8® CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



\* Default setting after reset

**Figure 37. Watch-Dog Timer Mode Register (Write Only)**

### WDT Time Select (D0, D1)

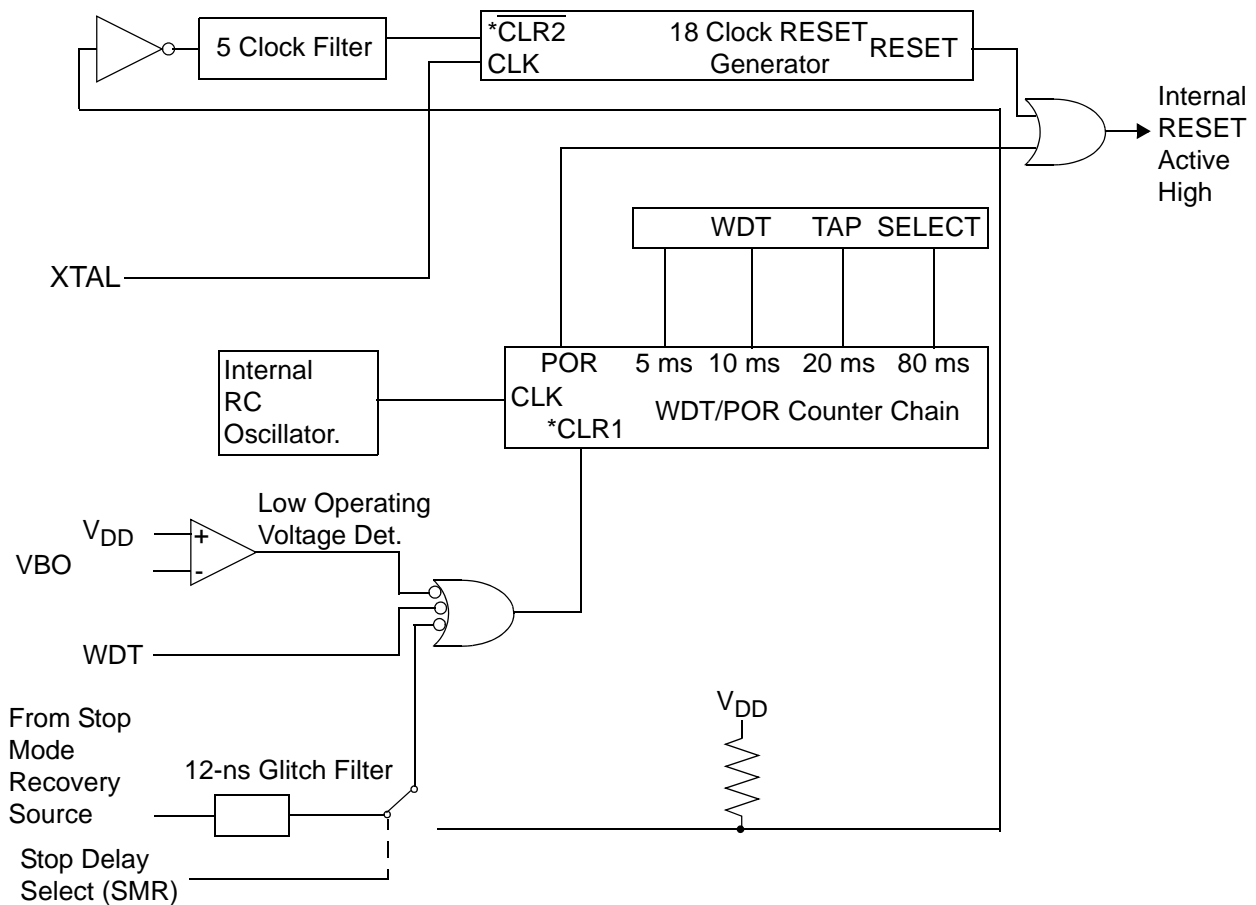
This bit selects the WDT time period. It is configured as indicated in Table 20.

**Table 20. Watch-Dog Timer Time Select**

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

### WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.

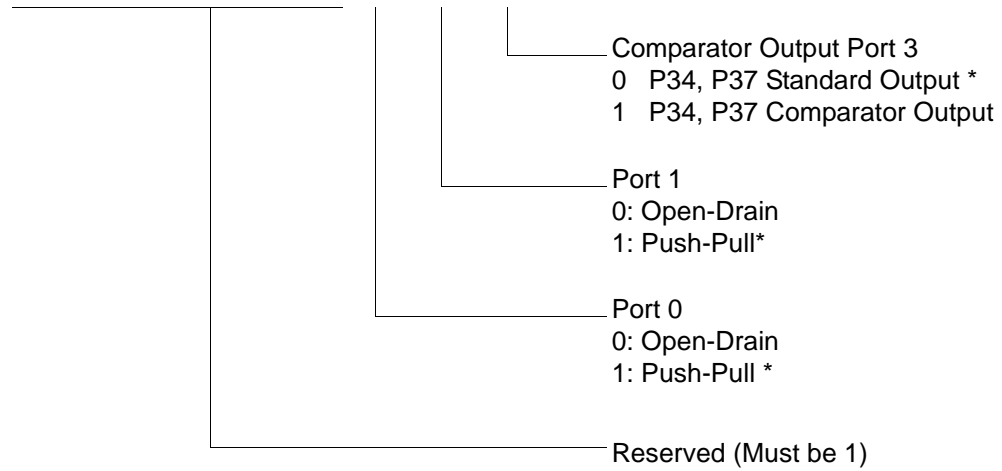


\* CLR1 and  $\overline{\text{CLR2}}$  enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

**Figure 38. Resets and WDT**

PCON(0F)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

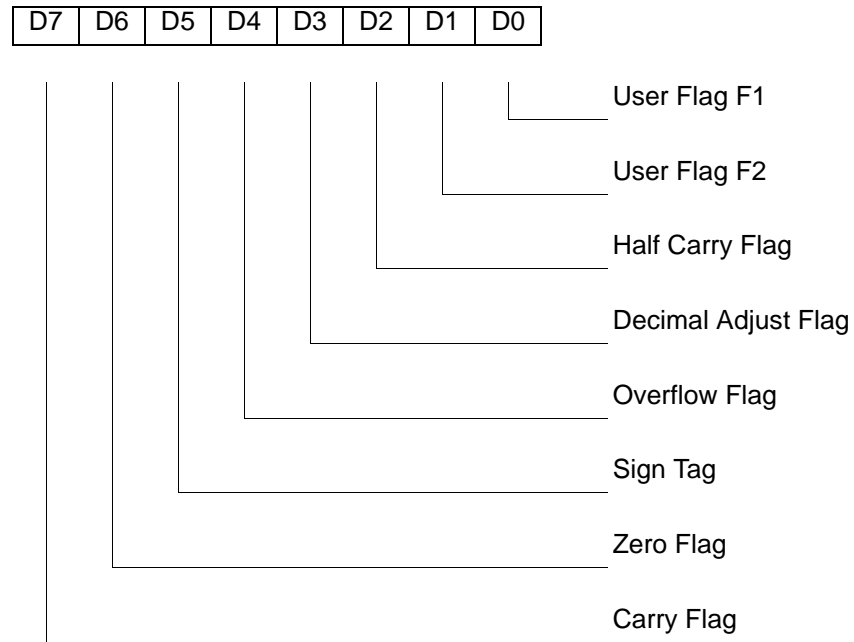


\* Default setting after reset

**Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)**

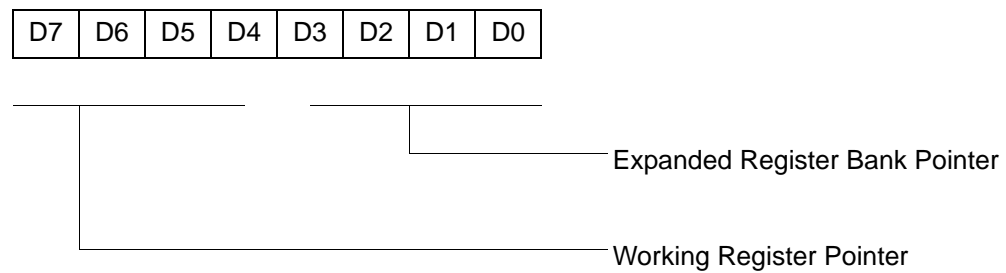


### R252 Flags(FCH)



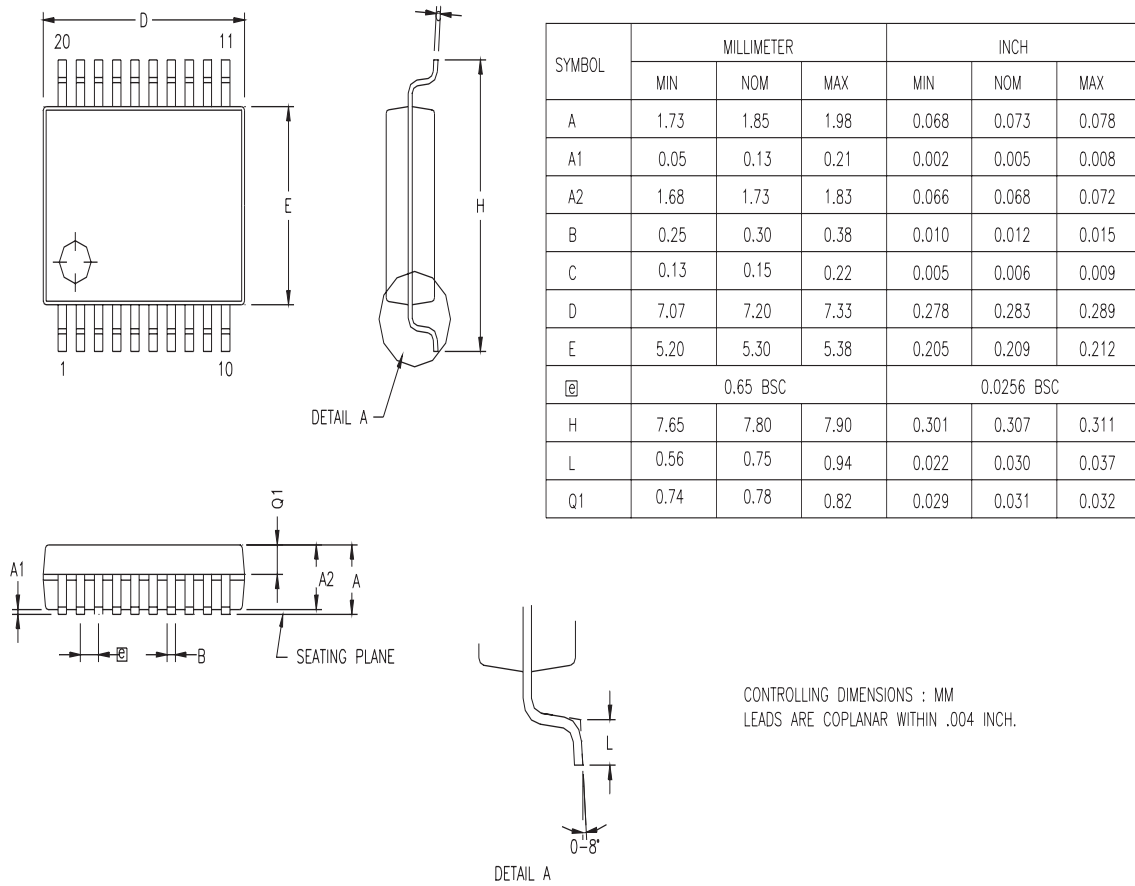
**Figure 54. Flag Register (FCH: Read/Write)**

### R253 RP(FDH)



Default setting after reset = 0000 0000

**Figure 55. Register Pointer (FDH: Read/Write)**



**Figure 61. 20-Pin SSOP Package Diagram**

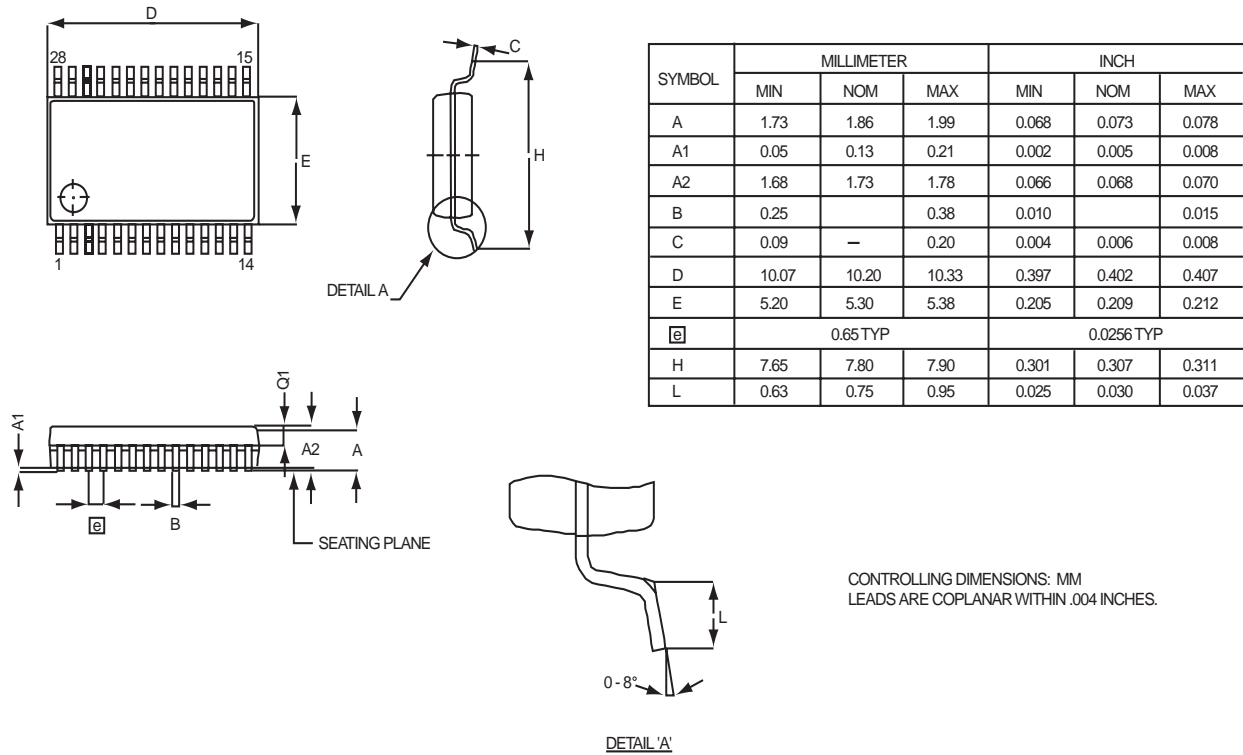


Figure 65. 28-Pin SSOP Package Diagram

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